NOTE: The theory in this application note is still applicable, but some of the products referenced may be discontinued.

Quiescent Current Thermal Tracking Circuit in the RF Integrated Circuit Family

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INTRODUCTION

During a power amplifier design phase, an important item for a designer to consider is the management of performance over temperature. One of the main parameters that affects performance is the quiescent current. The challenge for a designer is to maintain constant quiescent current over a large temperature range. The problem becomes more challenging in a multistage IC (integrated circuit). To overcome this difficulty, Freescale has embedded a quiescent current thermal tracking circuit in its recently introduced family of RF power integrated circuits.

This application note reviews the tracking circuit implemented in the RF power integrated circuit family, its static characterization and its impact on linearity.

This information is applicable to the MW4IC2020, MW4IC2230, MWIC930, MW4IC915, MHVIC2115 and MHVIC915 products.

First is a review of the LDMOS thermal behavior, then an analysis of the thermal tracking circuit and its functioning. A discussion of how it reacts to different bias sources follows, and the capability of the user to disable it. The next part discusses the characterization results of the thermal tracking under DC conditions. Finally, the characterization under RF conditions is presented.

LDMOS THERMAL BEHAVIOR

Figure 1 presents the quiescent current thermal behavior of a 30 Watt LDMOS device.

The drain-source current is strongly impacted by temperature. In Class AB and for a given V_{GS}, the I_{DQ} rises with temperature. Consequently, the shapes of the AM/AM response as well as linearity are affected by temperature.

Figure 2 presents the third order IMD for a 2-tone CW excitation for two different quiescent currents. As expected, the I_{DQ} variation has a strong effect on the third order IMD behavior.

CIRCUIT IMPLEMENTATION

The thermal tracking device is a very small integrated LDMOS FET transistor that is located next to the active LDMOS die area on the die. There are several such thermal tracking FETs in an LDMOS IC.

A thermal tracking transistor has its gate and drain connected together, and its source is connected to ground (see Figure 3).

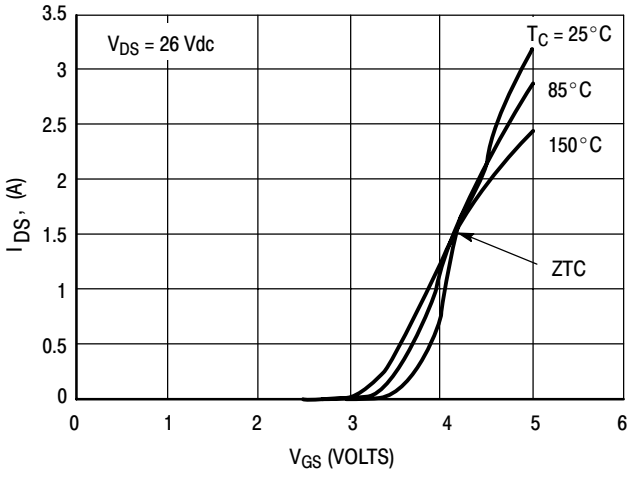

Figure 1. I_{DS} versus V_{GS} and Case Temperature

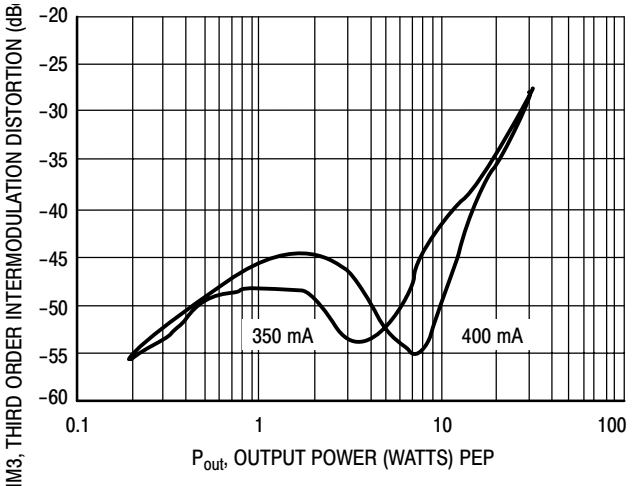

Figure 2. Third Order Intermodulation Distortion versus Quiescent Current, Single Stage

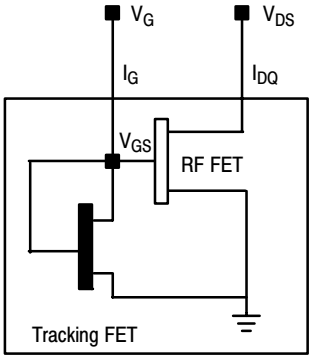

Figure 3. Thermal Tracking Schematic

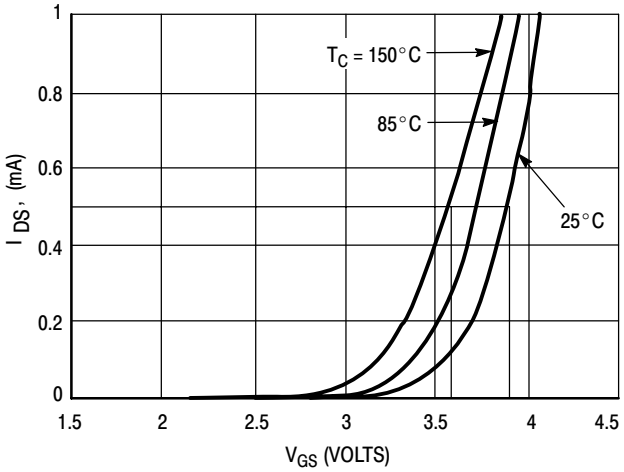

Figure 4. Thermal Tracking FET, DC Characteristic

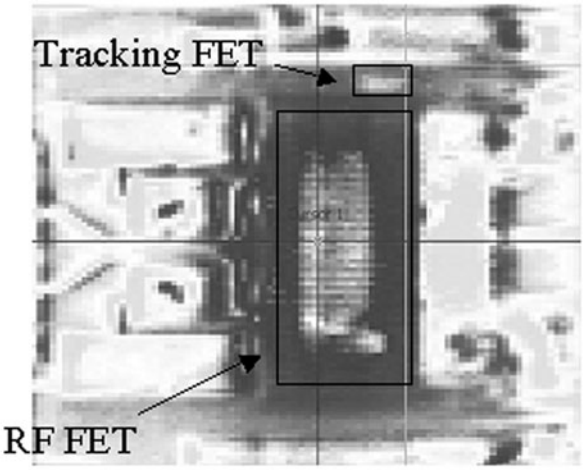

Figure 5. Infrared Picture

When a constant current source is applied to V_G, the thermal tracking FET draws a constant current I_G; when the temperature varies, the voltage V_{GS} varies to maintain the constant current I_G.

As a consequence, the LDMOS power FET sees a varying gate voltage, V_{GS} (from 3.6 to 3.8 Volts as shown in Figure 4) that also maintains its I_{DQ} constant with temperature. The tracking FET acts as a mirror of the RF FET. Consequently, the thermal tracking is independent of the quiescent current and the temperature.

When a constant voltage source V_G is applied, the voltage is set on the thermal tracking transistor, and its current varies with a change in temperature. Therefore, the thermal tracking is disabled.

Note that the ratio I_{DQ}/I_G is set by design; it reflects the size of the two transistors: RF FET gate periphery and tracking FET gate periphery.

The RF FET is biased at V_{DS} = 26 to 28 Volts while the tracking FET is biased around V_{DS} = 3 to 4 Volts, depending on the quiescent current needed. Although the two FETs are biased in different conditions, the I_{DS} versus V_{GS} curves behave almost identically over temperature under nominal conditions of operation. In other words, the thermal coefficient remains constant for V_{DS} = 3.5 to 4 Volts and 26 to 28 Volts and for a given I_{DQ}.

During operation, the RF FET is biased at 26 Volts and in Class AB while the tracking FET is biased at V_{DS} = 3 to 4 Volts. Therefore, the power dissipation is significantly different; consequently, the two die are not at the same temperature (see Figure 5).

Under DC conditions, the temperature difference can be significant. RF FET is at a higher temperature than its associated thermal tracking FET, and the ratio I_{DQ}/I_G is higher than the theory.

CIRCUIT CHARACTERIZATION

As described earlier, a current source is needed to power on the thermal tracking. There are several ways to supply a constant current source.

The simplest way to realize a current source is to implement a resistor R_G in series in the gate bias circuit. The quiescent current is measured and adjusted by varying V_G (see Figure 6). Depending on the IC and desired I_{DQ}, the gate draws a current up to 5 mA.

For a better understanding of the thermal tracking constant current behavior, the following example is presented. This example uses a 2-stage 900 MHz IC (the MHVIC915) that is characterized over temperature for two different values of R_{GATE}. (R_{GATE} = 4.51 kOhm and R_{GATE} = 1 kOhm)

Tables 1 and 2 show the different DC voltage and DC current readings versus temperature for the second stage in this IC.

In this example, over a 100 degree range, the gate current varies about 5% with a 4.5 kOhm resistor and about 21% with a 1 kOhm resistor. This variation induces a variation of 8% on the I_{DQ} of the power stage in the first case and 25% in the second case.

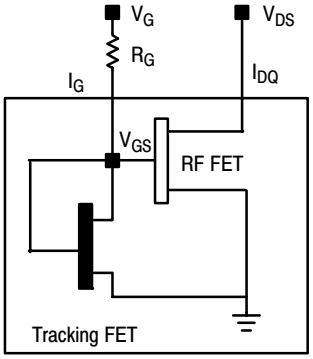

Figure 6. Thermal Tracking Schematic with Its Bias Circuit

Table 1. I_{DQ}/I_G versus Temperature (R_G = 4.51 kOhm)

Temp	V_G (V)	V_{GS2} (V)	I_{G2} (mA)	I_{DQ2} (mA)	R_G (kOhm)
100	8.55	3.75	1.023	266	4.51
90	8.55	3.77	1.018	264	4.51
80	8.55	3.79	1.013	262	4.51
70	8.55	3.81	1.008	260	4.51
60	8.55	3.83	1.003	258	4.51
50	8.55	3.85	0.998	256	4.51
40	8.55	3.87	0.993	254	4.51
30	8.55	3.89	0.988	252	4.51
20	8.55	3.91	0.983	250	4.51
10	8.55	3.93	0.978	248	4.51
0	8.55	3.95	0.974	246	4.51
-10	8.55	3.97	0.966	243	4.51
-20	8.55	3.99	0.962	241	4.51
-30	8.55	4.01	0.958	240	4.51
-40	8.55	4.03	0.953	238	4.51

Table 2. I_{DQ}/I_G versus Temperature (R_G = 988 Ohm)

Temp	V_G (V)	V_{GS2} (V)	I_{G2} (mA)	I_{DQ2} (mA)	R_G (Ohm)
100	4.89	3.65	1.168	294	988
90	4.89	3.68	1.147	289	988
80	4.89	3.71	1.126	283	988
70	4.89	3.74	1.105	278	988
60	4.89	3.77	1.084	272	988
50	4.89	3.8	1.063	267	988
40	4.89	3.83	1.042	261	988
30	4.89	3.86	1.021	256	988
20	4.89	3.89	1	250	988
10	4.89	3.92	0.967	242	988
0	4.89	3.95	0.95	235	988
-10	4.89	3.97	0.93	233	988
-20	4.89	3.99	0.912	228	988
-30	4.89	4.01	0.894	224	988
-40	4.89	4.01	0.874	217	988

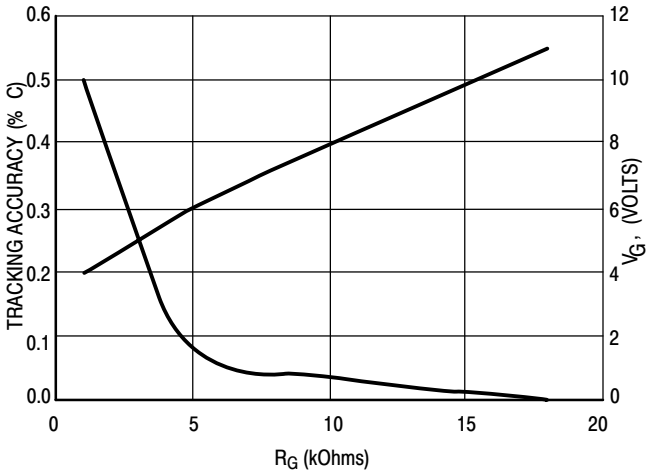

Figure 7. Tracking Accuracy and V_G versus R_G

The explanation for 5% variation instead of 21% is quite simple. Consider that, due to an external phenomenon (increasing temperature for instance), the I_G current increases. As V_G is fixed by the supply, the drop through the R_{GATE} resistor also increases. This, in turn, means that V_G decreases ($V_{GS} = V_G - R_{GATE} I_G$), thus forcing less current through the tracking FET. This compensates for the initial I_G increase imagined.

This current regulating effect is even more pronounced if the value of R_G is high. Ideally, an infinite value resistor would yield a 0% variation in I_G and, therefore, a 0% variation in the corresponding stage quiescent current.

On the opposite end, no resistor (or a 0 Ohm resistor) has no regulating effect, and the thermal tracking is disabled.

Also note that the resistor temperature variation during the experiment is negligible (less than 0.1%)

Finally, from Tables 1 and 2, note that there is a higher voltage drop through the 4.51 kOhm than through the 1 kOhm resistor. This implies the availability of a higher voltage source to better control the quiescent current.

In summary, the constant current regulation is better with a higher value gate resistor, but care is needed to be able to supply the corresponding V_G voltage (see Figure 7).

A better way to set the quiescent current would be as follows: The ratio I_{DQ}/I_G is defined by design so gate current

could be used to set individual stage I_{DQ}'s independently from the part-to-part variation, assuming that everything is perfect.

Table 3 presents the result of a characterization of four different lots. A constant gate current (1.6 mA) has been applied to Stage 3 of MW4IC2020, and the quiescent current is measured. This table shows that with a quite good control of I_G (1.5% variation), the variation of I_{DQ} is in the range of 10%. So gate current should not be used to set the individual stage I_{DQ}'s with good accuracy.

Table 3. I_{DQ} versus I_G

	I_{G3}	I_{DQ3}
Mean value (mA)	1.596	204
(Max-Min)/Mean (%)	1.56	9.4

The variation of I_{DQ}/I_G from part to part is because the tracking FET is very small compared to the RF FET so it is more sensitive to the process variation while the RF FET DC characteristic is an average of a large amount of transistor fingers in parallel.

Table 4 presents stage by stage the theoretical ratio RF gate periphery/tracking FET gate periphery.

Table 4. Ratio of RF FET Size Relative to RF Tracking FET

	Stage 1	Stage 2	
MWIC930	100	400	
MW4IC915	100	200	
MHVIC915	50	200	
	Stage 1	**Stage 2**	**Stage 3**
MW4IC2020	20	42	100
MW4IC2230	20	42	100
MHVIC2115	50	100	200

Also, the tracking does not compensate for the HCI (Hot Carrier Injection) that induces I_{DQ} drift of the power LDMOS. This is because the tracking FET sees a drain voltage of about 4 Volts, which induces negligible HCI. The drain voltage of the power LDMOS is generally comprised between 26 Volts and 32 Volts that induces a certain amount of HCI. If the tracking FET had the same drain voltage as the power FET, HCI tracking would occur in the same manner as thermal tracking.

LINEARITY PERFORMANCE

The following set of experiments using the MW4IC2020MB show the RF performances over temperature when the thermal tracking is turned on.

First, the device is evaluated with one tone. AM/AM and linearity performance have been conducted for three temperatures. The bias circuit is made with series resistors R_G > 1.5 kOhms and a voltage power supply. This configuration yields ±3% quiescent current accuracy over 150°C. The device is biased at 26 Volts, and I_{DQ1} = 80 mA, I_{DQ2} = 200 mA, I_{DQ3} = 300 mA. Measurement frequency is 1.96 GHz, and tone spacing is 100 kHz for the third order IMD and GSM EDGE signal for the EVM graph.

Figures 8 and 9 present the AM/AM and AM/PM versus case temperature. As expected, the shape of the curves are maintained over a large dynamic range. Also, the power capability is degraded due to temperature effect as well as gain.

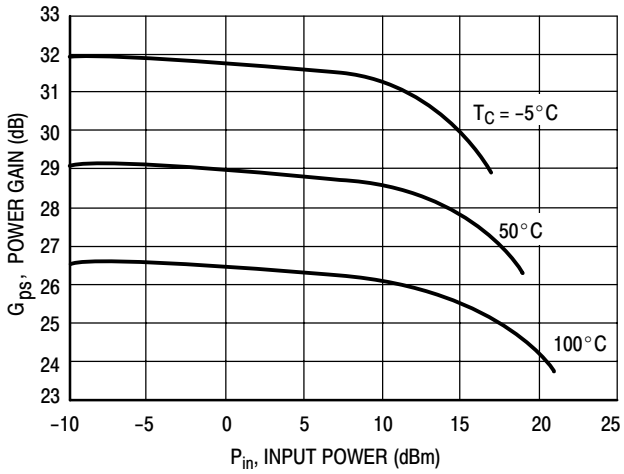

Figure 8. AM/AM versus Temperature

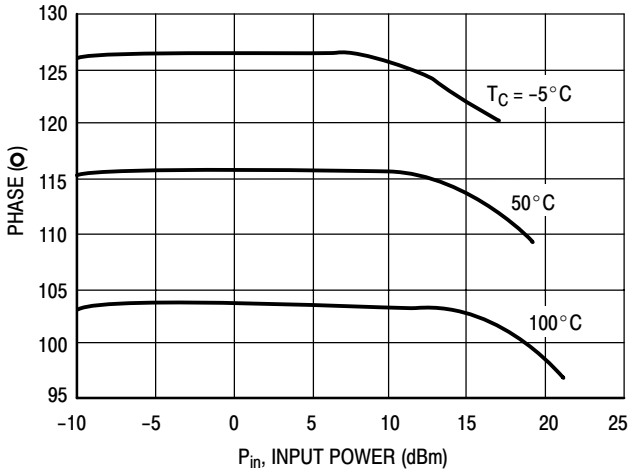

Figure 9. AM/PM versus Temperature

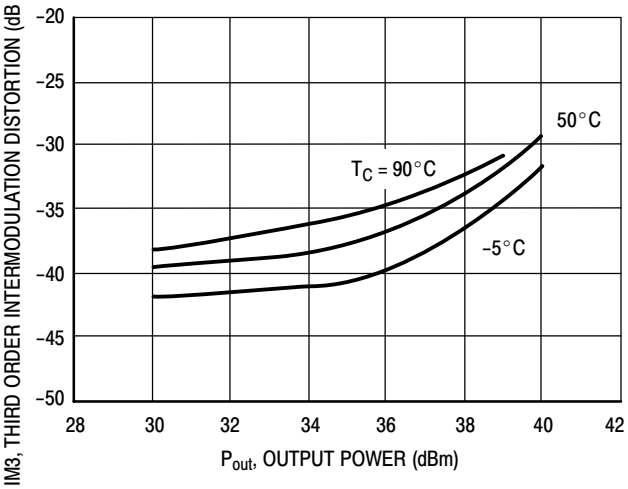

Figure 10. Third Order Intermodulation Distortion versus Output Power

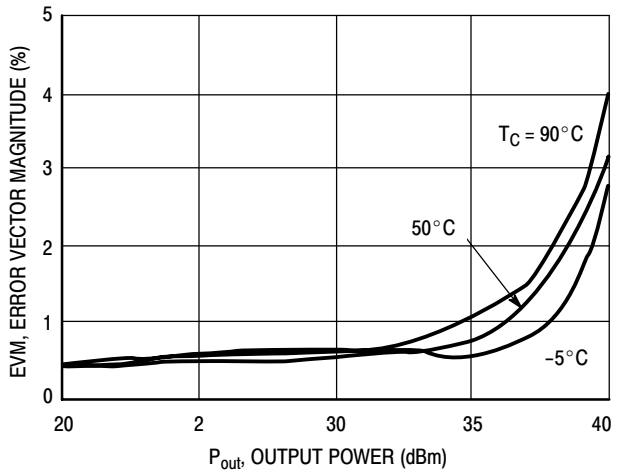

Figure 11. Error Vector Magnitude versus Output Power

Figures 10 and 11 present two-tone CW and EDGE performance.

Note the degradation of the power capability of the device when the temperature is increased. Taking into account this effect, the linearity behavior is maintained.

CONCLUSION

Freescale's new RF power integrated circuits integrate a thermal tracking device that keeps the I_{DQ} constant for all stages versus temperature variations.

This application note explored the working mechanism of this thermal tracking as well as its performance. Explained was how with careful resistive loading of the gate bias, I_{DQ} variations of less than 5% over 100 degrees can be easily obtained. Also described was how to disable the thermal tracking by running a voltage source to the gate bias.

Finally, it showed the RF performance with temperature when the thermal tracking is enabled. As expected, the shape of the different RF parameters remained unchanged over a large dynamic range.

The integrated I_{DQ} thermal tracking FET is a very useful feature that allows the necessary thermal compensation to be suppressed at the board level.

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