



# PowerQUICC® III Processor with TDM, DDR, PCI, PCI Express®, RapidIO, 1 GB Ethernet, Security, CPM with UTOPIA

## MPC8560

### Not Recommended for New Designs

This page contains information on a product that is not recommended for new designs.

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The PowerQUICC® III is a versatile one-chip integrated microprocessor and peripheral combination that can be used in a variety of controller applications, excelling particularly in communications and networking products. Our PowerQUICC III processor family is the next generation of integrated communications processors. The PowerQUICC III provides higher performance in all areas of device operation, including greater flexibility, extended capabilities, and higher integration.

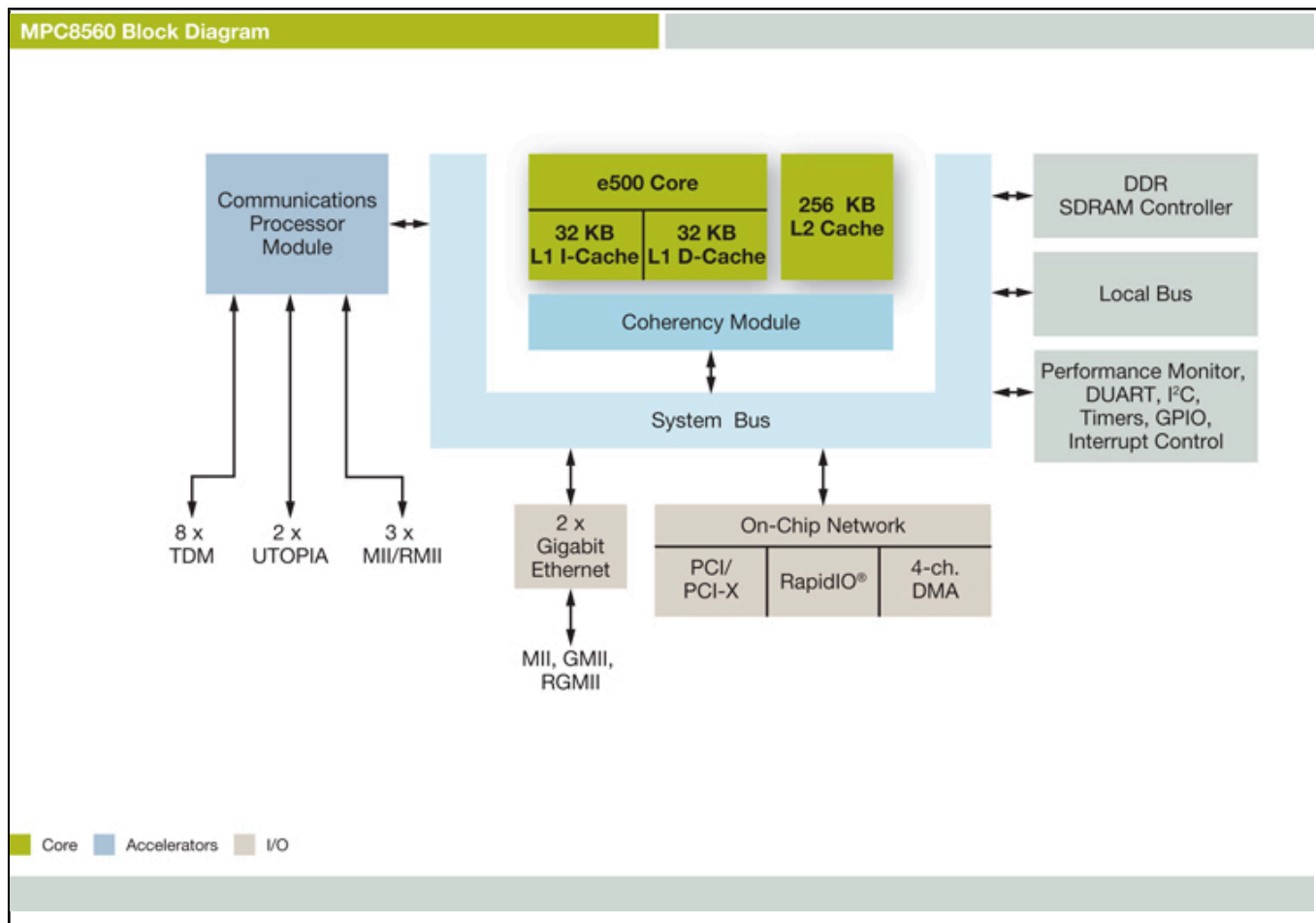
Our leading PowerQUICC III architecture integrates two processing blocks. One block is a high-performance embedded e500 core. With 256 KB of level 2 cache, the e500 core is built on Power Architecture® technology and provides unprecedented levels of hardware and software debugging support. The second block is the communications processor module (CPM). The CPM of the PowerQUICC III can support three fast serial communications controllers (FCCs), two multichannel controllers (MCCs), four serial communications controllers (SCCs), one serial peripheral interface (SPI) and one I<sup>2</sup>C interface.

The PowerQUICC III also offers two integrated 10/100/1000 Ethernet controllers, a DDR SDRAM memory controller, a 64-bit PCI-X/PCI controller, and a RapidIO® interconnect. This high level of integration helps simplify board design and offers significant bandwidth and performance for high-end control-plane and data-plane applications.

Contact your local [NXP Sales Office](#) or [NXP Authorized Distributor](#).



# Freescale PowerQUICC MPC8560 Communications Processor Block Diagram Block Diagram



View additional information for [PowerQUICC<sup>®</sup> III Processor with TDM, DDR, PCI, PCIx Express<sup>®</sup>, RapidIO, 1 GB Ethernet, Security, CPM with UTOPIA.](#)

**Note:** The information on this document is subject to change without notice.

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