# AN10571

## Sleep programming for NXP bridge ICs

**Rev. 01 — 5 January 2007** **Application note**

### Document information

| Info | Content |
|---|---|
| **Keywords** | SC16IS750, Bridge IC, Sleep programming |
| **Abstract** | The sleep programming of NXP Bridge ICs such as SC16IS750 ($I^2C$-bus/SPI to single UART) is discussed in this application note. The conditions of sleep and wake-up are described. In addition, a sample code for sleep programming is provided. This application note is also applicable to other bridge ICs such as SC16IS740, SC16IS760, SC16IS752, and SC16IS762. |

founded by Philips

### Revision history

| Rev | Date | Description |
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| 01 | 20070105 | Application note; initial version. |

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# 1. Introduction

The NXP Bridge IC is a new generation of interface solutions for managing high-speed serial data communication among various bus interfaces such as SPI, $I^2C$-bus, and UART including RS-232 and RS-485. The Bridge IC is commonly used to overcome the limitation of the host bus interface to peripherals and provides easy to interface with existing different serial buses interface.

The Bridge IC features a Sleep mode that can reduce the current consumption by putting the Bridge IC into sleep when there is no activity on the bus. The Sleep mode programming described in Section 2 shows how a microcontroller or an embedded processor programs the Bridge IC into sleep so users can quickly understand the implementation of NXP Bridge IC serial interface for RS-232 point-point communication. The goal is to help users to design the Bridge IC in their applications, especially battery-operated applications, and also shorten their product development cycle.

# 2. Sleep mode programming

## 2.1 Programming Sleep mode

- Enabling the Sleep mode must happen after the divisor latches, DLL and DLH, have been programmed because the DLL or DLH can only be written before the Sleep mode is enabled (IER[4] = 1). Therefore, it is advisable to disable the Sleep mode (IER[4] = 0) before writing to DLL or DLH registers.
- To enable the Sleep mode feature, bit 4 of the Enhanced Register Set (EFR) must be set prior to setting bit 4 of Interrupt Enable Register (IER) as follows:

```
// Sample code
void SC16IS750_init (void) {
    writeRegister (LCR, 0x80);     // access program baud rate
    writeRegister (DLL, 0x08);     // baud rate low byte set to 115.2 Kbaud
                                   // with X1 = 14.456 MHz
    writeRegister (DLM, 0x00);     // program baud rate high byte
    writeRegister (LCR, 0XBF);     // access enhanced register
    writeRegister (EFR, 0X10);     // enable enhanced functions
    writeRegister (LCR, 0x03);     // set 8 data bit, 1 stop bit, no parity
    writeRegister (FCR, 0x07);     // reset TXFIFO, reset RXFIFO,
                                   // and enable FIFO mode
    writeRegister (IER, 0x11);     // enable sleep mode and receive
                                   // data interrupt
}
```



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### 2.2 Sleep mode conditions

All of the following conditions must be satisfied for the UART to enter the sleep mode:

- The receiver data input lines must be idling at logic 1 (HIGH state).
- The transmitter FIFO and transmitter shift register must be empty.
- There are no interrupts pending for UART channels (ISR[0] = 1) except THR and Time-out interrupts.
- There is no data in the receiver FIFO.
- No change of state on any of the modem input pins ($\overline{RI}$, $\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$) or general-purpose serial inputs.
- Reading Modem Status Register bit 0 to bit 3 (MSR[3:0]) should be logic 0.

### 2.3 UART clock and baud rate clock stopped in Sleep mode

In Sleep mode, the UART clock and baud rate clock are stopped and XTAL2 is floating. Since most registers are using these clocks, the current consumption is greatly reduced.

### 2.4 Wake-up condition from the Sleep mode

- A receive data start bit transition from logic 1 to logic 0.
- A change of state on any of the modem input pins ($\overline{RI}$, $\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}$) or general-purpose serial inputs.
- A data byte is written to the transmitter FIFO.

If the UART is awakened by one of the conditions described above, it will return to the Sleep mode automatically after the last character is transmitted or read by the host processor. The UART will stay in Sleep mode until setting IER[4] to logic 0 disables it.

The inputs must remain steady at $V_{DD}$ or $V_{SS}$ (ground) state to minimize the sleep current. The inputs are address, data, read, write, chip selects, and all modem inputs. Also, the UART receiver inputs must idle at logic 1 state while at sleep. Floating inputs may result in sleep currents in the mA range. Also, the sleep current might be higher if there is any activity on the UART data bus during Sleep mode.

## 3. Conclusion

The NXP Bridge IC provides easy interface to microcontrollers or embedded processors and enables seamless high-speed SPI or Fast $I^2C$-bus to RS-232 or RS-485 protocols convergence including GPIO for general-purpose input/output and IrDA for wireless data links. Also, the Bridge IC offers low voltage operation, low current consumption, and compact design in very small packages, which is suitable for battery-operated applications. In addition, the Bridge IC reduces software overhead, frees up the host controller's resources, increases design flexibility, and improves overall system performance. For more details about the Bridge ICs, please visit our website at http://www.NXP.com/interface to download the data sheets.



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# 4. Abbreviations

**Table 1. Abbreviations**

| Acronym | Description |
|---|---|
| FIFO | First In, First Out |
| GPIO | General-Purpose Input/Output |
| $I^2C$-bus | Inter-Integrated Circuit bus |
| IC | Integrated Circuit |
| IrDA | Infrared Data Association |
| SPI | Serial Peripheral Interface |
| THR | Transmit Holding Register |
| UART | Universal Asynchronous Receiver Transmitter |



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