AN11031

PCB layout and ADC circuit recommendations for LPC1100 and LPC1300

Rev. 1 — 4 February 2011

Application note

Revision history

Rev	Date	Description
1	20110204	Initial version.

Contact information

For more information, please visit: http://www.nxp.com

For sales office addresses, please send an email to: salesaddresses@nxp.com

AN11031

Application note

Rev. 1 — 4 February 2011 **2 of 15**

1. Introduction

The LPC1100 is based on the ARM Cortex M0, and the LPC1300 family is based on the ARM Cortex M3 core. Both families include an 8 channel 10-bit successive approximation Analog-to-Digital Converter (ADC) with a maximum conversion rate of 400 kHz.

The ADCs of the LPC1100 and LPC1300 differ from other LPC devices in that they do not have an external Vref[1]. This means that extra precautions have to be taken to minimize noise effects that can affect the conversion results.

The goal of this Application Note is to show how to develop a printed circuit board (PCB) that is optimized for the ADC on the LPC1100 and LPC1300 families.

This application note is intended as a guideline for hardware and/or PCB designers with basic PCB design knowledge, with the intent of suggesting methods to prevent potential electromagnetic interference (EMI) and electromagnetic compatibility (EMC) problems.

Unlike many other design issues, EMC is not an area where it is possible to list a set of rules. In general, EMC compliance cannot be guaranteed by design; it has to be tested. That is why this application note includes a test software routine to compare and quantify the difference between a basic and an optimized design.

---

[1] Vref = reference voltage source

2. PCB Optimizations of the ADC

The microcontrollers in the LPC1100 and LPC1300 families are all equipped with a single external power supply. The digital (core) and analog parts (ADC/V_{ref}) are all connected to the same external supply. Without precautions, noise produced by the core could influence the readout of the ADC via the internal V_{ref}.

Inside the devices, some measures are taken to reduce the noise on the ADC unit. For example, having an extra set of bonding wires and a separate isolated internal regulator reduces the noise transfer from the core to the ADC. To shield the ADC lines, decoupling capacitors are added. In Fig 1 a schematic wire interconnection block diagram of the ADC and the core is shown.
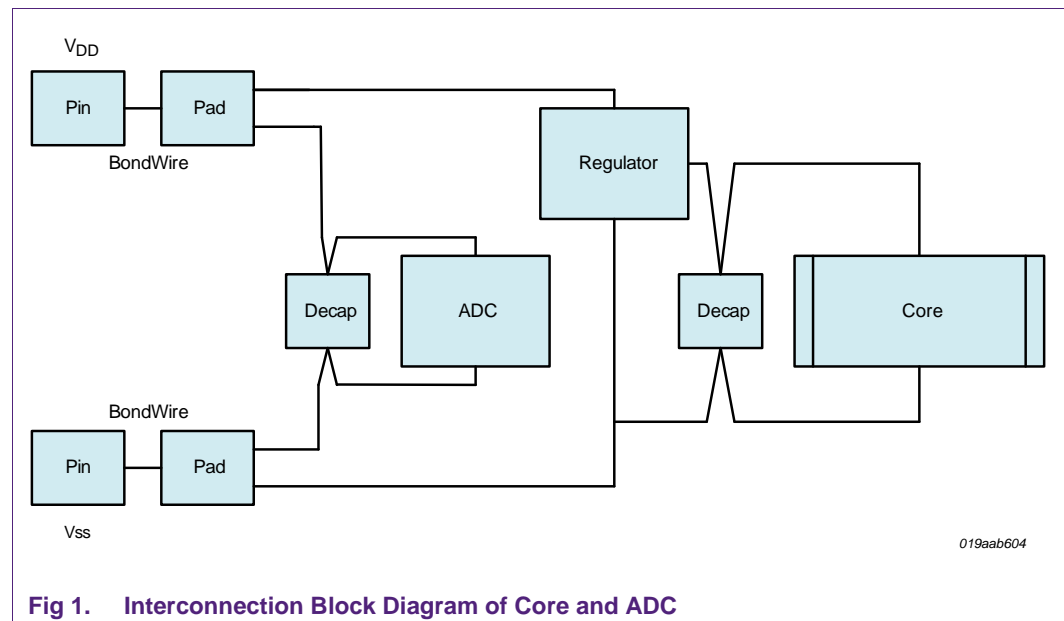

Fig 1. **Interconnection Block Diagram of Core and ADC**

The physical location of the ADC-block inside the chip is as close as possible to the ADC pins in order to reduce noise.

The LPC1100 and LPC1300 series microcontrollers are equipped with a 10-bit ADC; therefore the resolution of the ADC is V_{DD} / 1024. For example this means when V_{DD} equals 3.3V, then resolution is 3.3V / 1024 = ~3.2 mV/bit. With these low voltages noise suppression is important. To suppress noise on the V_{DD} of the device, decoupling capacitors on the PCB is very important.

2.1 Example hardware design

The following section provides some details on board layout, grounding and decoupling.

2.1.1 ADC pin out

First step is to make an electrical design. If one does not need all the ADC-channels, the required channels can be selected in a manner so as to reduce crosstalk from the digital domain. See the user manual for the physical pin-out. In the example shown all the channels are wired.
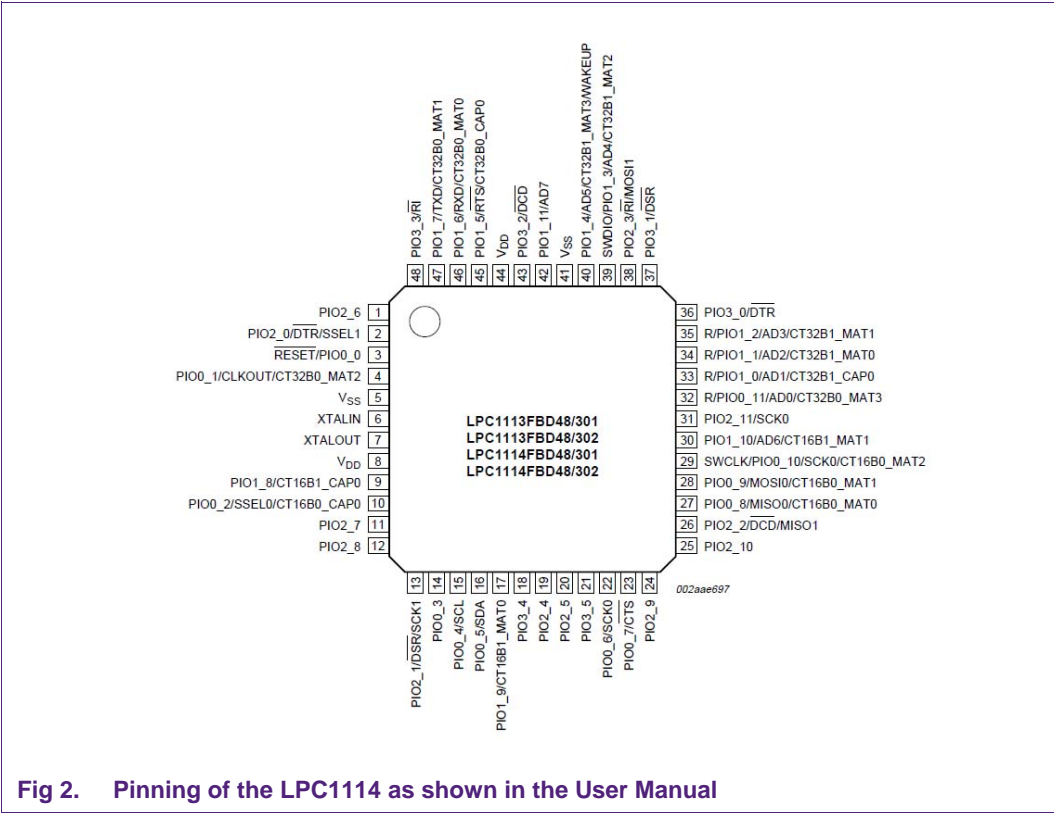
Top pins (left to right): PIO3_3/RI [48], PIO1_7/TXD/CT32B0_MAT1 [47], PIO1_6/RXD/CT32B0_MAT0 [46], PIO1_5/RTS/CT32B0_CAP0 [45], V_{DD} [44], PIO3_2/DCD [43], PIO1_11/AD7 [42], V_{SS} [41], PIO1_4/AD5/CT32B1_MAT3/WAKEUP [40], SWDIO/PIO1_3/AD4/CT32B1_MAT2 [39], PIO2_3/RI/MOSI1 [38], PIO3_1/DSR [37]

Left pins (top to bottom): PIO2_6 [1], PIO2_0/DTR/SSEL1 [2], RESET/PIO0_0 [3], PIO0_1/CLKOUT/CT32B0_MAT2 [4], V_{SS} [5], XTALIN [6], XTALOUT [7], V_{DD} [8], PIO1_8/CT16B1_CAP0 [9], PIO0_2/SSEL0/CT16B0_CAP0 [10], PIO2_7 [11], PIO2_8 [12]

Center label:
LPC1113FBD48/301
LPC1113FBD48/302
LPC1114FBD48/301
LPC1114FBD48/302

Right pins (top to bottom): PIO3_0/DTR [36], R/PIO1_2/AD3/CT32B1_MAT1 [35], R/PIO1_1/AD2/CT32B1_MAT0 [34], R/PIO1_0/AD1/CT32B1_CAP0 [33], R/PIO0_11/AD0/CT32B0_MAT3 [32], PIO2_11/SCK0 [31], PIO1_10/AD6/CT16B1_MAT1 [30], SWCLK/PIO0_10/SCK0/CT16B0_MAT2 [29], PIO0_9/MOSI0/CT16B0_MAT1 [28], PIO0_8/MISO0/CT16B0_MAT0 [27], PIO2_2/DCD/MISO1 [26], PIO2_10 [25]

Bottom pins (left to right): PIO2_1/DSR/SCK1 [13], PIO0_3 [14], PIO0_4/SCL [15], PIO0_5/SDA [16], PIO1_9/CT16B1_MAT0 [17], PIO3_4 [18], PIO2_4 [19], PIO2_5 [20], PIO3_5 [21], PIO0_6/SCK0 [22], PIO0_7/CTS [23], PIO2_9 [24]

002aae697

Fig 2. **Pinning of the LPC1114 as shown in the User Manual**

Observe that all the ADC-channels are situated relatively close to each other (see pins 30, 32 … 35, 39, 40 and 42). Since some digital signal lines are located in between the analog pin, it is recommended avoid them when possible. Doing so reduces the amount of crosstalk transferred onto the ADC block.

AN11031

Application note **Rev. 1 — 4 February 2011** **5 of 15**

Fig 3. Electrical design with locations where extra precautions have to be taken for shielding (see: dashed lines)

2.1.2 Separate or isolate ground planes

The analog and the digital domains are separated inside the chip; however, they are linked to the same power pins. Therefore, noise on the power and ground lines should be reduced as much as possible. Major noise sources are the Oscillator, CPU core, system PLL, Clock-Tree and General Purpose IO-Ports. A decrease of noise can be achieved by segmenting the ground plane into the digital and analog domains. These planes are physically separated by a small gap and connected only at one point that is a few millimeters in size.

Fig 4 depicts the main (digital) ground plane 'A', the sub ground (analog) planes 'B', 'C' (with ADC-filters), and sub ground plane 'E' (Crystal-circuitry).

By creating an analog sub ground plane with only one entrance 'F'; local ground currents are restricted to travel through this gap. Confining these analog ground currents to this gap prevents other currents entering the analog sub plane and interfering with ADC conversions.

Although the quartz oscillator is not a big source of emissions, it may be susceptible to noise; therefore, special care must be taken when routing the PCB's oscillator section.

One can place a guard ring with capacitors around the quartz oscillator circuit for additional emission isolation. When possible, avoid close proximity between clocks and analog traces. See section 'E' in Fig 4.

The CPU core, system PLL and Clock-Tree are responsible for noise on the power lanes. When using one or more clock dividers, low frequency harmonics are to be expected. The noise contribution of General Purpose IO-pins cannot be generally estimated as it depends on the user pin configuration. If a GPIO is toggled frequently, it may also create additional noise. By keeping digital pin toggling to a minimum, it may be possible to reduce noise emissions.

The noise emissions from GPIO pins are due to their narrow band character. One could expect such emissions in system clock drivers or CAN data lines.

2.1.3 Decouple the supply system

A power supply system consists of one or more power pins and their related ground pins. The LPC1100 and LPC1300 are equipped with two supply pins i.e. two V_{DD} and V_{SS} pins. At least one decoupling capacitor for each power supply system is needed to ensure low impedance over a wide frequency range. In this design two capacitors are placed as close as possible to the power pins of the microcontroller.

In Fig 4 the capacitors are indicated by the letters 'G' and 'H'. For improved decoupling, two vias are used to connect the capacitor to the ground plane.
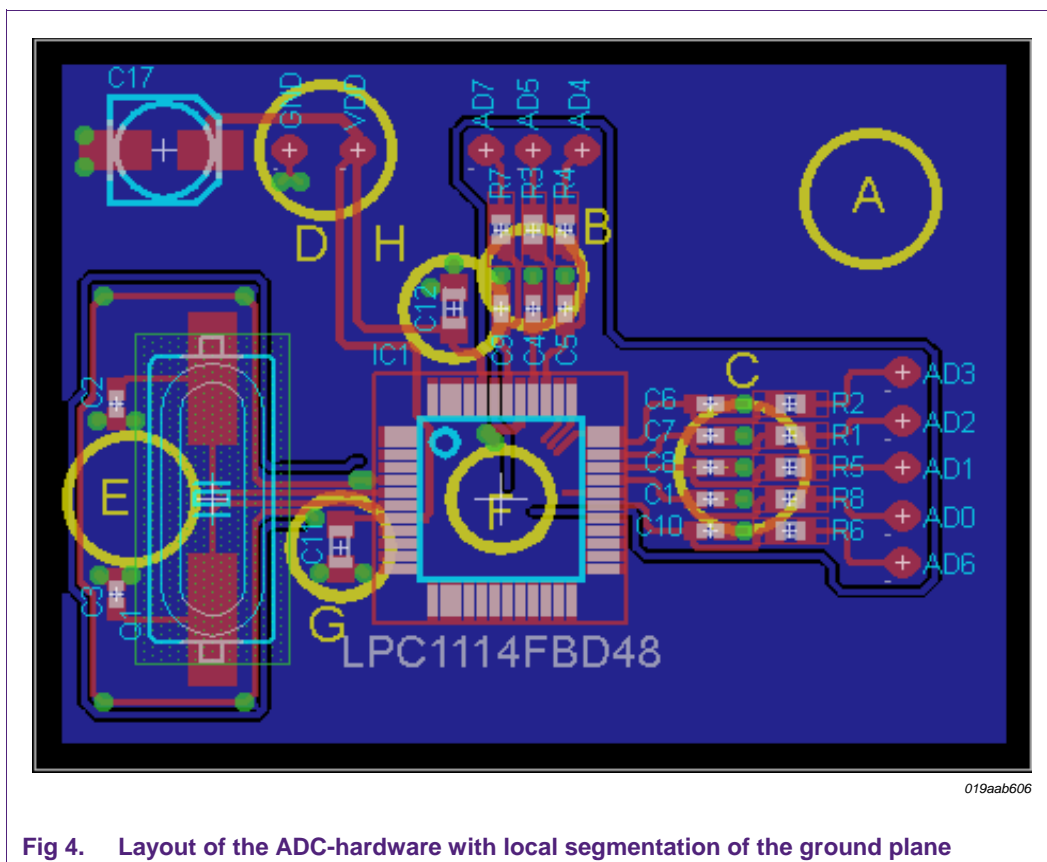
019aab606

Fig 4.   Layout of the ADC-hardware with local segmentation of the ground plane

Any active element inside a microcontroller has direct or indirect connections to the power supply system; thus, any switching inside the microcontroller will cause current to flow. The noise from this current loop is proportional to the area of the loop(s) in which the current flows; therefore, it's necessary to design these loops as small as possible. One such loop is the current loop between the microcontroller and the decoupling capacitors. A power supply has an impedance greater than 0 Ohm. Particularly at higher frequencies the inductive wire impedance of the power supply becomes more significant. Pulsed currents overlay a ripple voltage to the DC power supply that contributes to noise emissions.

By using thicker traces to the microcontroller's power supply its inductive impedance is lowered, thus effectively reducing noise emissions. Due to the power line emissions, it is suggested to separate power lines from signal lines to decrease crosstalk.

Use electrolytic capacitors in the vicinity of the PCB's power source input (shown left side of 'D') and ceramic capacitors next to the power pins of the microcontroller. Input filters connected to the ADC will have a significant impact on the noise immunity of the analog parts. The type of the filters to be used depends on the input signal frequency. The location of the filter's capacitors is also very important. It's recommended to place the filter capacitors onto the same (analog) sub ground plane as shown in Fig 4.

When possible, separate analog traces from digital traces; for example one could use extra grounded traces. Keep digital pins away from analog pins when physically possible. When that is not possible, try to use extra shielding between digital and the analog tracks.

3. Test software for optimizing the hardware of the ADC

Testing the noise immunity of a design is very important. This can be done by using a small software program, which gives a numerical indication of the stability of the ADC conversion results. The test software was developed using the NXP's LPCXpresso IDE:

http://ics.nxp.com/support/lpcxpresso/

To determine how relatively stable the ADC design is, 1,000,000 ADC measurements are taken of a known voltage. Of those measurements, the most stable result is within a 1 to 2 LSBs of the expected ADC conversion.

For example if V_{DD} equals 3.3 V and AD7 equals 1.6 V: The readout should be in between 496 and 497 (decimal).

3.1 Gauging the ADC conversion results

Generating a histogram for a series of ADC readings can be done using the following two pass process:

1. Connect the LPCXpresso board to the workstation and apply an external 1.6 V voltage to P1.11 (AD7).

2. "Build all projects" and Debug the "adc" project to execute he software.

3. During the first pass the software performs 1,000,000 measurements in order to calculate the average. This average is used to determine the ADC conversion values' approximate location on a histogram. It essentially "zooms in" into the area of interest.

4. The second pass takes another 1,000,000 measurements and increments the bins that correspond to the individual readings between [avg - 15] to [avg + 15]. This will populate the array with the histogram's data.

5. Export the data to a PC to visualize the results. The application example allows a "copy and paste" of the data into a spreadsheet program to plot a scatter chart.

The histogram gives a graphical representation of distribution of ADC conversions. Running this application could be useful if changes on the electronic design were performed; for example by adding extra filtering, relocating traces, or changing decoupling capacitors.

Ideally, a good set of ADC conversions would result a histogram with a very narrow distribution of samples; meaning that the ADC sampling would have a higher precision.

Fig 5 shows three sets of sample data. ADC data sets D1 and D2 are suffering from noise interference while column D3 shows a set where ADC layout was optimized. Notice that data set D3 has a very narrow distribution set.
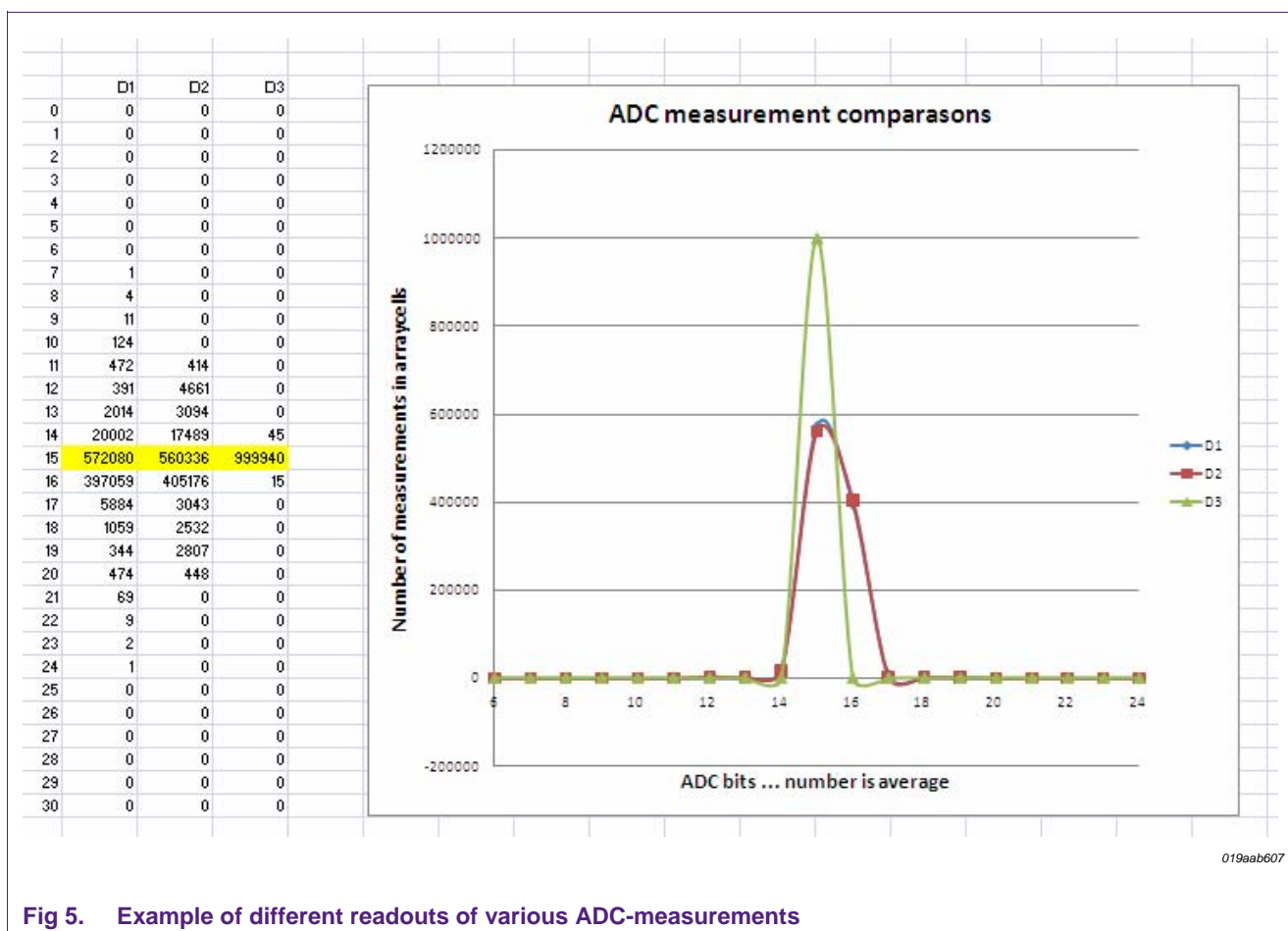
AN11031

Application note **Rev. 1 — 4 February 2011** **9 of 15**

	D1	D2	D3
0	0	0	0
1	0	0	0
2	0	0	0
3	0	0	0
4	0	0	0
5	0	0	0
6	0	0	0
7	1	0	0
8	4	0	0
9	11	0	0
10	124	0	0
11	472	414	0
12	391	4661	0
13	2014	3094	0
14	20002	17489	45
15	572080	560336	999940
16	397059	405176	15
17	5884	3043	0
18	1059	2532	0
19	344	2807	0
20	474	448	0
21	69	0	0
22	9	0	0
23	2	0	0
24	1	0	0
25	0	0	0
26	0	0	0
27	0	0	0
28	0	0	0
29	0	0	0
30	0	0	0

Fig 5. Example of different readouts of various ADC-measurements

3.2 Software example

As mentioned earlier, this sample application takes 1,000,000 measurements and stores histogram distribution into the cnt_adc_val[31] array. The center of the histogram is located at cnt_adc_val[15], which corresponds to the histogram's bin at which the software determined the ADC conversion to be equal to the previously calculated average.

For example if the calculated average value from the first iteration of 1,000,000 samples equal 510. Then cnt_adc_val[15] will contain a count value of how many times out of the second iteration of 1,000,000 samples the ADC has again measured 510.

By storing the distribution in this manner, it implies that the remainder of the cnt_adc_val[] array is used to store the frequency count where the ADC has measured 509 (cnt_adc_val[14]), 511 (cnt_adc_val[16]), and etc…

This pattern is repeated for the entire array, essentially allowing us to collect a histogram focusing on the "area of interest" (which is nearby the expected average value).

```
// actual calculations -> result 30 counter-values
for (j=0;j<1000000;j++)
{
    ADCRead( 7 );                  // ADC conversion
    while ( !ADCIntDone );         // wait till conversion is done
    ADCIntDone = 0;
    temp_ADC7 = ADCValue[7];       // put ADC-value in temp-var
    // value should be > 0.048 V and < 3.248 V
    if ((temp_ADC7 > 15) && (temp_ADC7 < 1023 - 15))
    {
        if (j%100000==0)  UARTSend( (uint8_t *)("."), 1 );

        if (temp_ADC7 < (sum_avg - 15))  cnt_adc_val[0]++;
        if (temp_ADC7 > (sum_avg + 15))  cnt_adc_val[30]++;
        if ((temp_ADC7 >= (sum_avg - 15)) && (temp_ADC7 <= (sum_avg + 15)))
        {
            cnt_adc_val[temp_ADC7 - sum_avg + 15]++;
        }
    }
}
```

019aab608

Fig 6.   Software excerpt where the histogram distribution is calculated

019aab609

Fig 7.   Sample console output (using the LPCXpresso debugger)

4. Conclusion

Designing a system using a 10-bit ADC with a single power supply will face issues unless noise cancellation techniques are applied in the PCB design. The PCB's trace layout should follow the guidelines as suggested throughout this application note. This will help to keep noise interface to a minimum, particularly while an ADC conversion is in progress.
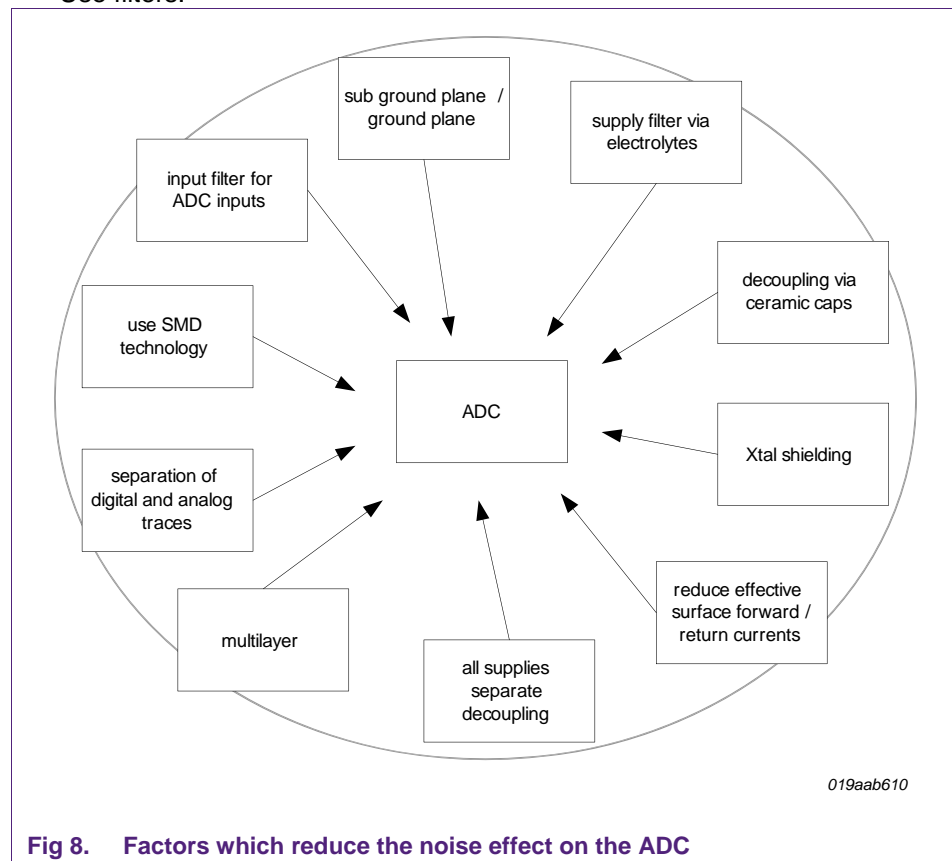
Some of these techniques include separating the ground planes, adding filters, keeping forward and return loops as small as possible, and strategically placing decoupling capacitors at close as possible to the supply pins.

The included application software is a simple and quick method to give a visual check on how noise can affect the ADC input's signal quality. The ideal histogram pattern shows a narrow distribution pattern indicating the ADC's ability to make precise conversions.

AN11031

Application note

Rev. 1 — 4 February 2011

12 of 15

5. Attachment: Checklist of PCB design considerations

The following is a list of items to beware of:

- In the schematic show the 'senders and receivers' of noise.
- Look at Emission: How the design may affect the environment.
- Look at Immunity: How the environment may affect the design.
- Use the lowest clock frequency required.
- Split analog and digital parts into isolated segments.
- Use multiple layers, e.g., ground plane(s) and power plane(s) instead of traces.
- Group functional components together.
- Keep the traces from the component to the ground plane as short as possible.
- Shield clock signals.
- Make power lines short and thick.
- Keep signal and return traces above/below each other.
- Place proper decoupling capacitors as close as possible to IC's and planes.
- Shield sensitive signals using ground planes or grounded tracks.
- Use filters.

Fig 8. Factors which reduce the noise effect on the ADC

6. Legal information

6.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

6.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer.

In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages.

Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

6.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are property of their respective owners.

AN11031

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2011. All rights reserved.

Application note   **Rev. 1 — 4 February 2011**   **14 of 15**

7.   Contents

Please be aware that important notices concerning this document and the product(s)
described herein, have been included in the section 'Legal information'.