AN12446

Migration Guide for RT1020 to RT1010

Rev. 1 — November 2019 Application Note

Contents

1 Introduction

This document describes the key points of the the migration from the i.MX RT1020 to i.MX RT1010 crossover processor for the embedded system development. It describes the hardware board design considerations, the software, and tools.

This document does not try to compare the advantages or disadvantages of the two silicons, as they have their own target markets. This document is for those who have developed embedded system with i.MX 1020, and decide to migrate the project to i.MX RT1010. The audience are expected to have i.MX 1020 experience and wish to start projects with i.MX RT1010.

The i.MX RT1020 expands the i.MX RT crossover processor families by providing high-performance feature set in low-cost LQFP packages, further to simplify board design and layout for customers. The i.MX RT1020 runs on the Arm® Cortex®-M7 core at 500 MHz.

The i.MX RT1010 is defined as a cost efficient crossover processor for low cost applications, where higher performance and real-time responses are critical. It is powered by a single Arm Cortex-M7 core running up to 500 MHz, which, along with a unique blend of ADC, PWM, Timers modules and I^2S interfaces, makes the i.MX RT1010 an ideal solution for IOT node, motor control, industrial and audio application. The i.MX RT1010 simplifies the board design and layout for customers. The i.MX RT1010 runs on the Arm Cortex-M7 core at 500 MHz.

2 Overview

Table 1 describes the feature differences for RT1010 and RT1020.

Table 1. Summary of feature differences for RT1010 and RT1020

Features	i.MX RT1020 [1]	i.MX RT1010
CPU core	Arm Cortex-M7 500 MHz Double Precision FPU + MPU	Arm Cortex-M7 500 MHz Single FPU + MPU
PLL	PLL2 - System PLL (528 MHz) PLL3 - USB1 PLL (480 MHz) PLL4 - Audio PLL PLL6 - ENET PLL	PLL2 - System PLL (528 MHz) PLL3 - USB1 PLL (480 MHz) PLL4 - Audio PLL PLL6 - ENET PLL
Power management	Integrated DCDC/LDO	Integrated DCDC/LDO
Cache	16 K/16 K L1 I/D-cache	**16 K/8 K** L1 I/D-cache
Internal RAM	256 KB FlexRAM(Bank0 – Bank7) (OCRAM+I/DTCM)	**128 KB** FlexRAM(Bank0 – Bank 3) (OCRAM+I/DTCM)

Table continues on the next page...

Table 1. Summary of feature differences for RT1010 and RT1020 (continued)

Serial flash I/F	Dual-channel QSPI NOR and NAND Octal flash and RAM XIP supported	**Dual-channel QSPI NOR** Octal flash and RAM XIP supported
Audio	Multi-channel I^2S × 1, SAI/I^2S × 2, SPDIF Tx/Rx, MQS	Multi-channel I^2S × 1, **SAI/I^2S × 1**, SPDIF Tx/Rx, MQS
ADC/ACMP	12-bits ADC × 2, ACMP × 4	**12-bits ADC × 1**
Timers and PWM	GPT × 2, PIT × 4, QTimer × 2, FlexPWM × 2, QuadDecoder × 2, WDOG × 3, ETM × 1	GPT × 2, **PIT × 1**, **FlexPWM × 1**, WDOG × 3, ETM × 1
Connectivity	LPUART × 8, LPSPI × 4, LPI^{2}C × 4, FlexIO × 1, FlexCAN × 2	**LPUART × 4**, **LPSPI × 2**, **LPI^{2}C × 2**, FlexIO × 1
Security	DCP, BEE, TRNG, SNVS, SJC	DCP, **OTFAD**, TRNG, SNVS, SJC
USB	USB OTG HS w/PHY × 2	**USB OTG HS w/PHY × 1**
High-speed GPIO	NA	**29 channels**
DRAM I/F	SDRAM 8/16-bit, 133 MHz	NA
External memory	8/16-bit parallel NOR flash 8/16-bit SLC NAND flash (SW ECC)	NA
eMMC/SD I/F	eMMC 4.5/SD 3.0 × 2	NA
Ethernet	10/100 with IEEE1588 × 1	NA
Boot Devices	Serial NOR flash via FlexSPI Interface Serial NAND Flash via FlexSPI Interface Parallel NOR flash with the Smart External Memory Controller (SEMC), located on CS0, 16-bit bus width. NAND Flash with SEMC interface, located on CS0, 8-bit/16-bit bus width. SD/MMC/eSD/SDXC/eMMC4.4 via uSDHC interface, supporting high capacity cards Serial NOR/EEPROM boot via LPSPI	Serial NOR flash via FlexSPI Interface

1. The i.MX RT1020 feature set varies on packages. For details, refer to the i.MX RT1020 datasheet.

3 System module

3.1 Clocks

RT1010's PLL is reused from the RT1020, which means that RT1010 can directly reuse the PLL configurations of the RT1020. However, there are modifications on CCM clock tree. Table 2 describes the CCM clock tree differences for RT1010 and RT1020. For details, refer to RT1010 and RT1020 Reference Manual.

Table 2. Summary of clock tree differences for RT1010 and RT1020

RT1010 removal	ARM_PODF DIV
	PERIPH_CLK2_PODF DIV
	USDHC1_CLK_ROOT
	USDHC2_CLK_ROOT
	SEMC_CLK_ROOT
	SAI2_CLK_ROOT
	CAN_CLK_ROOT
RT1010 add	FLEXSPI_CLK_SRC MUX
	ADC_ALT_CLK
	Pll3_sw_clk as a source for SAI1 and SAI3
RT1010 update	AHB_CLK_ROOT -> CORE_CLK_ROOT
	FlexSPI CLK source: SEMC_CLK_ROOT_PRE -> PLL2

3.2 High-speed GPIO

The RT1010 provides 29 channels of High-Speed GPIO (HSGPIO). The HSGPIO can be accessed with high frequency. The maximum toggle frequency of HSGPIO is half of the CORE, but the maximum toggle frequency of the pad is about 200 MHz. Therefore, the maximum toggle frequency of HSGPIO is about 200 MHz.

GPIO1 is the general GPIO port and GPIO2 is the HSGPIO port, as shown in Figure 1. The `IOMUXC_GPR26` register controls which port to be mapped to the pad, as shown in Figure 2.

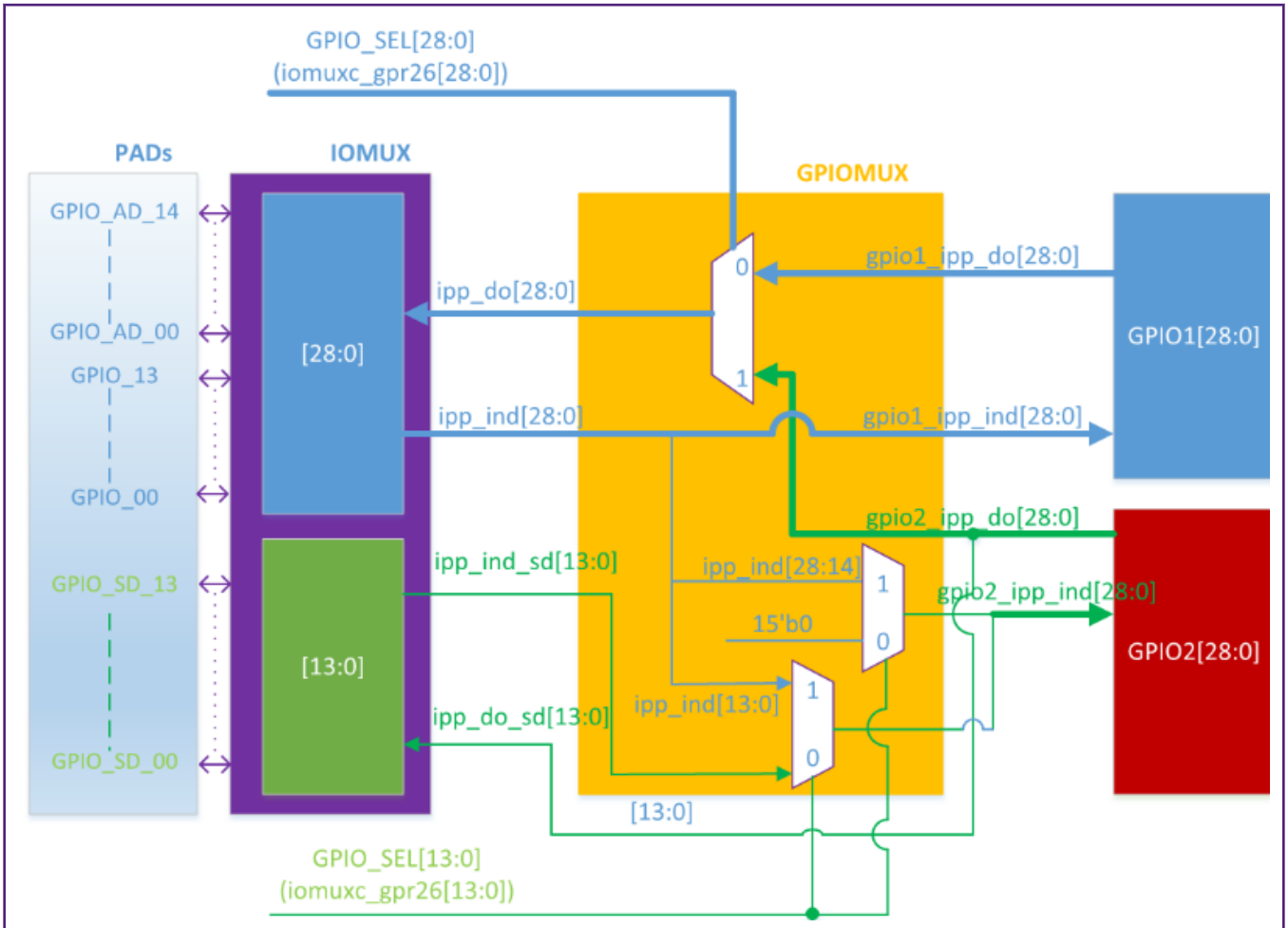

Figure 1. GPIOMUX diagram

GPR Register

Address: 400A_C000h base + 68h offset = 400A_C068h

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R W	GPIO_SEL																															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

IOMUXC_GPR_GPR26 field descriptions

Field	Description
GPIO_SEL	Select GPIO1 or GPIO2

Figure 2. IOMUXC_GPR26 field descriptions

According to Figure 1 and Figure 2, Table 3 can be obtained.

Table 3. High-speed GPIO mapping table

	GPIO	PAD
IOMUXC_GPR26[28:0] = 0	GPIO1[28:0]	GPIO[13:0],GPIO_AD[14:0]
	GPIO2[13:0]	GPIO_SD[13:0]
IOMUXC_GPR26[28:0] = 1	GPIO1[28:0]	NA
	GPIO2[28:0]	GPIO[13:0],GPIO_AD[14:0]

3.3 SAI

There are three SAIs in the RT1020 but only two in the RT1010. SAI2 is removed from the RT1010 and only SAI1 and SAI3 are provided in RT1010.

3.4 OTFAD

For on-the-fly decryption and XIP, the RT1020 uses the Bus Encryption Engine (BEE) while RT1010 uses the On-the-fly AES Decryption (OTFAD). No software or hardware changes are required if ROM is used for the image decryption. Since the BEE and OTFAD use different IP, there are some differences. For example, BEE encrypts paramters by PRDB but OTAFD by Key Blob.

- **BEE**

  Typical AES engine performs a single-round operation in 1-2 machine cycles.

- **OTFAD**

  Heavily pipelined AES engine, optimized for decryption, performs three rounds per cycle.

4 Hardware design

The hardware design key points of the RT1010 is almost same as the RT1020. For details, refer to RT1010 Hardware Design Guide.

5 Revision history

Table 4. Revision history

Revision No.	Date	Description
0	May 2019	Initial release
1	November	Updated Table1

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