AN12724

LPC800 Reset Circuit Design and VDD Timing Control Guideline

Rev. 0 — 19 February 2020

Application Note

Contents

1 LPC800 start-up behavior

During LPC800 development, depending on different application requirement such as power-up ramp condition or VDD climb-up speed, there may be start-up issue.

This application note document list few solutions for reset circuit design and VDD timing control, to let LPC800 start-up more stably.

The document provides an introduction for LPC800 reset principle.

LPC800 has two methods for power-up reset: Power-On Reset (POR), and by reset pin.

Chip can use either reset method to get proper reset during power-on.

1.1 Reset by POR

By this method, MCU requires:

Before ramping up, the minimum wait time (twait) of the power supply on the VDD pin (200 mV or below) is 2 ms. This is a requirement for LPC81x/82x but not for LPC80x/84x. VDD raises above 1.71 V (LPC80x) or 1.8 V (LPC81x, LPC82x, LPC84x), completes a whole reset process, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0.

1.2 Reset by Reset Pin

By this method, MCU requires:

When VDD reach to 1.8 V, after 60-200 µs (different series have different spec), A LOW-going pulse (below 0.3VDD) not short than 1 µs on reset pin take chip into reset status, then if the voltage on reset pin raises to high (above 0.7VDD), chip will release from reset status, completes a whole reset process, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0.

The most unstable start-up issue caused by not fitting the POR start-up condition, using reset pin to get chip reset is a popular solution for these issues.

2 LPC800 reset circuit design guideline

- RC reset circuit
- MOSFET reset circuit

2.1 RC reset circuit

The RC reset circuit is a low-cost reset circuit as shown in Figure 1.

Adjust the R and C value, to ensure that when VDD reaches to 1.8 V, after 200 µs, a low-going pulse (below 0.3 VDD) not short then 1 µs on reset pin. The chip can get a worked reset, promise the LPC800 have a stable start-up.

Timing formula is: Tr = k * R * C

k stands for timing factor, if voltage thread hold for reset pin is 0.54 VDD=1.8 V, k=0.7

The formula suggests: R = 37 kΩ, C = 0.22 μF, and it spends 5.6 ms when the voltage on reset pin reaches to 1.8 V.

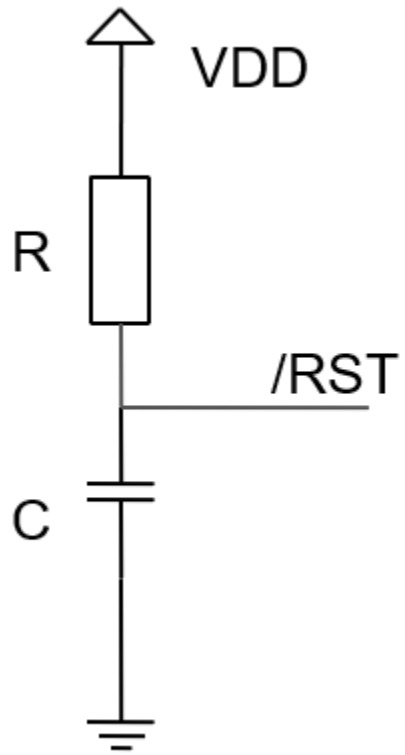


Figure 1. RC reset circuit

2.2 MOSFET reset circuit

In some application, you need to provide reset signal according to the VDD voltage. For example, if the VDD climbing speed is very slow the reset signal should be provided at VDD reach to a certain value, ensure chip can get a stable power up reset.

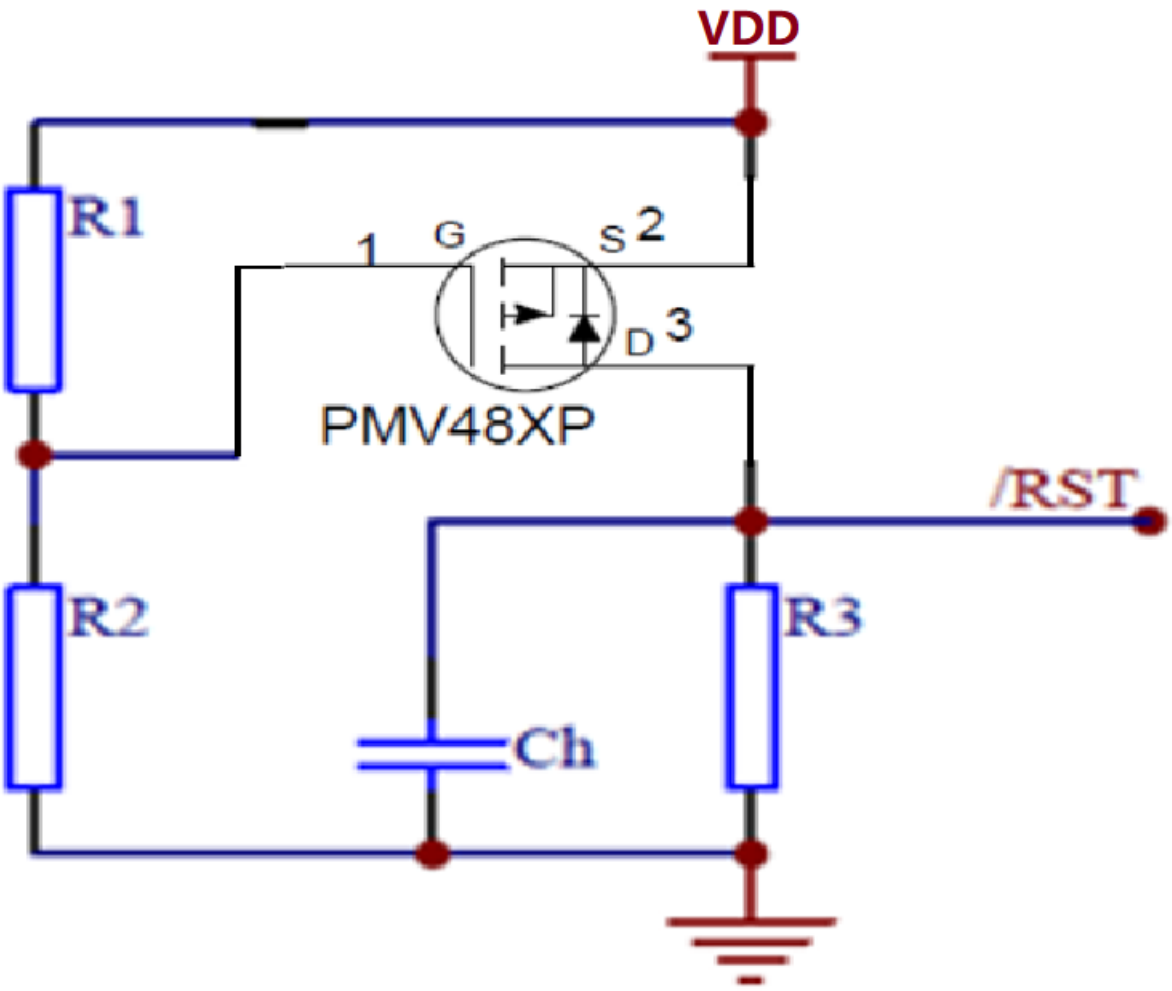


Figure 2. MOSFET reset circuit

Using MOS to control RST signal according VDD supply, require when VDD raises to 1.8v, RST signal will output a “high”.

Calculate the R2/R1;

Define:

Vdt = VDD voltage, when MOSFET tube conduction

Vsgth = source-gate threshold voltage

Because: [R2/(R1+R2)]* Vdt = Vdt – Vsgth

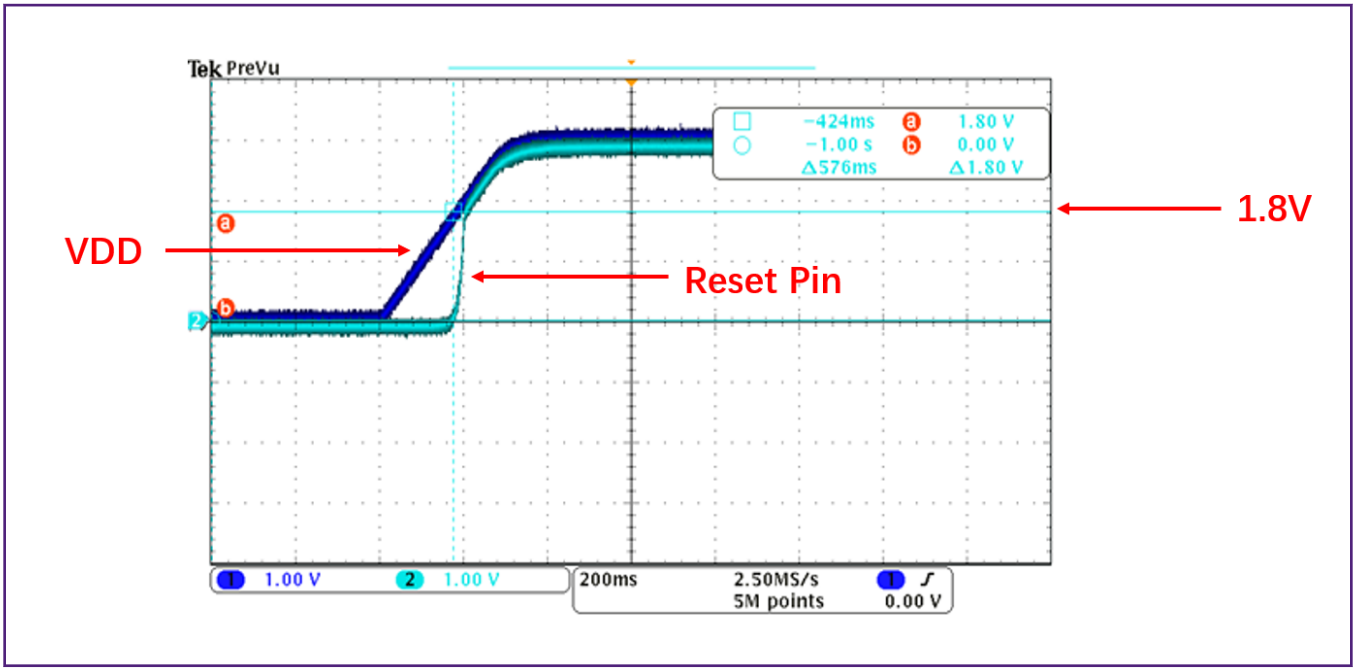
Get: R2/R1 = (Vdt - Vsgth)/ Vsgth

According this formula:

When using a MOSFET Vsgth=0.9 V, if want output the RST “high” when VDD raising to 1.8 V,

R2/R1 = (1.8 – 0.9) / 0.9 = 1

In My testing, using Vsgth=0.9 V MOSFET PMV48XP, R2=R1=10KOhm, get the result as below:



The waves on VDD and reset pin based MOSFET reset circuit

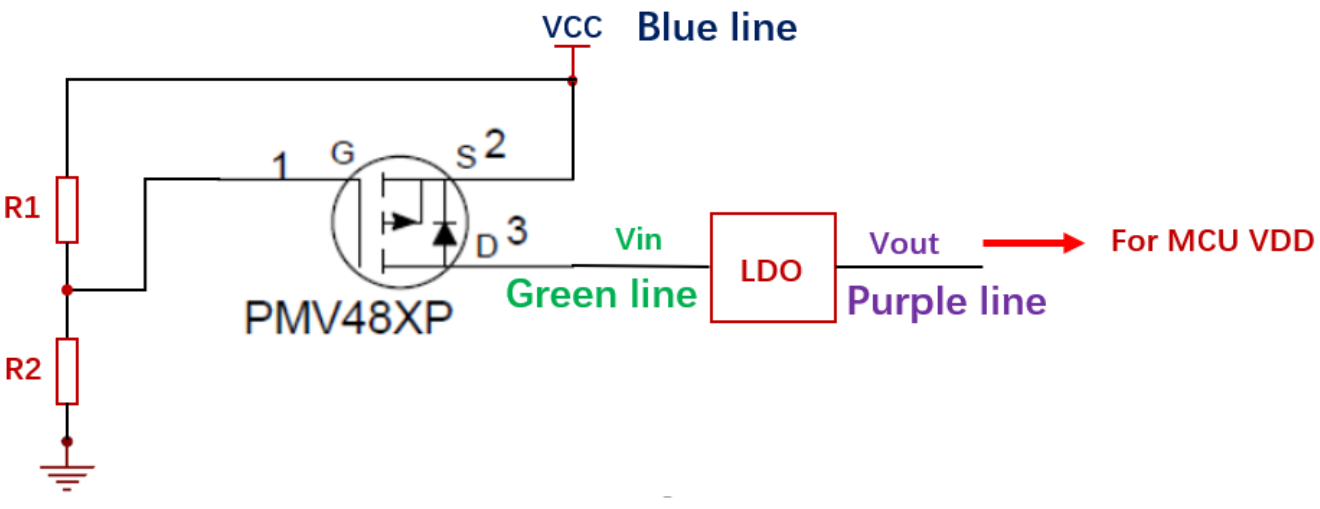
3 VDD timing control guideline

In some application, it requires VDD climbing very faster. The following are two kinds of relative testing results. The workable solution is provided according to the results.

3.1 Testing1 – Using normal LDO

In test mode 1, we use a normal LDO to provide the Vout for MCU VDD, reference solution shown as Fig4.

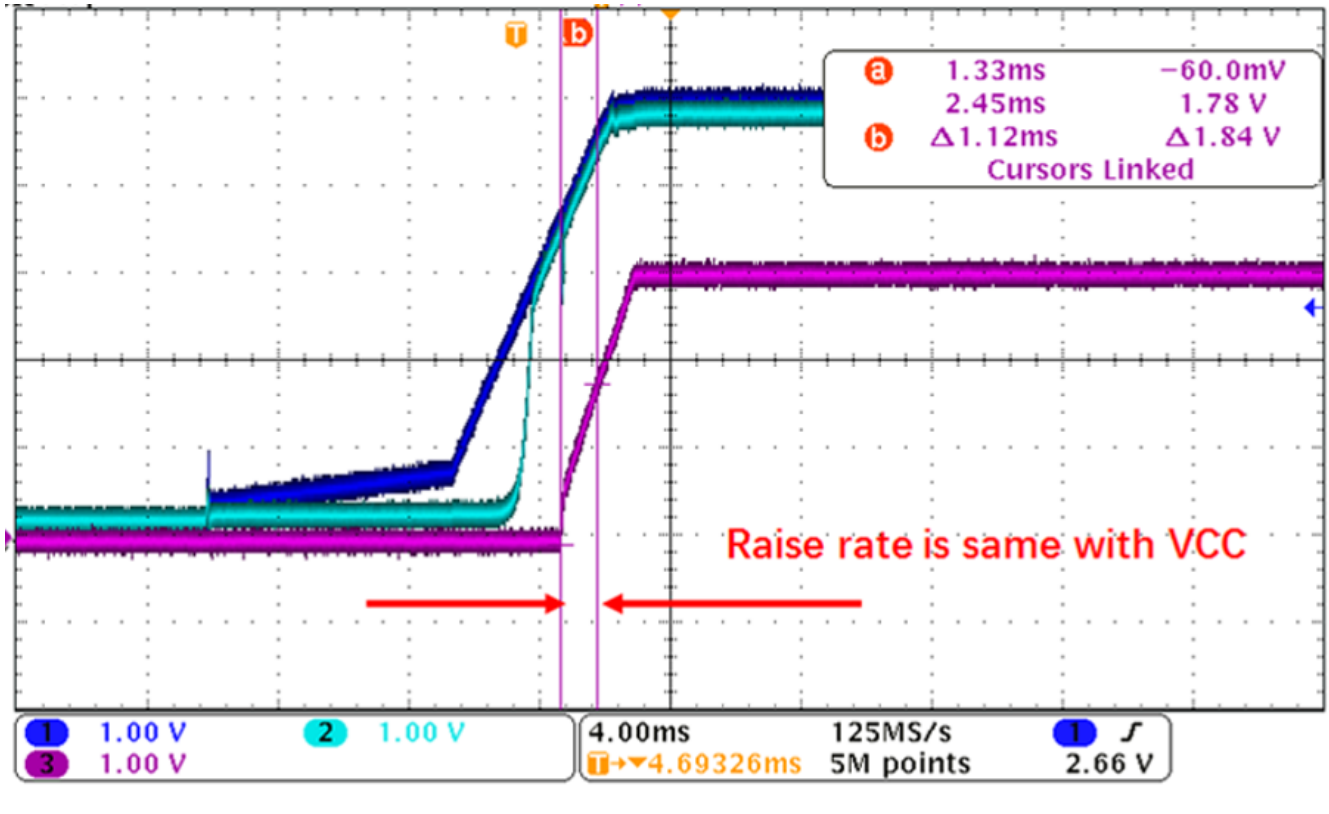
Table 1.



Using normal LDO to speed up MCU VDD climbing rate

The testing result shown as Fig5:

Table 2.



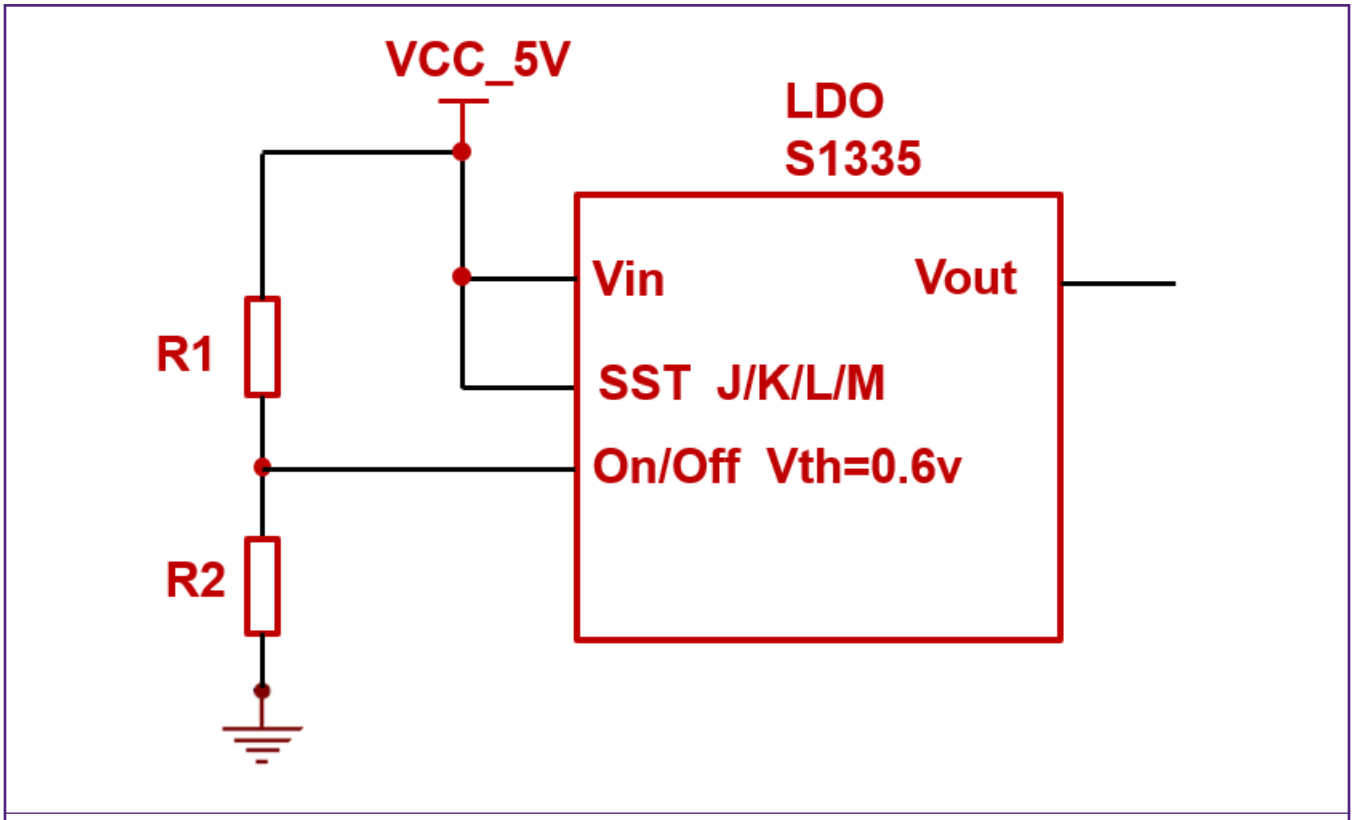
Testing result for using normal LDO

According the testing result, the climb rate of LDO Vout is same with VCC, so this solution cannot provide the result needed for speed up MCU VDD climbing rate. Below, we suggest another solution using LDO with On/Off control.

3.2 Testing2 – Using LDO with On/Off control

Second, we use a LDO with On/Off control to provide the Vout for MCU VDD, reference solution shown as Fig6.

Table 3.



Using LDO with On/Off control to speed up MCU VDD climbing rate

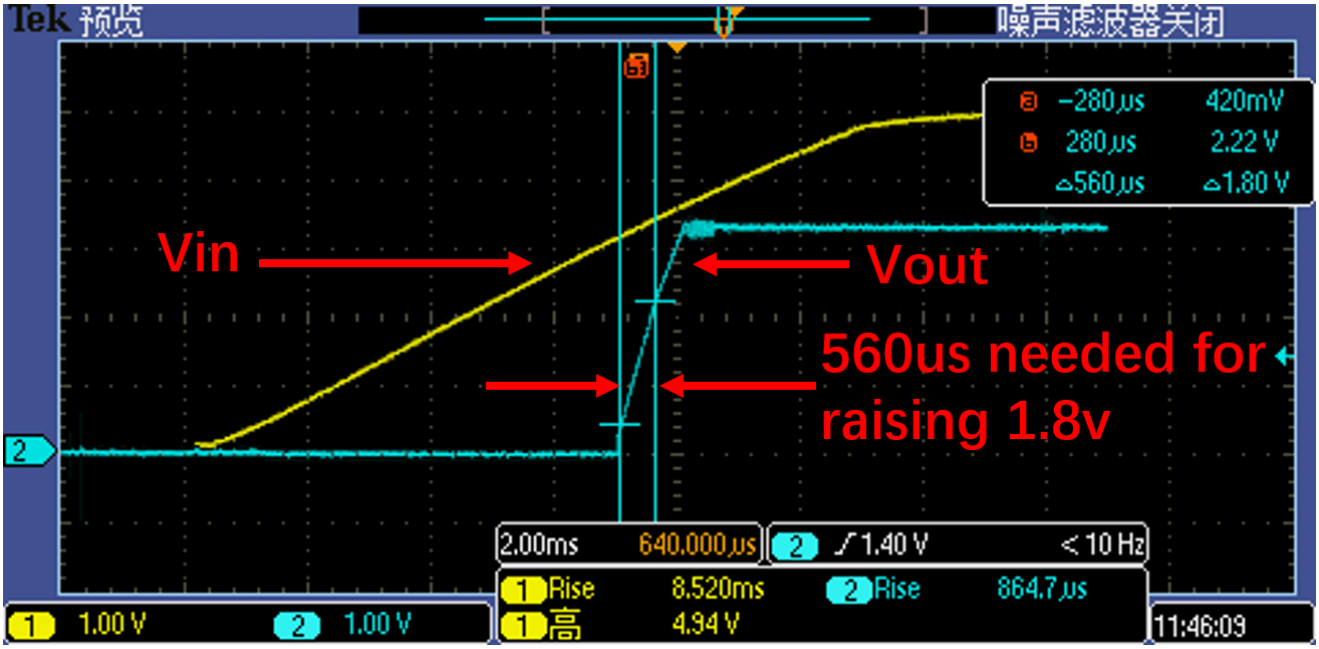
In this solution, because Vth is solid at 0.6v, we can adjust the proportion of R1, R2, to choose when Vout can be output according the voltage of Vin.

For example, if we use R1=4R2, make Von/off =1/5*Vin = 0.6v, in this condition, the Vout can be output when Vin raised to 3v.

User can also use different proportion for R1 and R2, to get different “gate” time, for example, if we use R1=7R2, will make Von/off = 1/8*Vin = 0.6v, in this condition, the Vout will be output when Vin raised to 4.8v.

Below testing result bases on condition of R1=4R2, the result shown as fig5:

Table 4.



Testing result for using normal LDO with On/Off control

From the test result, when Vin raised to 3v, Von/off reach the Vth of 0.6v, the Vout get output. The time is only 560us for Vout raised from 0v to 1.8v.

According the result, the solution by using LDO with On/Off pin, can speed up the Vout climbing rate successfully.

3.3 An example for using LDO with On/Off control

For earlier versions of LPC802, there is a problem existed for the rise time of the power supply ramp, it requires the rise time of the power supply ramp on the VDD pin must be 1 ms or above. That needs an extra circuit to speed up the VDD rising speed for some application which the power supply speed is limited. The solution of using LDO with On/Off control just can solve the problem for these applications.

For latest version of LPC802 (Rev 1D and later), this power supply ramp problem has been fixed, customer can use the latest version chips to avoid this problem.

4 Revison history

This table summarizes revisions to this document.

Table 5. Revision history

Rev	Date	Description
0	02/2020	Initial version

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For sales office addresses, please send an email to: salesaddresses@nxp.com

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