# AN12779

## Migrating from KL Series to K32L2 Series

Rev. 0 — July 2020 Application Note

Contents



# 1 Introduction

K32L2 family is an expansion of K32L series, that provides a unique balance of core efficiency, low-power modes, memory scalability, and mixed signal integration.

K32L2 family includes Arm Cortex-M0+ processor, with options scaling from 64 KB to 512 KB flash and 32 KB to 128 KB SRAM. It is the target for secure and power-optimized MCUs for next generation power-conscious and low-leakage applications.

It is simple to port to the new K32L2 family for the users of the Kinetis KL series MCUs. There are also tips and information that require attention. This application note provides a short description of those tips as well as provides a general peripheral difference between classic KL series and K32L2. Also, this document provides information about some differences between K32L2B and K32L2A.

## 1.1 Orderable part numbers

Table 1. Orderable part numbers

| Part number | Flash | RAM | Pin count | Package |
|---|---|---|---|---|
| K32L2B11Vxx0A | 64 | 32 | 32, 48, 64 | QFN, LQFP, MAPBGA |
| K32L2B21Vxx0A | 128 | 32 | 32, 48, 64 | QFN, LQFP, MAPBGA |
| K32L2B31Vxx0A | 256 | 32 | 32, 48, 64 | QFN, LQFP, MAPBGA |
| K32L2A31Vxx1A | 256 | 128 | 64, 100 | LQFP |
| K32L2A41Vxx1A | 512 | 128 | 64, 100 | LQFP |

## 1.2 Migration scenario

1. Here are the scenario for porting KL series to K32L2If you are using KL1x, KL2x (except KL28), KL3x, KL4x series, you can port to K32L2B, as most of the peripherals are compatible.
2. If you are using Kinetis KL28 and KL8x you can port to K32L2A, as most of the peripherals are compatible.
3. If your current design has limited resources on Flash, SRAM, and performance, you can port to K32L2A. K32L2A has the highest performance and memory resource in all KL series and K32L2 family.
4. KL27Z64 and KL27Z256 has some differences, although they share same QFN32 package, the following sections describes the details. KL27Z256 and KL43Z256 series are 100% compatible with K32L2B, while KL27Z64 has minor differences.
5. K32L2A and K32L2B does not have a hardware I2S/SAI module. You can use FlexIO to simulate the I2S interface.
6. The new K32L2 family has few package options than the classic KL series.

7. K32L2A has a High Speed Run mode (HSRUN), which can boot core frequency to 96 MHz. However, there are limitations in HSRUN mode, such as MCU cannot erase/program internal flash when in HSRUN mode.

## 1.3 K32L2B block diagram

The operating frequency of K32L2B can run up to 48 MHz and compatible with classic KL series peripherals and system architecture.

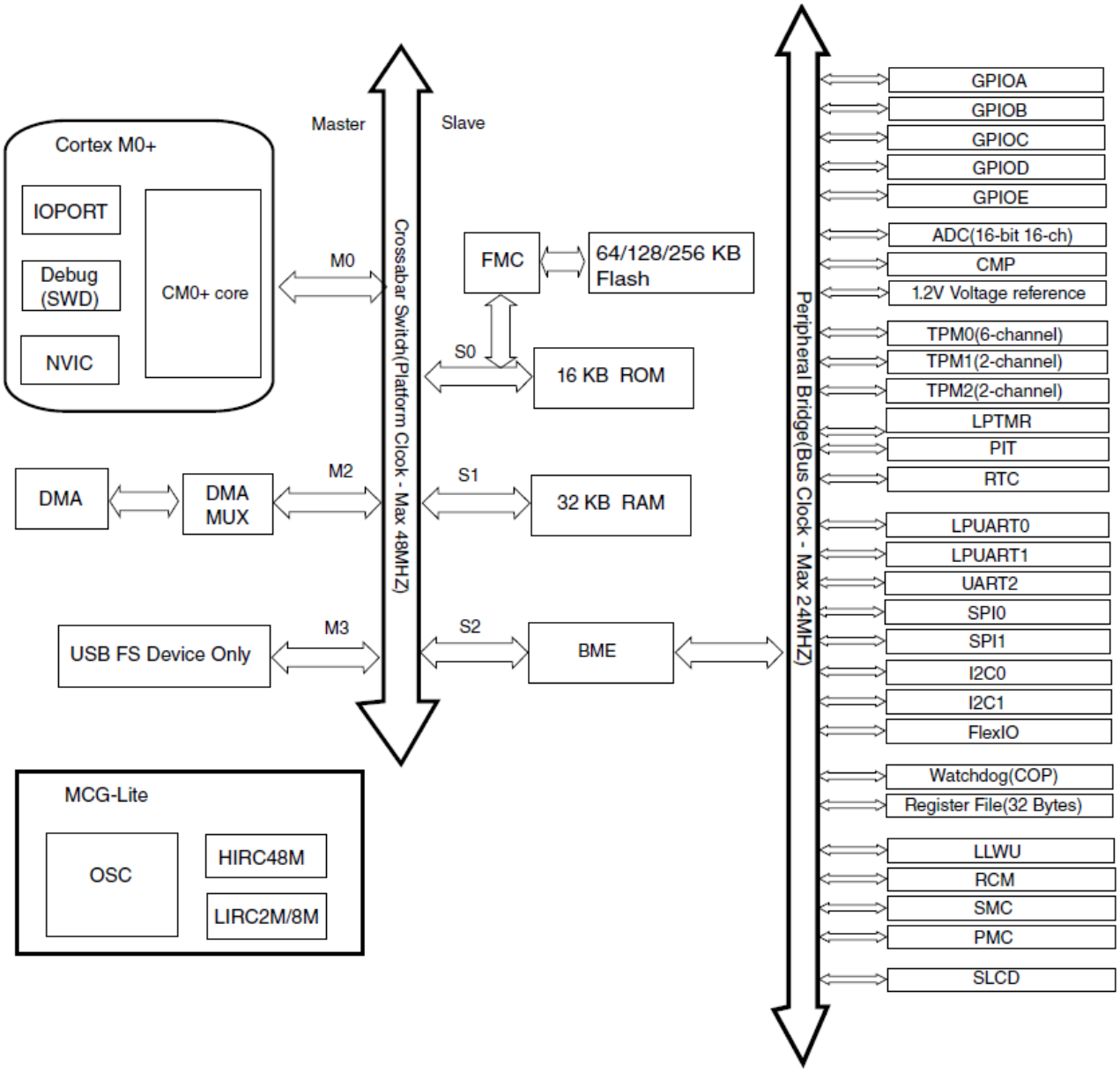


Figure 1. K32L2B block diagram

## 1.4 K32L2A block diagram

K32L2A has the highest performance in all K32L2 and KL series. The core can run up to 96 MHz in HSRUN mode. As shown in the following figure, the clock system architecture and communication peripherals are different from classic KL series and K32L2B. K32L2A is compatible with KL28.

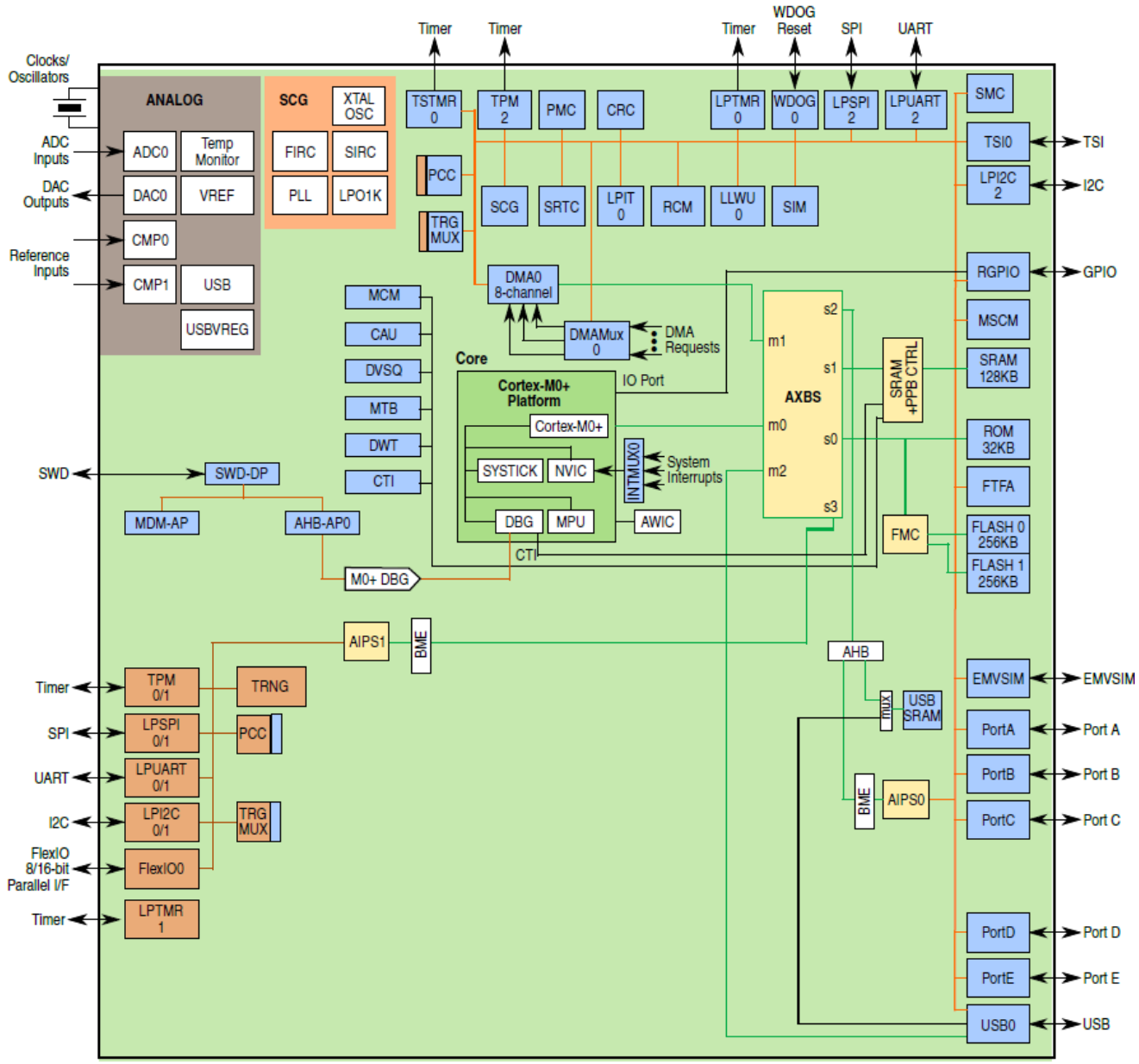


Figure 2. K32L2A block diagram

# 2 K32L2 system and clock architecture

## 2.1 K32L2B

The clock system is important for porting to a new platform. For K32L2B, the clock system is MCG_Lite and SIM module. It is an architecture for the classic KL series. KL26, KL8x, and other KL parts use MCG instead of MCG_Lite. See the corresponding Data Sheet and Reference Manual for details between MCG and MCG_Lite.

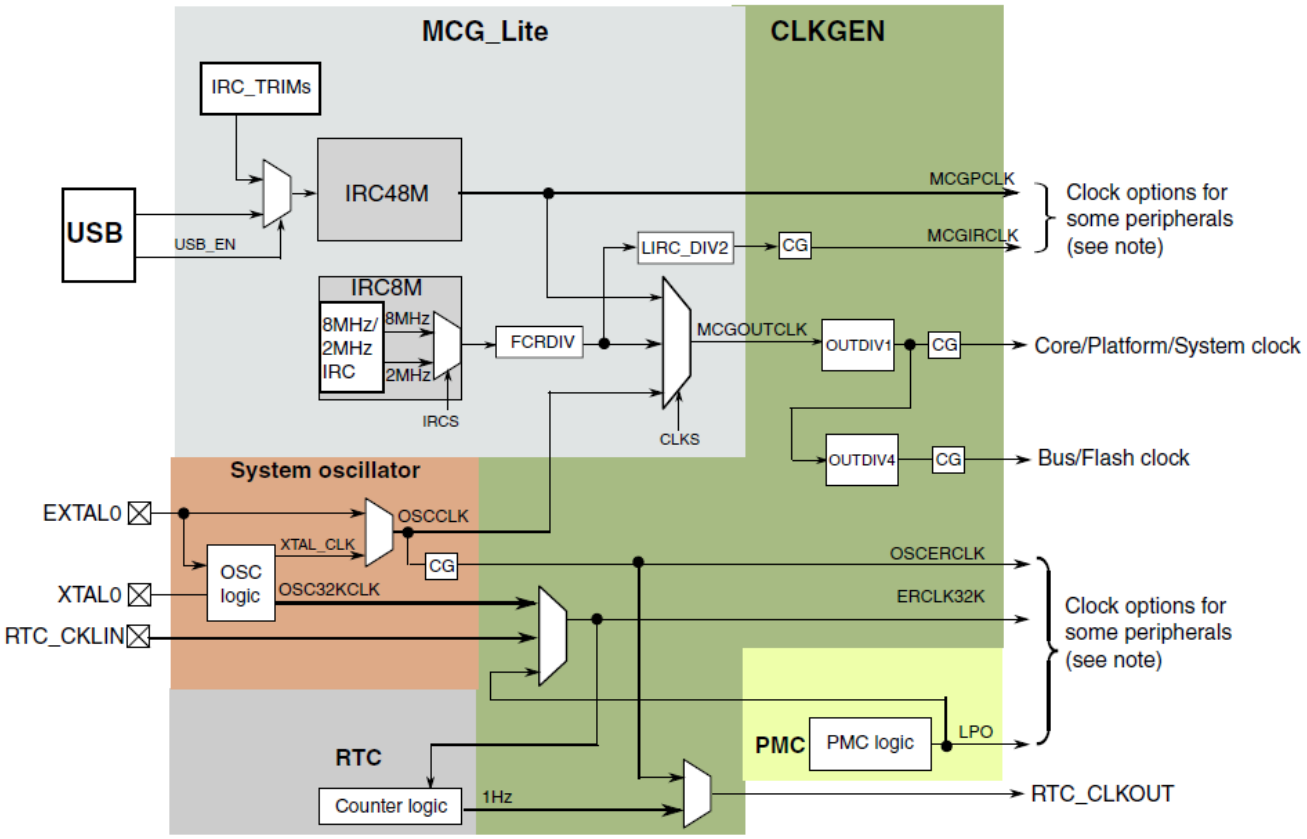


Figure 3. K32LB use MCG_Lite/SIM as clock generation/control architecture

## 2.2 K32L2A

K32L2A uses the new generation clock module called SCG.

K32L2Ais a new clock architecture in comparison with classic KL parts which is MCG (MCG-Lite). It makes the clock source control easy to use and flexible.

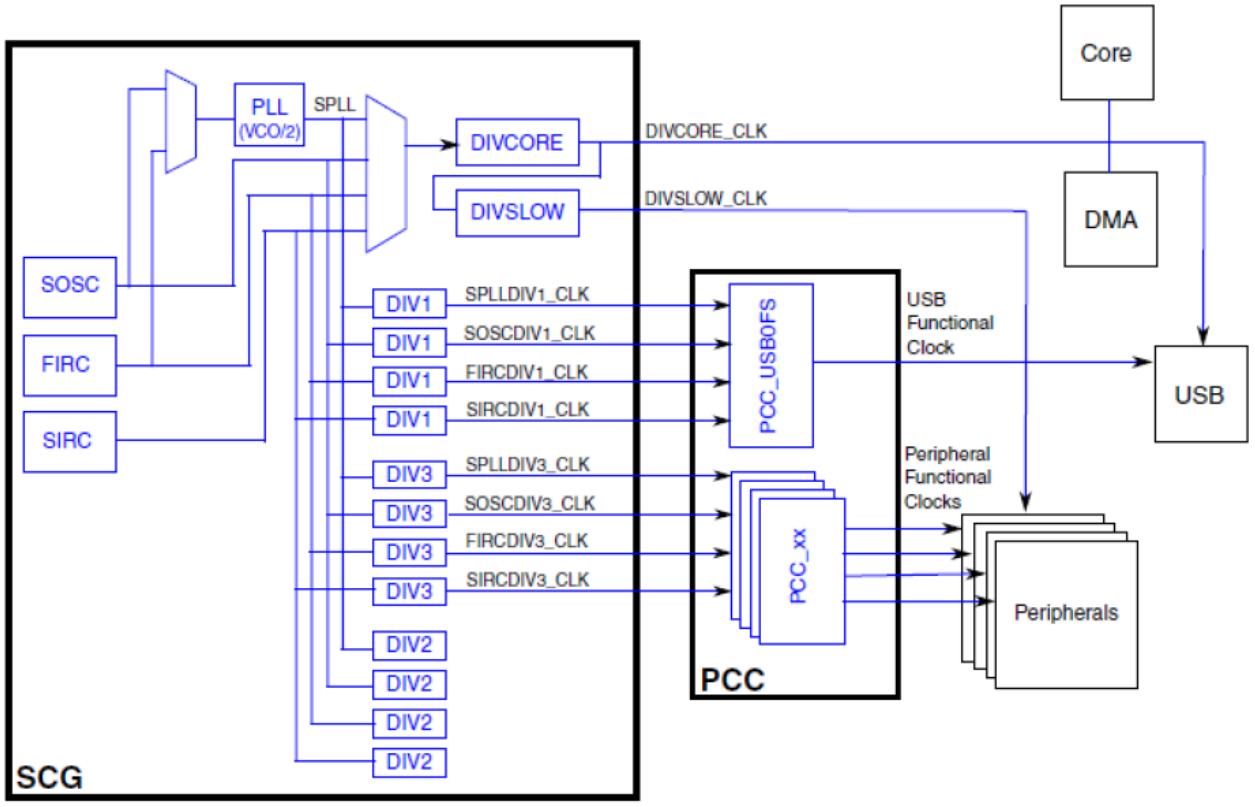


Figure 4. K32LA use SCG/PCC as clock generation/control architecture

The SCG provides three clock sources as shown in the following table. Each clock source is a controlled separated register.

Table 2. SCG clock source

| Clock source | Description | Comments |
|---|---|---|
| SOSC | Output of the external oscillator, a crystal, or externally applied clock input | 32-40 kHz, or 3-32 MHz crystal oscillator, can be used as the clock source for PLL, RTC, or System/Peripheral |
| SIRC | Output of the slow(2/8 MHz) internal RC oscillator | 2/8 MHz is set by SCG_SIRCCFG[RANGE] |
| FIRC | Output of the fast (48/52/56/60 MHz) internal RC oscillator | 48/52/56/60 MHz is set by SCG_FIRCCFG[RANGE] |

SCG also includes System PLL (SPLL), it is similar to classic MCG's PLL with following features:

- The output frequency is 72 MHz for RUN mode or 96 MHz for HSRUN mode
- Voltage-Controlled Oscillator (VCO)
- PLL output frequency is half of VCO output frequency.
- Selectable Internal or External reference clock is used as the PLL source
- Can be selected as the clock source for the MCU system clocks
- Two programmable post-divider clock outputs, which can be used as clock sources for other on-chip peripherals

Peripheral Clock Control module (PCC) is a replacement for SIM. It provides peripheral clock control and configuration functions. The main function is clock gate control for peripherals. Each peripheral has a separate PCC_XXX register to control all the clock features of that module and makes it easy to use than SIM.

## 2.3 Summary

- K32L2B clock system inherited from classic KL series and uses MCG_Lite and SIM.
- K32L2A uses SCG and PCC, and it is compatible with KL28.

For more details on the K32L2A clock system, see AN12680.

# 3 K32L2A typical peripherals

This section focuses on typical communication peripheral differences between K32L2 and other classic KL series. The following table summarizes typical communication peripherals used in each part and it lists parts in classic KL series.

**Table 3. Major peripheral differences**

| PARTS | UART | SPI | I2C | USB | SMARTCARD | FlexIO | TRGMUX | TSI |
|---|---|---|---|---|---|---|---|---|
| K32L2B | UART<br>LPUART | SPI | I2C | USBFS | N | Y | N | N |
| K32L2A | LPUART | LPSPI | LPI2C | USBFSOTG | Y | Y | Y | Y |
| KL27Z64 | UART<br>LPUART | SPI | I2C | USBFS | N | Y | N | N |
| KL27Z256 | UART<br>LPUART | SPI | I2C | USBFS | N | Y | N | N |
| KL43 | UART<br>LPUART | SPI | I2C | USBFS | N | Y | N | N |
| KL26 | UART<br>LPUART | SPI | I2C | USBFSOTG | N | N | N | N |
| KL8x | LPUART | SPI | I2C | USBFSOTG | Y | Y | Y | Y |
| KL28 | LPUART | LPSPI | LPI2C | USBFSOTG | Y | Y | Y | Y |

For more details and comparison see Kinetics L Series Selector Guide.

LPSPI, LPI2C, and LPUART are fully functional when the system enters Low-Power mode, and also supports DMA driven operation. This feature makes it possible to save more power in low-power applications.

## 3.1 LPSPI

LPSPI works with DMA in Low-Power mode and uses VLPS mode. This means that LPSPI communication can be maintained and enter in Low-Power mode to reduce power consumption. This feature is available for both Master and Slave mode.

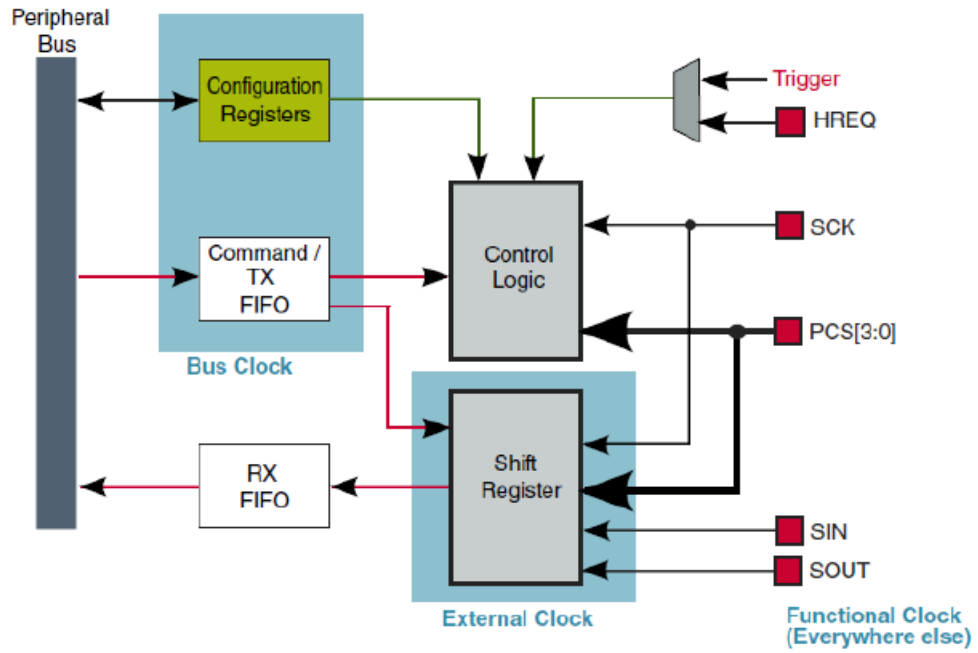


Figure 5. LPSPI

Compared with the old SPI/DSPI module, LPSPI has the following enhancements, as shown in the following table.

Table 4. Comparison between LPSPI and SPI

| Feature | LPSPI | SPI/DSPI | Benefit |
|---|---|---|---|
| Separated command FIFO and data FIFO | Yes | No | Software oriented design, easy to use with DMA. Reduce SW intervention and increase data throughout. |
| Operational in VLPS in Slave mode | Yes | No | LPSPI can receive data in VLPS mode. Give more flexible option of Low-Power mode selection. |
| Host request input can be used to control the start time of an SPI bus transfer | Yes | No | External pin can direct trigger SPI to send/receive data, help to reduce CPU overhead. |

For more details on LPSPI, see AN5320.

## 3.2 LPI2C

Compared with the classic I2C module. LPI2C works with DMA in Low-Power mode in comparison with the classic I2C module and uses VLPS mode.

This means that I2C communication can be maintained and enter in Low-Power mode to reduce power consumption. In such cases, DMA takes over CPU to take data transmission task.

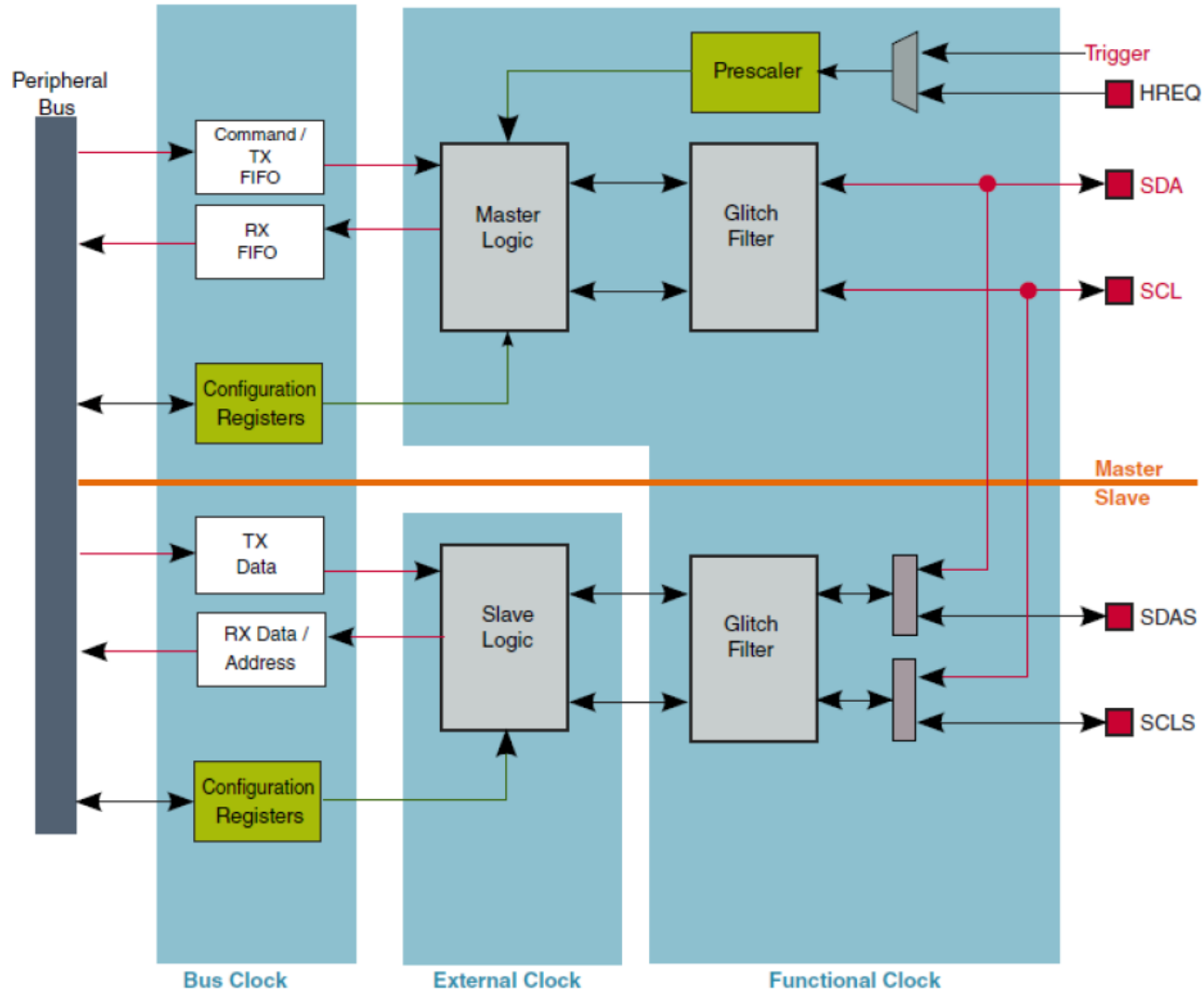


Figure 6. LPI2C

Compared with the old I2C module, LPI2C has several enhancements, as shown in the following table:

Table 5. Comparison between LPI2C and I2C

| Feature | LPI2C | I2C | Benefit |
|---|---|---|---|
| Function as both master and slave in the same time | Yes | No | Support I2C bridge to transfer data. Enable the fastest switch from master to salve with low SW intervention. |
| Configurable pin mode (4-wire, 2-wire or separately 2-wire for master and salve, as well as drive type) | Yes, there are 8 selectable pin types to get difference functions | No, support 2-wire | Flexible to interface with external custom line drivers, provides higher bus driver capability, reduces total system BOM. |

*Table continues on the next page...*

**Table 5. Comparison between LPI2C and I2C (continued)**

| Feature | LPI2C | I2C | Benefit |
|---|---|---|---|
| Support Standard, Fast Fast+, Ultra-Fast and HS-mode | Yes | Support Standard and Fast mode. | Support all I2C-bus protocol logics for different applications with baud rate up to 5 Mbit/s. |
| Both transmit and receive FIFO with DMA supported | Yes, support 4 words command/transmit, and 4 words FIFO receive FIFO | No, some parts support dual buffer and no command FIFO supported | Command FIFO based state machine provides the best performance with low CPU overhead. |
| Unified peripheral clock control register names | Yes | No | Software-oriented design makes code compatible. |
| Software reset master or salve | Yes | No | Conveniently reset master or slave when bus lockup occurs. |
| Configurable host trigger sources | Yes, available to configure host request select from LPI2C HREQ or input trigger | No | Automatic trigger I2C master to initiate a START condition when bus is idle. Reduces SW handshake overhead. |
| Configurable timing parameters of SCL and SDA | Support dedicated register to configure setup host time and valid delay of data, as well as high period and low period of clock. | Determined by I2C baud rate setting | More flexible to configure I2C timing. |
| Separately address matching flag | Support separately address match flag for address0/1 and general call match event | Just one address matching flag to indicate the address matching event occur | Reduce to software intervention to differ matching address in multi-master system. |
| • More status indication and interrupt control--Bit error detection by slave<br>• End of packet detection by master | • Support stop, start, FIFO, address match, and bit error status indication and other status flag<br>• support interrupt control for these flags | • Combine some status to one interrupt flag (CCIF).<br>• Can not control stop and start interrupt separately<br>• No bit error detection | Able to get more status information and flexible to enable expected interrupt, avoid generating unwanted interrupt.<br>Able to do fault detection and recover in noise environment.<br>Reduce SW overhead and increase the bus throughout. |
| Flexible master received data match can generate interrupt on data match or discard unwanted data | Yes | No | Reduce SW overhead to do pattern search |
| Automatic STOP generation | Yes | No | Reduce SW overhead for STOP generation |

For more details on LPI2C, see AN5301.

## 3.3 FlexIO

FlexIO is not a new module, many KL series already have this peripheral. FlexIO is a highly configurable module providing a wide range of functionality that includes:

- Emulation of various serial communication protocols.
- Flexible 16-bit timers with support for various triggers, reset, enable, and disable conditions.

The differences between FlexIO on K32L2B and K32L2A :

- The K32L2B's FlexIO has 4 shifter and 4 timers, so it can emulate 2 full duplex UART/I2C or 4 channel PWMs. K32L2B's FlexIO does not have parallel mode, so It cannot emulate 8080 or camera interface.
- The K32L2A's FlexIO has 8 shifter and 8 timers, so it can emulate 4 full duplex UART/I2C or 8 channel PWMs, also, K32L2A's FlexIO has parallel modes, so it can emulate 8080 or camera interface.

## 3.4 TRGMUX

TRGMUX is a flexible way of connecting various trigger sources to multiple pins/peripherals. It is a replacement for the SIM module in the classic KL series. The following figure shows the block diagram of TRGMUX.

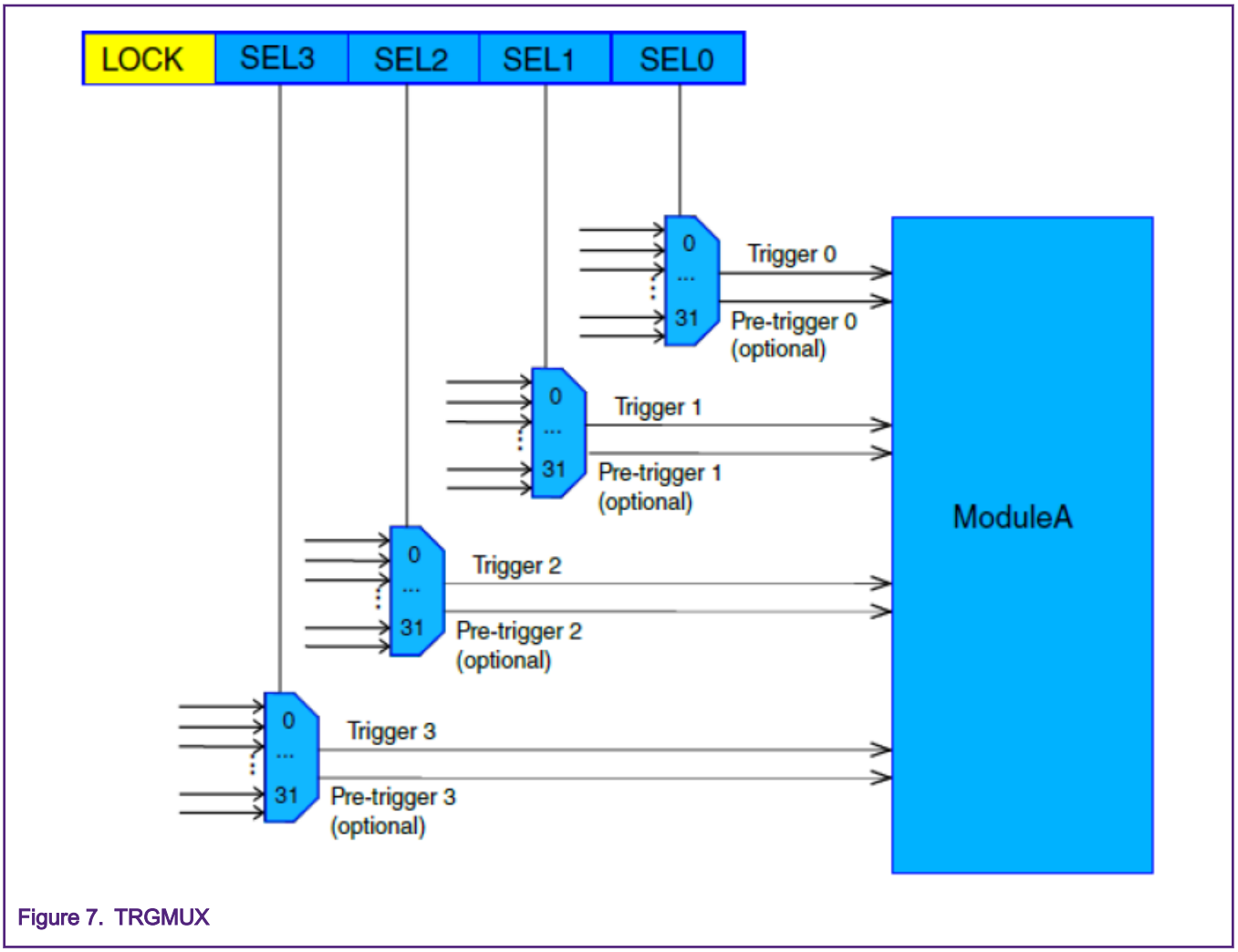


Figure 7. TRGMUX

TRGMUX is a simple interconnection peripheral that aimed to replace peripheral-to-peripheral interconnection functions in SIM. Such a separate module is powerful than an old SIM configuration and more user friendly to configure. Each peripheral has a unique 32-bit register dedicated to configuring the interconnection function.

For more details on TRGMUX, see AN5399.

## 3.5 EMVSIM

The EMVSIM is a standalone ISO7816 module that is connected to the AIPS0 peripheral bridge. It includes TX RX FIFO and various advanced features for the ISO7816 interface. The latest MCU SDK includes an EMVSIM driver.

**NOTE**

EMVSIM exists only on K32L2A.

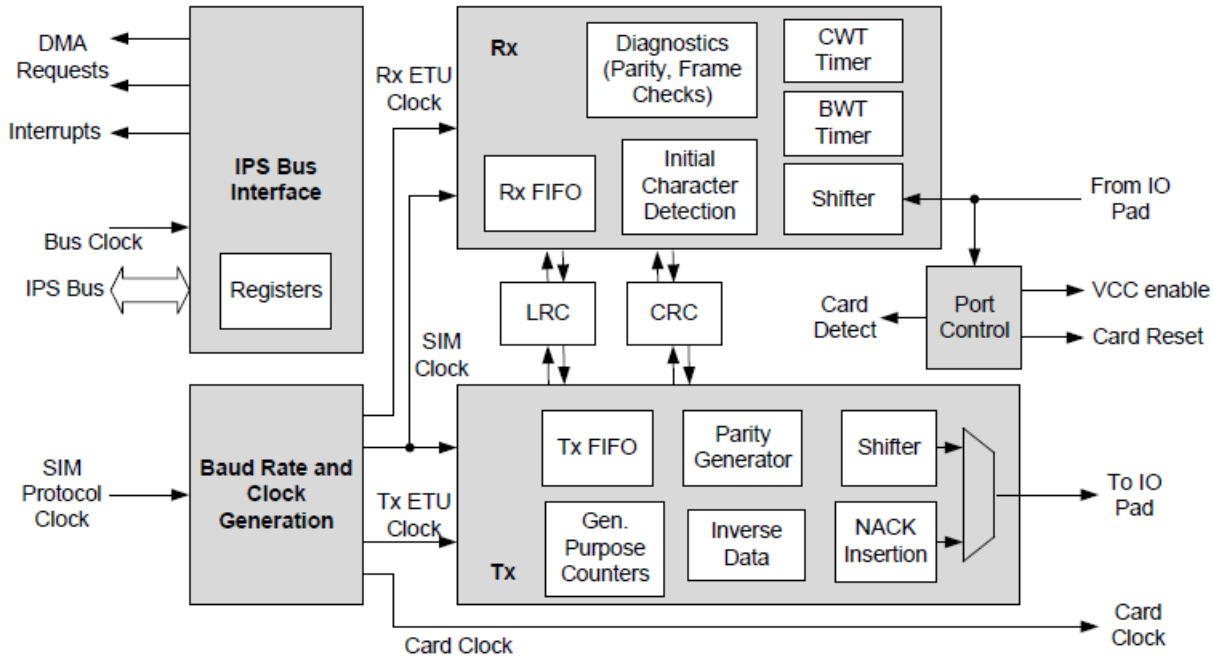


Figure 8. EMVSIM

## 3.6 Flash

Both K32L2A and K32L2B use FTFA. All flash erase/program command and operation are the same. The only difference is that K32L2B flash sector size is 1 KB while K32L2A flash sector size is 2 KB.

**NOTE**

When K32L2A is in HSRUN mode, user cannot erase/program internal flash.

# 4 Examples

## 4.1 Migration from KL1x series

KL1x family ranging from KL13 to KL17. The last number of the part name (3 - 7) roughly indicated from old parts to newly launched parts. Old parts may use old peripherals.

See Kinetis KL1x MCU Family - Fact Sheet for detail.

The list of the major difference for KL1x series as follows:

| Sub-Family | | KL13 | KL14 | KL15 | KL16 | KL17 |
|---|---|---|---|---|---|---|
| CPU Frequency | | 48MHz | 48MHz | 48MHz | 48MHz | 48MHz |
| Memory | Flash/SRAM Size | 32KB/4KB - 64KB/8KB | 32KB/4KB - 128KB/16KB | 32KB/4KB - 128KB/16KB | 32KB/4KB - 256KB/32KB | 32KB/8KB - 128KB/32KB, 256KB/32KB |
| | Boot ROM | 8KB | - | - | - | 16KB |
| Communication Interface | LPUART | 2 | 1 | 1 | 1 | 2 |
| | UART | 1 | 2 | 2 | 2 | - |
| | UART w/ ISO7816 | 1 | - | - | - | 1 |
| | SPI | 2[2] | 2[1] | 2[1] | 2[2] | 2[2] |
| | I2C | 2[3] | 2 | 2 | 2 | 2[3] |
| | I2S | - | - | - | 1 | 1 |
| | FlexIO | YES | - | - | - | YES |
| Analog Modules | ADC | 16-bit | 12-bit | 16-bit | 16-bit | 16-bit |
| | ADC Channels (SE/DE) | 11/2 - 20/4 | 11/0 - 20/0 | 11/2 - 20/4 | 11/2 - 20/4 | 11/2 - 20/4 |
| | DAC | 12-bit | - | 12-bit | 12-bit | Optional[4] |
| | VREF | Optional[6] | - | - | - | YES |
| Other Modules | CRC | YES | - | - | - | Optional[5] |
| | TSI | - | - | 9ch - 16ch | 9ch - 16ch | - |
| | Total GPIOs | 28 - 70 | 28 - 70 | 28 - 70 | 28 - 54 | 28 - 54 |
| | MCG | High Accuracy 48MHz IRC, 8/2MHz IRC | 4MHz/32KHz IRC PLL/FLL | 4MHz/32KHz IRC PLL/FLL | 4MHz/32KHz IRC PLL/FLL | High Accuracy 48MHz IRC, 8/2MHz IRC |

Figure 9. KL1x differences

For more detail see Kinetis KL1x – General-Purpose Ultra-LowPower MCUs.

When MCU resources Flash RAM and CPU performance meet current application requirements, it is recommended migrate to K32L2B, because most of the peripherals and system architecture are compatible. For the older parts, for example KL15 it requires more effort for migration, because the older part tends to have old peripherals.

Here are the key points to be notice:

1. Some of the KL series contains an 8-bit SPI module, while others have a 16-bit SPI module, K32L2B use 16-bit SPI.
2. K32L2B does not have an I2S module.
3. KL1x series does not have USB module
4. Most of GPIOs and pin mux is compatible with KL1x series, but some power pins are not (also includes K32L2B USB pins), carefully compare each pin between old parts and new parts for the new design, avoid the use of conflict pin in software.

## 4.2 Migration from KL2x series

KL2x is based on KL1x but add USB feature. KL2x is the mostly used series in the KL series. Ranging from KL24 to KL28. Which the last number of the part name roughly indicated from old parts to newly launched parts.

For more details see Kinetis KL2x Fact Sheet.

The rules apply to the KL1x series also apply to KL2x. Besides, the KL2x series has many derivative parts. The following figure shows the differences between major parts.

| Subfamily | | KL24 | KL25 | KL26 | KL27 | KL28 |
|---|---|---|---|---|---|---|
| CPU frequency | | 48 MHz | 48 MHz | 48 MHz | 48 MHz | 72 MHz ( up to 96 MHz) |
| Memory | Flash/SRAM size | 32 KB/4–128 KB /16 KB | 32 KB/4–128 KB /16 KB | 32 KB/4–256 KB /32 KB | 32 KB/8–128 KB /32 KB, 256 KB/32 KB | 512 KB/128 KB |
| | ROM | — | — | — | 16 KB | 32 KB |
| Connectivity | USB | USB OTG 2.0 LS/FS | USB OTG 2.0 LS/FS | USB OTG 2.0 LS/FS | FS USB 2.0 Slave, Crystal-less USB | Crystal-less USB |
| | UART (LPUART /with ISO7816) | 2(1 / –) | 2(1 / –) | 2(1 / –) | 2(2 / 1) | 3(3 / –) |
| | SPI | 2[1] | 2[1] | 2[2] | 2[2] | 3[6] |
| | I²C | 2 | 2 | 2 | 2[3] | 3[6] |
| | I²S | — | — | 1 | 1 | 1 |
| | FlexIO | — | — | — | YES | YES[7] |
| | EMVSIM | — | — | — | — | 1 |
| Analog modules | ADC | 12-bit | 16-bit | 16-bit | 16-bit | 16-bit |
| | ADC channels (SE/DE) | 7/0–16/0 | 7/0–16/2 | 7/0–20/4 | 7/0–17/2 | — |
| | DAC | — | 12-bit | 12-bit | Optional[4] | 12-bit |
| | VREF | — | — | — | YES | YES |
| Other modules | CRC | — | — | — | Optional[5] | YES |
| | Security | — | — | — | — | MMCAU, FAC, TRNG |
| | TSI | — | 9 ch–16 ch | 9 ch–16 ch | — | 16 ch |
| | Total GPIOs | 23–66 | 23–66 | 23–80 | 23–51 | 82 |
| | MCG | 4 MHz/32 KHz IRC PLL/FLL | 4 MHz/32 KHz IRC PLL/FLL | 4 MHz/32 KHz IRC PLL/FLL | High-accuracy 48 MHz IRC, 8/2 MHz IRC | High-accuracy 60/48 MHz IRC, 8/2 MHz IRC, |

Figure 10. KL2x differences

For more detail see Kinetis KL2x—Ultra-Low-Power MCUs with USB.

Here are the additional tips for KL2 series:

- If you are using KL28, it is recommended to migrate it to K32L2A series, they are similar. For other KL2x series, it is recommended to migrate it to K32L2B.

- Pay attention to the pin difference on KL27Z64 and KL27Z256, especially for QFN package, although some KL27Z64 and KL27Z256 share same package. The power pin definition has slight differences. For more details, see Data Sheet and Reference Manual.

## 4.3 Migration from KL3x/KL4x series

KL4x series is the closest series to K32L2B both have SLCD and USB. There are no migration efforts. See Migration scenario.

If you are using KL3x, see KLx3 Product Brief for the difference between KL3x and KL4x.

## 4.4 Migration from KL8x series

KL8x is mainly for the security application. If your application involves hardware Cryptographic accelerator for AES, DES, and temper detection then migrate it to K32L2A.

Some efforts are needed for the clock system since KL8x use classic MCG/SIM architecture while K32L2A use SCG/PCC architecture.

## 4.5 Migration between K32L2A and K32L2B

As mentioned in the above sections, K32L2A and K32L2B use different system clock and system architecture, and some communication peripherals are different. However, NXP's MCU SDK covers the different features, which makes it easier for a user to port their old firmware to the new platform.

The following table summarizes the major differences.

**Table 6. Major differences between K32L2A and K32L2B**

| Features | K32L2B | K32L2A |
|---|---|---|
| Clock | MCG_Lite/SIM | SCG/PCC |
| FlexIO | 4 timers and 4 shifters, no parallel mode | 8 timers and 8 shifters support parallel mode |
| SPI | SPI | LPSPI |
| I2C | I2C | LPI2C |
| EMVSIM | No | Yes |
| USB | USBFS | USBFSOTG |

### 4.5.1 Pinout consideration

The following table lists the incompatible pins in LQFP64 package. The user must pay attention to those pins and change software accordingly for migration.

**Table 7. Pinout differences for K32L2A and K32L2B**

| PIN index in LQFP64 | K32L2B | K32L2A |
|---|---|---|
| 48 | SCLD_VLL3 | VDD |
| 49 | SCLD_VLL2 | PTC4/LLWU_P8 |

*Table continues on the next page...*

Table 7. Pinout differences for K32L2A and K32L2B (continued)

| PIN index in LQFP64 | K32L2B | K32L2A |
|---|---|---|
| 50 | SCLD_VLL1 | PTC5/LLWU_P9 |
| 51 | SCLD_VCAP2 | PTC6/LLWU_P10 |
| 52 | SCLD_VCAP1 | PTC7 |
| 53 | PTC4/LLWU_P8 | PTC8 |
| 54 | PTC5/LLWU_P9 | PTC9 |
| 55 | PTC6/LLWU_P10 | PTC10 |
| 56 | PTC7 | PTC11/LLWU_P11 |

**NOTE**

- SLCD_VLL: LCD bias voltages. It requires external capacitors when charge pump is used. Those pins cannot be MUX to GPIO.
- SCLD_VCAP: SLCD charge pump capacitor pins. Those pins cannot be MUX to GPIO.

# 5 Summary

This application note provides the migration tips for porting from classic KL series to new K32L2 family. It lists the useful documents for the user reference. This application note cannot cover all the aspect for migration details. Some of the features such as power consumption and power mode selection are different for each part. They are not fully described here. The best and safest way for migration is to find out which peripheral is used in classic KL parts and check their differences in Datasheet and Reference Manual.

# 6 Revision history

Table 8. Revision history

| Revision number | Date | Substantive changes |
|---|---|---|
| 0 | 07/2020 | Initial release |

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