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Application Note

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The Clocks of the MPC8540

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This application note describes the different clocks in the MPC8540 device and explains how to configure them for each functional block. The MPC8540 integrates a processor core that implements the Book E PowerPC™ architecture with system logic required for networking, storage, and general-purpose embedded applications. The MPC8540 is a member of a growing family of products that combines system-level support for industry-standard interfaces to processors that implement the PowerPC architecture. The MPC8540 contains a high-performance embedded e500 processor core. The e500 core, with its 256 Kbytes of L2 cache, implements the enhanced Book E instruction set architecture and provides unprecedented levels of hardware and software debugging support.

In addition, the MPC8540 offers two integrated 10/100/1Gb three-speed Ethernet controllers (TSECs), a 10/100 fast Ethernet (maintenance) port, a DDR SDRAM memory controller, a 64-bit PCI/PCI-X controller, an 8-bit RapidIO port, a programmable interrupt controller, an I^2C controller, a 4-channel DMA controller, a general-purpose I/O port, and two universal asynchronous receiver/transmitters (DUART). Figure 1 shows the major functional units of the MPC8540.

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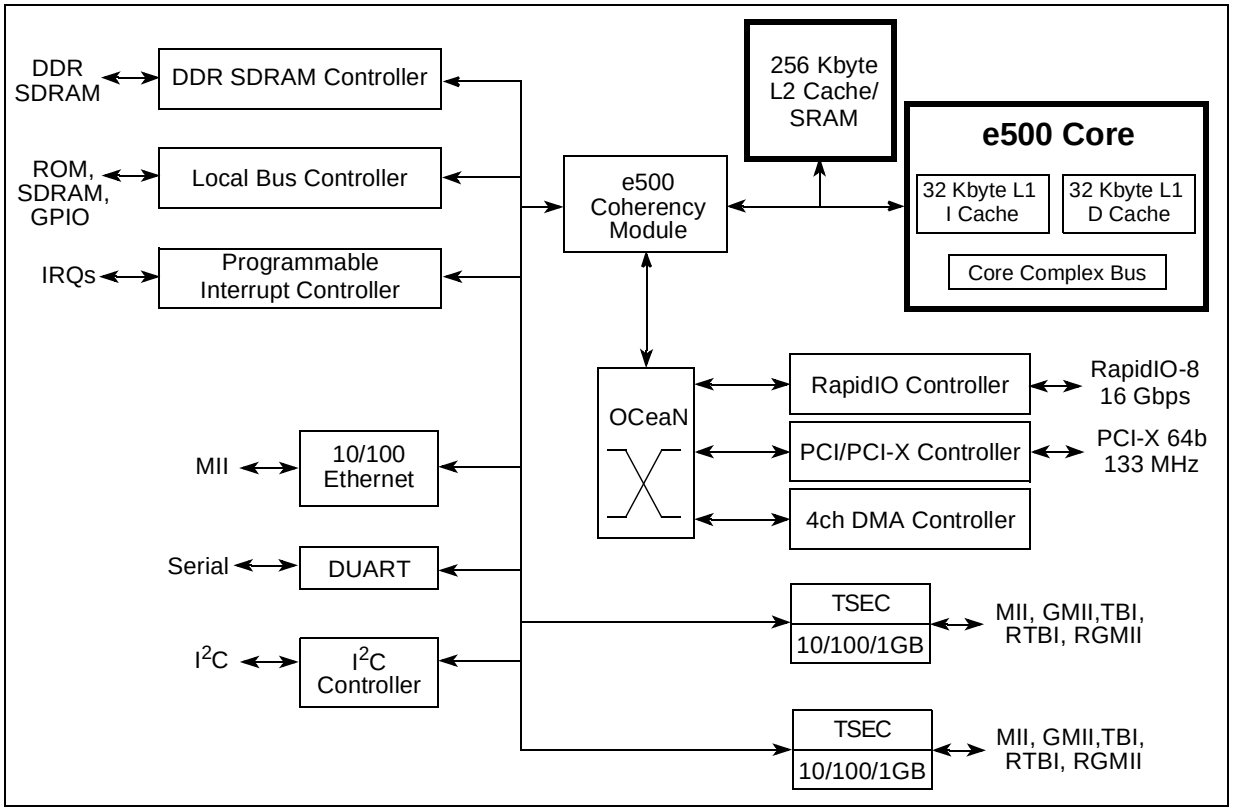

Figure 1. MPC8540 Functional Block Diagram

1 Clocking Architecture

The clocking requirements of the MPC8540 functional blocks vary both in terms of the clock source and the AC timings. For details on AC timing requirements, see the *MPC8540 Preliminary Hardware Specifications*. The MPC8540 takes a single-input system clock (SYSCLK) as its primary clock source for the e500 core and all functional blocks and interfaces that operate synchronously with the core. The SYSCLK input clock creates the frequency for the core complex bus (CCB) clock, also called the platform clock, through multipliers of the device phase locked loop (PLL). The CCB clock is used by virtually all the synchronous system logic, including the L2 cache, the DDR SDRAM, the local bus memory controllers, and other internal blocks such as the interrupt controller. The CCB clock, in turn, feeds into the e500 core PLL to provide the frequency for the e500 core clock. Figure 2 shows the clock subsystem block diagram.

The frequency of the CCB clock is derived from the input clock (SYSCLK) with the use of a PLL device. The cfg_sys_pll[0:3] reset configuration signals shown in Figure 2 represent the signals that determine the configuration of the PLL. The ratio relationship between the CCB and the SYSCLK is determined by the PLL. The cfg_sys_pll[0:3] refers to signals LA[28:31] as shown in Table 2. The values of these signals at power-on reset determines the PLL configuration and therefore the related multiplier ratio.

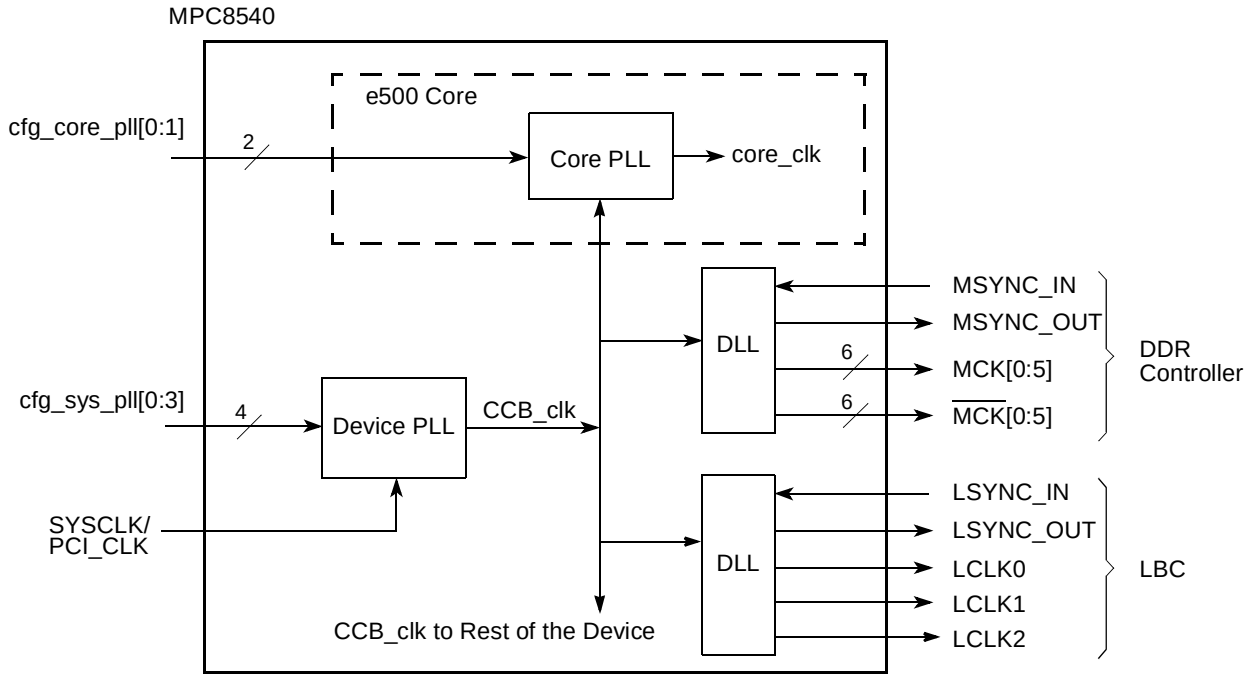

Figure 2. Clock Subsystem Block Diagram

The CCB clock derives other frequencies used throughout the device. This also applies to the e500 core clock. The e500 core clock is determined by the ratio created by the core PLL configuration signals labeled as cfg_core_pll[0:1] in Figure 2. These signals are the core PLL configuration signals (LALE and LGPL2) and are shown in Table 3. The values of these signals at power-on reset determine the core PLL configuration and therefore the related multiplier ratio.

NOTE

Reset configuration signals must conform to the following guidelines:
Pins are set by using a 4.7-kΩ pull-up resistor. A zero value for a signal is determined if the pin is pulled down to ground. Pull-down resistors should have a 4.7-kΩ value.

Table 1 gives an overview of the relationship between the various blocks and their clocks and shows how these clocks are derived.

Table 1. Functional Blocks and Clocks

Functional Block	Clock	Ratio (Clock:Source)	Ratio Definition
DDR memory	Memory clock	CCB:memory = 2:1	—
DUART	N/A	Software-programmable baud generators divide the CCB clock by 1 to (2^{16} - 1) and generate a 16x clock for the transmitter and receiver engines.	See the *MPC8540 PowerQUICC III Host Processor Reference Manual*.
e500 core	Core clock	e500 core:CCB	Table 3

Table 1. Functional Blocks and Clocks (continued)

Functional Block	Clock	Ratio (Clock:Source)	Ratio Definition
Ethernet	TSEC*n*_GTX_CLK TSEC*n*_RX_CLK TSEC*n*_TX_CLK EC_MDC EC_GTX_CLK125	See the *MPC8540 PowerQUICC III Host Processor Reference Manual*	
I^2C	SCL	CCB:SCL Software programmable	Table 5
L2 cache	CCB	CCB:SYSCLK	Table 2
Local bus controller	LCLK	CCB:LCLK Software programmable	Table 2, Table 7
PCI bus	SYSCLK	Not relevant	See Table 2 for relationship with CCB
PIC timers	Timer clock	Timer clock:SYSCLK Software programmable	Table 9
RapidIO	RIO_TCK	Not relevant	Table 2, Table 10

2 CCB Clock Generation

The MPC8540 takes in the PCI_CLK/SYSCLK signal as an input to the device PLL and multiplies it by an integer between 1–16 to generate the CCB clock signal. This CCB clock is the same frequency as the DDR DRAM data rate, for example, 266 MHz or 333 MHz. The L2 cache also operates at this frequency. When the PCI/PCI-X interface is used, SYSCLK also functions as the PCI_CLK signal when the MPC8540 is in agent mode or host mode; the MPC8540 does not provide a separate PCI_CLK output in host mode.

There is no default configuration PLL for the CCB to SYSCLK ratio; reset configuration signals must be pulled to the desired values to select the PLL ratio. For the available speeds of the MPC8540, consult the *MPC8540 Preliminary Hardware Specifications*. The relationship between the PLL configuration signal values and the ratio of the CCB clock to the SYSCLK is shown in Table 2.

Table 2. CCB Clock PLL Ratio

Functional Pins Used as PLL Reset Configuration Signals	Value (binary)	Ratio (CCB clock: SYSCLK)
LA[28:31] (No default)	0000	16:1
	0001	Reserved
	0010	2:1
	0011	3:1
	0100	4:1
	0101	5:1
	0110	6:1
	0111	Reserved
	1000	8:1
	1001	9:1
	1010	10:1
	1011	Reserved
	1100	12:1
	1101	Reserved
	1110	Reserved
	1111	Reserved

The following sections summarize the clocking requirements for the functional blocks of the MPC8540.

2.1 Dual Universal Asynchronous Receiver/Transmitters (DUART)

Each UART is clocked by the CCB clock, but each UART also contains an independent programmable baud-rate generator (BRG). Each UART can take the clock input and divide it by any divisor from 1 to 2^{16} – 1. The output frequency of the BRG is 16 times the baud rate. Therefore, the baud rate = (1/16) × (CCB frequency/divisor value). For details, see the DUART chapter of the *MPC8540 PowerQUICC III Host Processor Reference Manual*.

2.2 e500 Core PLL Ratio

The e500 core uses the CCB clock as an input to its PLL, which multiplies it by 2, 2.5, 3, or 3.5 to generate the e500 core clock. The core PLL reset configuration inputs establish the clock ratio between the e500 CCB and the e500 core clock. There is no default for this PLL ratio; these signals must be pulled to the desired values. Table 3 shows the PLL ratios between the e500 core and the CCB clock on the MPC8540.

Table 3. e500 Core PLL Ratio

Functional Pins Used as Core PLL Configuration Signals	Value (Binary)	Ratio (e500 Core:CCB)
LALE, LGPL2 (No default)	00	2:1
	01	5:2
	10	3:1
	11	7:2

2.3 Ethernet Clocks

The three-speed Ethernet controllers (TSECs) contain several clock domains that are asynchronous to each other, including the receive clocks, the transmit clocks, and the host clock. Each TSEC synchronizes data transfers to the CCB clock. In 10/100 mode, the Ethernet blocks use receive and transmit clocks supplied by the chips of the physical layer transceiver device (PHY device), and the media-independent interface (MII) uses the management data clock (MDC) generated by TSEC1. TSEC1 is the master of the MII management interface and is used to configure all PHYs (10/100 Ethernet, or TSEC PHYs).

The CCB clock is divided by eight to form a clock that is further divided by 4, 6, 8, 10, 14, 20, or 28 to form the Ethernet controller management data clock (EC_MDC at 12.5 MHz maximum frequency). Register-based programmable dividers allow the user to control the value of EC_MDC. In 1 Gbps mode, the PHY supplies the receive clock (TSEC*n*_RX_CLK), but the applicable TSEC generates the transmit clock (TSEC*n*_GTX_CLK). In 1 Gbps ten base interface (TBI) mode, the PHY supplies the receive clocks, which are two 180 degrees out-of-phase 62.5-MHz clocks. For TBI mode, the TSEC*n*_TX_CLK pin supplies the physical medium attachment (PMA) receive clock 1 input, and the TSEC*n*_RX_CLK pin supplies the PMA receive clock 0. The TSEC generates the 1 Gbps TBI transmit clock, TSEC*n*_GTX_CLK. To generate the transmit clocks in these GMII and TBI gigabit protocol modes, the TSEC requires a 125 MHz (+/– 6250 Hz) free-running clock externally sourced by the EC_GTX_CLK125 pin.

The TSEC also supports the reduced gigabit MII (RGMII) and reduced 10-bit interface (RTBI). In reduced pin mode, data and control signals are multiplexed, and both edges of the clock are used. For RGMII 1 Gbps, the TSEC*n*_GTX_CLK operates at 125 MHz, and for RGMII 10/100 the clock is reduced to 2.5 MHz or 25 MHz, respectively. TBI and RTBI operate only at 1 Gbps. For details, see the *MPC8540 PowerQUICC III Host Processor Reference Manual*.

Table 4 shows the EC_MDC-to-CCB (EC_MDC:CCB) clock ratios on the MPC8540. The ratio can be changed by writing to the MII management configuration register (MIIMCFG) on TSEC1.

Table 4. EC_MDC to CCB Ratio

MIIMCFG[29:31]	Ratio (EC_MDC:CCB)
000	1:(4*8)
001	1:(4*8)
010	1:(6*8)

Table 4. EC_MDC to CCB Ratio (continued)

MIIMCFG[29:31]	Ratio (EC_MDC:CCB)
011	1:(8*8)
100	1:(10*8)
101	1:(14*8)
110	1:(20*8)
111	1:(28*8)

2.4 I²C Bus

The inter-integrated circuit (IIC or I²C) bus is a two-wire, bidirectional serial bus that provides a simple and efficient method of data exchange between the system and other devices, such as microcontrollers, EEPROMs, real-time clock devices, A/D converters, and LCDs. The two-wire bus, composed of serial data (SDA) and serial clock (SCL), minimizes the interconnections between devices. The I²C interface uses the SDA and SCL signals for data transfer. The frequency of the serial clock is determined by the ratio relationship between the CCB clock and the serial clock. This ratio depends on the value of bits 2–7 of the I²C frequency divider register (I2CFDR). For details, see the *MPC8540 PowerQUICC III Host Processor Reference Manual.*

Table 5 describes the function of the bits to determine the frequency divider ratio (FDR). For details on the decimal number assigned to the hexadecimal equivalent of each FDR value, consult the *MPC8540 PowerQUICC III Host Processor Reference Manual*. Note that the digital filter sampling rate also affects the frequency divider of the I²C controller, as described in application note AN2919, *Determining the I²C Frequency Divider Ratio for SCL on the MPC8245 and MPC8241*. This application note discusses how to calculate the frequency divider for various sampling clocks per the I²C digital filter sampling register.

Table 5. Bits 2–7 of I²C Frequency Divider Register

2–7	FDR	Frequency divider ratio. Used to prescale the clock for bit rate selection. The serial bit clock frequency of SCL is equal to the CCB clock divided by the divider. The frequency divider value can be changed at any point in a program. This six-bit field is represented in hexadecimal in Table 6.

NOTE

The value of the FDR determines the divider used to calculate the serial clock (SCL) from the CCB clock. There are 64 divider choices available to determine the SCL using bits 2–7 of the I2CFDR.

Table 6. Serial Bit Clock Frequency Divider Selections

FDR	Divider (decimal)	FDR	Divider (decimal)
0x00	384	0x20	256
0x01	416	0x21	288
0x02	480	0x22	320

Table 6. Serial Bit Clock Frequency Divider Selections (continued)

FDR	Divider (decimal)	FDR	Divider (decimal)
0x03	576	0x23	352
0x04	640	0x24	384
0x05	704	0x25	448
0x06	832	0x26	512
0x07	1024	0x27	576
0x08	1152	0x28	640
0x09	1280	0x29	768
0x0A	1536	0x2A	896
0x0B	1920	0x2B	1024
0x0C	2304	0x2C	1280
0x0D	2560	0x2D	1536
0x0E	3072	0x2E	1792
0x0F	3840	0x2F	2048
0x10	4608	0x30	2560
0x11	5120	0x31	3072
0x12	6144	0x32	3584
0x13	7680	0x33	4096
0x14	9216	0x34	5120
0x15	10240	0x35	6144
0x16	12288	0x36	7168
0x17	15360	0x37	8192
0x18	18432	0x38	10240
0x19	20480	0x39	12288
0x1A	24576	0x3A	14336
0x1B	30720	0x3B	16384
0x1C	36864	0x3C	20480
0x1D	40960	0x3D	24576
0x1E	49152	0x3E	28672
0x1F	61440	0x3F	32768

2.5 Local Bus Controller (LBC)

The local bus controller clock generator performs the following functions:

- Generates the local bus clock signal, LCLK, for use by external devices.
- Produces a bus clock ready signal that asserts when the bus clock is stable and allows the LBC to start processing read and write transactions

The LBC supports ratios of 2, 4, and 8 between the faster CCB speed and the slower external bus clock (LCLK[0:2]). This ratio is software-programmable through the clock ratio register (LCRR[CLKDIV]). In addition to setting the frequency of the LCLK outputs, the LCRR[CLKDIV] ratio affects the resolution of signal timing shifts in general-purpose chip-select machine (GPCM) mode and the interpretation of user-programmable machine (UPM) array words in UPM mode. The bus clock is driven identically onto pins LCLK[0], LCLK[1], and LCLK[2] so the clock load can be shared equally across three signal nets, thereby enhancing the edge rates of the bus clock. Bits 28–31 of the clock ratio register (LCCR) set the ratio between the CCB clock frequency and the LBC bus frequency.

Table 7 shows the bit assignments for the various ratios between the SYSCLK and the clock of the local bus controller interface.

Table 7. Bits 28–31 of Clock Ratio Register—LCCR

28–31	CLKDIV	Platform/CCB to local bus clock divider. Sets the frequency ratio between the CCB clock and the memory bus clock of the local bus controller. Only the values shown here are allowed: 0000 Reserved 0001 Reserved 0010 2 0011 Reserved 0100 4 0101 Reserved 0110 Reserved 0111 Reserved 1000 8 1001–1111 Reserved

DLLs in the local bus memory controller generate memory clocks. Three clock outputs are generated for the local bus controller. They are available through signals LCLK[0:2].

In normal operation, the DLL is enabled by keeping the LCRR[DBYP] cleared (default following reset). The local bus clock monitors whether the DLL has locked properly and the bus clock to external devices is stable. The bus clock is considered unavailable under any of the following conditions:

- Hardware reset is asserted.
- The LBCR[LDIS] bit is set.
- The DLL lock counter restarts due to a sudden change in bus clock frequency (for example, the LCRR[CLKDIV] bit changes) or a change in system power saving mode.
- The global system clock stops.

Conversely, the bus clock is considered available when the DLL lock timer successfully expires and the DLL is not in bypass mode. This condition may take up to two, four, or eight bus clock cycles, depending on the clock division ratio, after the DLL lock counter is restarted.

2.6 Memory Bus and Data Rate

DLLs in the DDR SDRAM controller generate memory clocks. Six differential clock pairs are generated for DDR SDRAMs (MCK[0:5], $\overline{\text{MCK}}$[0:5]). DDR SDRAM devices support data transfers on both the rising and falling edge of each clock cycle. Thus, the memory bus speed is doubled for DDR SDRAM. Since the memory bus speed of regular SDRAM is half that of the CCB, the DDR rate is equivalent to that of the CCB speed. For the MPC8540, the memory bus speed increases to 166 MHz.

2.7 Programmable Interrupt Controller Timer Frequency

The programmable interrupt controller (PIC) is compliant with the OpenPIC architecture. The interrupt controller provides interrupt management and receives hardware-generated interrupts from different sources (both internal and external), prioritizes them, and delivers them to the e500 core for servicing. A series of timers in the PIC operate at the timer frequency. The source of this frequency is determined by bit 15 of the timer clock register (TCR[RTM]) and can be either the CCB clock or the real-time clock. Table describes the functionality of bit 15. Bits 22 and 23 of the timer clock register (TCR[CLKR]) define the ratio relationship between the timer frequency and SYSCLK. Table 9 lists the ratio relationship between the timer frequency and the CCB clock.

Table 8. Bit 15 of Timer Clock Register

15	RTM	Real-time mode. Specifies the clock source for the PIC timers. 0 Timer clock frequency is a ratio of the frequency of the platform (CCB) clock as determined by the CLKR field. This is the default value. 1 The RTC signal clocks the PIC timers. If this bit is set, the CLKR field has no meaning.

Table 9. Bits 22–23 of Timer Clock Register

22–23	CLKR	Clock ratio. Specifies the ratio of the timer frequency to the CCB clock. The following clock ratios are supported: 00 Default. Divide CCB speed by 8. 01 Divide CCB speed by 16. 10 Divide CCB speed by 32. 11 Divide CCB speed by 64.

2.8 Real-Time Clock

RTC is optionally used to clock the e500 time base unit by setting HID0[SEL_TBCLK]. The TBCLK input to the e500 is the RTC input to the MPC8540. The RTC input frequency must be no more than half the frequency of the SYSCLK input.

2.9 RapidIO Transmit Clock Source

The RapidIO transmit clock is sourced from one of three locations: the CCB clock, the RapidIO receive clock, or a low voltage differential signalling (LVDS) clock input. The RapidIO interface can operate at a continuum of frequencies of up to 1 Gbps per pin rate. Because RapidIO is a double data rate interface, 1 Gbps per pin rate represents a bus clock frequency of up to 500 MHz. The LGPL0 and LGPL1 reset configuration signals specify the source for the RapidIO transmit clock. They are referred to as cfg_rio_clk[0:1] in Figure 3.

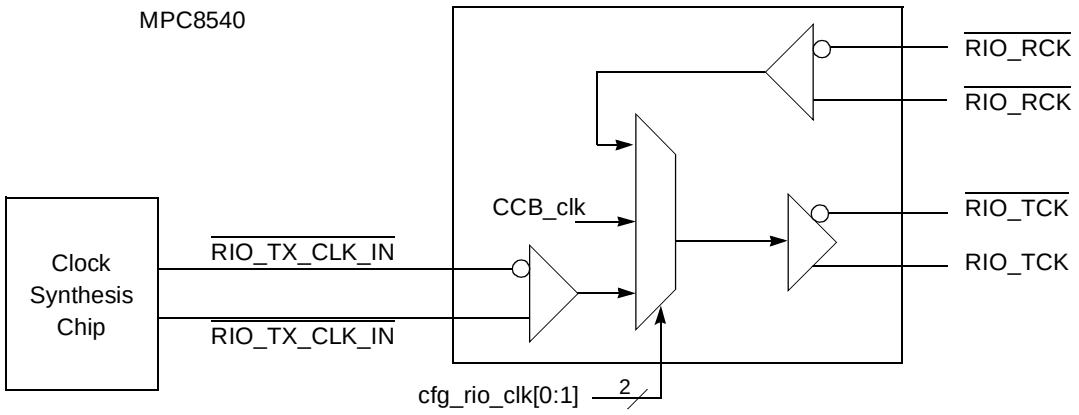

Figure 3. RapidIO Transmit Clock Options

Table 10 shows the signal settings that determine the source of the RapidIO transmit clock.

Table 10. RapidIO Transmit Clock Source

Functional Signals	Reset Configuration Name	Value (Binary)	Source of the Transmit Clock
LGPL0, LGPL1 (Default -11)	cfg_rio_clk[0:1]	00	Reserved.
		01	RapidIO receive clock.
		10	RapidIO transmit clock input (RIO_TX_CLK_IN).
		11	CCB clock (default).

3 Conclusion

The MPC8540 integrated PowerPC processor has several internal peripheral blocks that operate at different clock speeds, with guidelines to determine the desired frequency of each. These guidelines, as well as the timing specifications in the *MPC8540 Preliminary Hardware Specifications*, help maintain the optimal functionality of the device. The main clocks are the SYSCLK, the CCB clock, and the e500 core clock. All other clocks are linked to these clocks. For the available speeds of the MPC8540 CCB, see the clocking section of the *MPC8540 Preliminary Hardware Specifications*.

4 Document Revision History

Table 11 provides a revision history for this application note.

Table 11. Document Revision History

Revision	Date	Substantive Change
1	2/2006	Updated template. Updated Section 2.4, "I2C Bus." to include reference to the AN2919 application note. Table 11 - Added a column for Date parameter.
0	11/2003	Initial release

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