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Application Note

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Single Phase Two-Channel Interleaved PFC Converter Using MC56F8006

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1 Preface

A power factor correction (PFC) system is commonly used in medium- or high-power power supply applications which require the ideal ohmic load character at the line input, low harmonic current injection into the line, and high efficiency. This would include such applications as an uninterrupted power supply (UPS), telecom power supply, motor drive inverter, and other power supplies for electronic equipment.

In many types of PFC topologies, the most popular topology for a PFC converter is the boost converter, because the boost converter has continuous input current that can be manipulated with an average-current-mode control technique to force the input current to track the changes in line voltage. Moreover, the interleaved boost PFC converter has many advantages in increasing power density, reducing input current ripple and RMS current of the boost capacitor, reducing filter volume, and cutting down the cost of materials.

Contents

The Freescale MC56F8006 is a cost-effective, low-power DSC product which meets the requirements of green power conversion based on all-digital control. This application note describes the implementation of a single-phase two-channel interleaved PFC converter based on the MC56F8006 device, and provides a reference for customers who require cost-effective and high performance/price ratio solutions.

This document includes target control theory, system design concept, hardware design, and software design.

2 MC56F8006 DSC Advantages and Features

The MC56F8006 combines, on a single chip, the processing power of a digital signal processor (DSP) and the functionality of a microcontroller unit (MCU) with a set of flexible peripherals to create low-cost and high-performance/price solutions.

The MC56F8006 uses the 56800E core, which is based on a dual Harvard-style architecture consisting of three execution units operating in parallel. This allows as many as six operations per instruction cycle. The MCU-style programming model and optimized instruction set allow straightforward generation of efficient, compact DSP and control code. The instruction set is also highly efficient for C compilers to enable rapid development of optimized control applications.

Because of its low cost and flexible peripherals configuration, the MC56F8006 is well-suited for many cost-effective and low-power-consumption applications such as digital switching mode power supplies, motor control, medical devices, power metering, handheld tools, etc.

The MC56F8006 provides the following peripherals:

- One six-channel output pulse width modulator (PWM) with up to 96 MHz operating clock, three current-sense inputs, and up to four fault inputs; fault-tolerant design with dead-time insertion, supporting both center- and edge-aligned modes
- Two analog-to-digital converters (ADCs), supporting two simultaneous conversions and ping-pong conversion with dual 24 inputs, 8-bit, 10-bit, and 12-bit output format, low-power operation; the ADC can be synchronized by PWM module; a temperature sensor is integrated with each ADC
- Two programmable gain amplifiers (PGA) with programmable gains up to a maximum of 32, supporting conversion of analog signals from differential to single-ended samples which can be synchronized with PWM, and calibration features of both offset and gain
- Two 16-bit general purpose timers (GPT) with up to 96 MHz operating clock, supporting up to 12 operating modes
- One programmable delay block (PDB), providing precise control of PGA/ADC and HSCMP sample time relative to PWM synchronization output
- One programmable interval timer (PIT) for timing; one real-time counter (RTC), supporting real-time clock and waking the core from low power mode
- Three high-speed comparators (HSCMP), supporting sample, window, and digital filters
- One serial communication interface (SCI) with up to 6 Mbps baud rate, supporting full-duplex, single-wire, and LIN slave modes

- One serial peripheral interface (SPI), supporting full-duplex operation, programmable length transactions from 2 to 16, and 12 master mode frequencies
- One inter-integrated circuit (IIC), supporting 10-bit address extension, general call recognition, and SMBus specification
- Power management controller (PMC), supporting seven power modes including ultra low power mode — partial power down mode
- Computer operating properly (COP) timer with independent 1 kHz on-chip oscillator, supporting operation in low power mode
- Up to 40 GPIO lines
- Two internal voltage regulators (VR) for core and clock; internal power-on reset (POR) circuit and low voltage interrupt (LVI) module
- Software-programmable phase-locked loop (PLL)
- JTAG/Enhanced On-Chip Emulation (EOnCE) for real-time debugging
- Cost-effective memory configuration (16 KB program flash, 2 KB program dual-port RAM)

The interleaved PFC system mainly benefits from the flexible PWM module, PDB/PGA/ADC, GPT module, and HSCMP module.

The PWM module offers flexibility in its configuration, enabling efficient two-channel interleaved PFC control. It has the following features:

- Three complementary PWM signal pairs, or six independent PWM signals
- Complementary channel operation:
  - Independent top and bottom deadtime insertion
  - Separate top and bottom pulse width correction via current status inputs or software
  - Separate top and bottom polarity control
- Edge-aligned or center-aligned PWM signals
- 15 bits of resolution
- Half-cycle reload capability
- Integral reload rates from 1 to 16
- Individual software-controlled PWM output
- Mask and swap of PWM outputs
- Programmable fault protection
- Polarity control
- 10/16 mA current source/sink capability on PWM pins
- Write-protected registers
- Option to supply the source for each complementary PWM signal pair from any of the following:
  - External digital pin
  - Internal timer channel
  - External ADC input, taking into account values set in ADC high and low limit registers

The single-phase two-channel interleaved PFC control system uses a PWM module set in the independent output mode, permitting the generation of two 180-degree phase-shifted PWM signals in center-aligned configuration for all power switches of the power stage. Also, the PWM reload SYNC signal is generated every half-cycle to provide synchronization with PDB/PGA/ADC modules for precise sample control of the ADC.

The ADC module consists of a digital control module and an analog sample/hold circuit, which offers low cost and low power. It has the following features:

- Input voltage values that may range from VSSA to VDDA
- Linear successive approximation algorithm with 12 bits resolution
- Up to 28 analog inputs
- Output formatted in 12-, 10-, or 8-bit right-justified format
- Single or continuous conversion (automatic return to idle after single conversion)
- Configurable sample time and conversion speed/power
- Conversion complete flag and interrupt
- Input clock selectable from up to four sources
- Operation in wait or stop mode for lower noise operation
- Asynchronous clock source for lower noise operation
- Selectable asynchronous hardware conversion trigger
- Temperature sensor integrated
- Can be configured to take two samples (with no software reconfiguration required) based on hardware triggers during ping-pong mode

The single-phase two-channel interleaved PFC control system uses two ADC modules set in single conversion and simultaneous sample mode for reducing the conversion time of the required analog signals. Each ADC operates in concert with the PGA for sensing small analog signals (currents) and differential analog signals (voltages). The trigger of the ADC is synchronized with the PWM for aligning converter analog signals within the required time.

The PGA module is useful for amplifying and converting differential signals to single-ended values when used to pre-process ADC inputs. It has the following features:

- Perform differential-to-single-ended conversion of analog signals
- Software and hardware triggers are available
- Power supply range: VDDA = 1.8 V to 3.6V
- Temperature range: –40 °C to 135 °C junction
- Input signal range: ground to VDDA
- Each PGA is designed to drive one 12-bit SAR converter input
- 1×, 2×, 4×, 8×, 16×, or 32× gain
- Integrated sample/hold circuit
- Correlated double sampling (CDS) in the Diff and Diff2SE gain stages:
  - Eliminates offset error associated with these circuits

  - Reduces 1/f noise
  - Sample/hold output can be over-sampled by the gain stages under software control
  - Automatic offset cancellation occurs during PGA startup
- Predictive CDS used in the S/H stage
- Includes additional calibration features
  - Offset calibration eliminates any errors in the internal reference used to generate the VDDA/2 output center point
  - Gain calibration can be used to verify the gain of the overall data path
  - Both features require software correction of the ADC result

The single-phase two-channel interleaved PFC control system uses two PGA modules to amplify currents (PFC1 inductance current, PFC2 inductance current, and total input current) and convert voltages (input voltage and DC bus voltage) respectively to improve the precision of ADC conversion results.

The PDB module primarily provides a controllable delay for trigger of PGA/ADC and a controllable sample/window for HSCMP to synchronize the time of a critical event. It has the following features:

- 16 bits of resolution with prescaler
- Positive transition of trigger_in will initiate the counter
- Support of two trigger_out signals — each has an independently controlled delay from sync_in
- Trigger outputs can be ORed together to schedule two conversions from one input trigger event
- Trigger outputs can be used to schedule precise edge placement for a pulse output; this feature is used to generate the control signal for the HSCMP windowing feature
- Continuous trigger or single shot mode supported
- Bypass mode supported
- Each trigger output is independently enabled

The single-phase two-channel interleaved PFC control system uses the PDB module to enable a delay of the A counter. This compensates for the delay of the hardware driver circuit for synchronizing the actual behavior of the power switch. At the same time, the PDB module is set in ORed trigger output mode to provide two identical triggers to support simultaneous conversion for two independent ADCs.

The GPT module is extremely flexible, providing all required services relative to time events. It has the following features:

- Four 16-bit counters/timers
- Count up/down
- Counters can be cascaded
- Programmable count modulo
- Max count rate equals peripheral clock/2 for external clocks
- Max count rate equals peripheral clock for internal clocks
- Count once or repeatedly
- Counters can be preloaded
- Compare registers can be preloaded

- Counters can share available input pins
- Separate prescaler for each counter
- Each counter has capture and compare capability
- Programmable operation during debug mode
- Inputs may act as fault inputs
- Programmable input filter
- Counting start can be synchronized across counters

The single-phase two-channel interleaved PFC control system uses a GPT module to capture the zero-cross time of input voltage for phase sensing. Another GPT module is set to generate a fixed-frequency PWM output for fan speed control.

The HSCMP module provides a circuit for comparing two analog input voltages. It has the following features:

- Operate over the entire supply range
- Inputs may range from rail to rail
- Less than 40 mV of input offset
- Less than 15 mV of hysteresis
- Selectable interrupt on rising edge, falling edge, or either rising or falling edge of comparator output
- Selectable inversion on comparator output
- Comparator output may be:
  - — Sampled
  - — Windowed
  - — Digitally filtered
    - – Filter can be bypassed
    - – May be clocked via external sample signal or scaled peripheral clock
- External hysteresis can be used at the same time that the output filter is used for internal functions
- The positive and minus inputs of the comparator are both driven from 4-to-1 muxes which allow additional flexibility in assigning GPIO as comparator inputs during PCB design
- Two software-selectable performance levels
  - — Shorter propagation delay at the expense of higher power — this mode can be used only if the VDDA rail is above the low voltage interrupt trip point
  - — Low power, with longer propagation delay

The single-phase two-channel interleaved PFC control system uses an HSCMP module to rectify the waveform of input voltage for GPT capture. A second HSCMP module is configured as over-voltage protection circuit for DC bus, and other HSCMP module is configured as an over-current protection circuit for total current.

3 Target Control Theory

Because the two channel boost PFC converters of single phase two-channel interleaved boost PFC converter are controlled independently in this application. This chapter will use the traditional single phase boost PFC converter to help understanding the control theory of interleaved boost PFC converter.

3.1 Single-Phase Boost PFC Converter

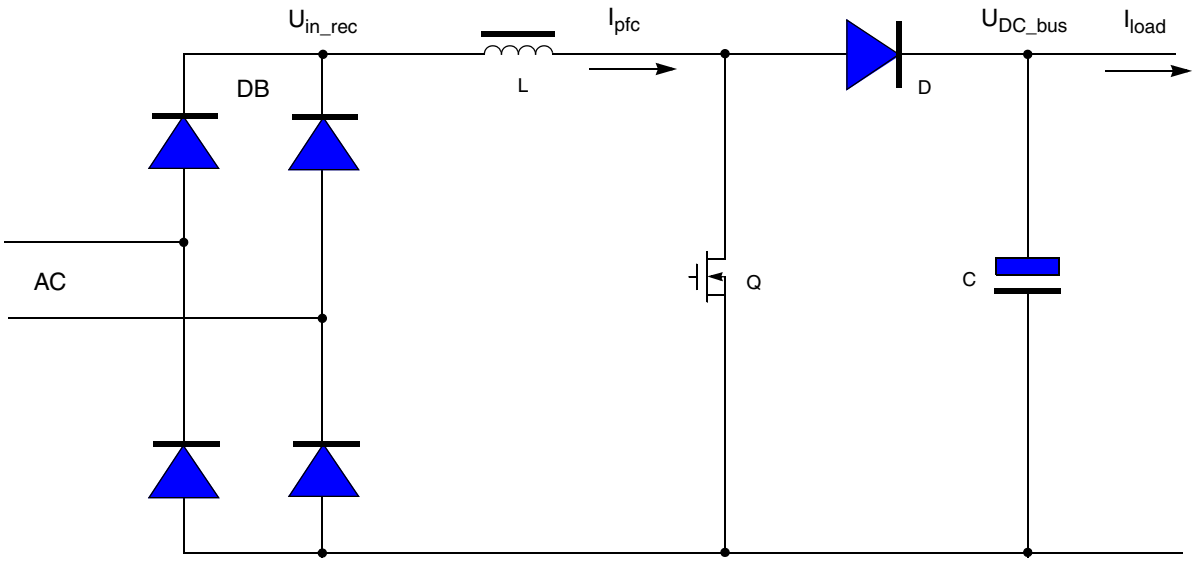

Figure 1. Single-Phase Boost PFC Converter Topology

The single-phase boost PFC converter incorporates an input diode bridge rectifier DB, PFC inductance L, PFC diode D, PFC switch Q and DC bus capacitor C (see Figure 1). The input current is controlled using the PFC switch to achieve the desired input current and the desired level for the DC bus voltage.

3.2 Mathematical Model of Boost PFC Converter

In a medium- or high-power application, the boost PFC converter is generally designed to operate in continuous current mode (CCM), so the mathematical model of the boost PFC converter is based on CCM.

According to the circuit diagram in Figure 1, the equivalent mathematical model of the boost PFC converter can be written as:

$$\begin{cases} U_{in\_rec} = RI_{pfc} + L\dfrac{dI_{pfc}}{dt} + S_Q U_{DC\_bus} \\ C\dfrac{dU_{DC\_bus}}{dt} = S_Q I_{pfc} - I_{load} \end{cases} \qquad \textit{Eqn. 1}$$

where:

U_{in_rec} corresponds to rectified input voltage

U_{DC_bus} corresponds to DC bus voltage

I_{pfc} corresponds to inductance current

I_{load} corresponds to load current

L corresponds to inductance value

R corresponds to equivalent resistance value of loop circuit

S_Q corresponds to switch function of power switch

$$S_Q = \begin{cases} 0 & on \\ 1 & off \end{cases}$$

Based on Equation 1, the control model of the boost PFC converter can be obtained as the following:

$$\begin{bmatrix} \dot{I}_{pfc} \\ \dot{U}_{DC\_bus} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & -\frac{S_Q}{L} \\ \frac{S_Q}{C} & 0 \end{bmatrix} \begin{bmatrix} I_{pfc} \\ U_{DC\_bus} \end{bmatrix} + \begin{bmatrix} \frac{1}{L} & 0 \\ 0 & -\frac{1}{C} \end{bmatrix} \begin{bmatrix} U_{in\_rec} \\ I_{load} \end{bmatrix} \quad \textit{Eqn. 2}$$

Equation 2 is a 2nd order control model for the boost PFC converter. Therefore the good performance of a boost PFC converter can be easily obtained through using only a simple and classical PID control algorithm.

3.3 Typical Control System Description

It is important for a designer to design a control system that has good steady-state and dynamic-state performance. To simultaneously solve the contradictory aspects of stability, accuracy, speed, and anti-jamming using classical correction methods, the designer needs to have a solid theoretical foundation and rich engineering experience. Most control systems for a switching mode power supply or for motor control can be approximately treated as a low-order control system, so an engineering design method for a typical control system is suitable for a designer who is a beginner or not a control expert.

The general control block diagram and open-loop transfer function of a single input/single output control system can be represented respectively as in Figure 2 and Equation 3.

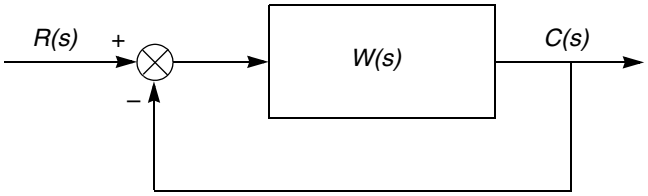

Figure 2. General Control Block Diagram

$$W(s) = \frac{K\prod_{j=1}^{m}(\tau_j s + 1)}{s^r \prod_{i=1}^{n}(T_i s + 1)}$$

Eqn. 3

For equation 3, the factor s^r in the denominator indicates that there are r poles on the origin. According to $r = 0,1,2...$, the control system is conventionally called a system of type 0, type I, type II....

For a type 0 system, automatic control theory proves that the system has bad steady-state precision. Also, systems of type III or higher exhibit bad system stability. Therefore, systems of type I and type II are recommended to use in engineering design to ensure good system stability and steady-state precision.

3.3.1 Type I System

The open-loop transfer function of a type I system is expressed as Equation 4.

$$W(s) = \frac{K}{s(Ts + 1)}$$

Eqn. 4

Where:

T corresponds to the inertia time constant of the control system

K corresponds to the open-loop gain of the control system

The open-loop logarithm frequency characteristics of a type I system are shown in Figure 3.

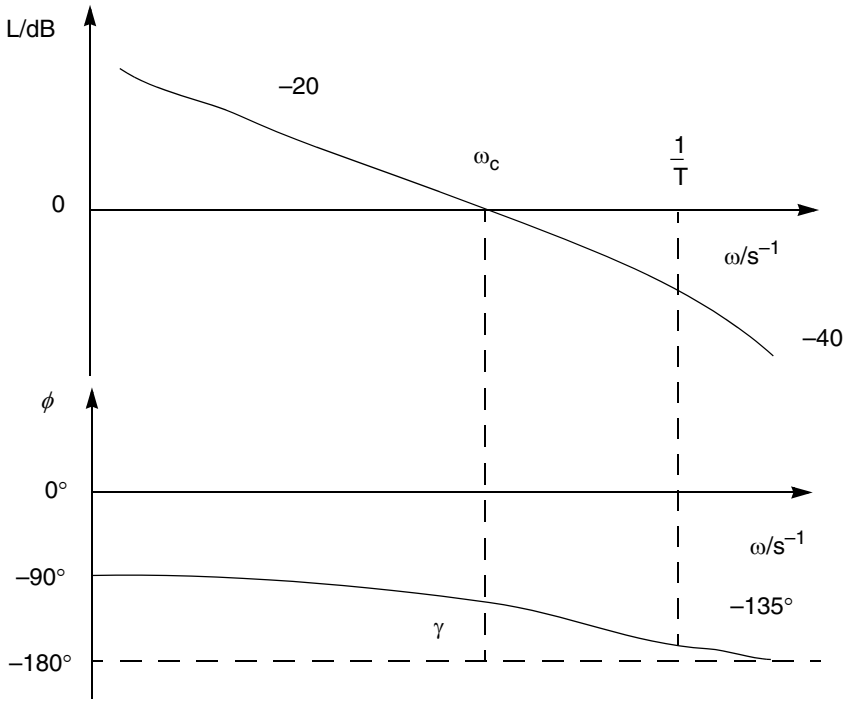

Figure 3. Bode Diagram of Type I System

According to Figure 3, as long as the control parameter is designed to ensure a wide enough medium-frequency band, the system is stable and has sufficient stability margin. So, the parameter must be designed to meet the following inequality:

$$\omega_c < \frac{1}{T}$$

Then, the phase angle margin is:

$$\gamma = 180^\circ - 90^\circ - \text{arctg}\omega_c T = 90^\circ - \text{arctg}\omega_c T > 45^\circ$$

According to results of control theory based on various inputs and disturbing signals, a type I system has better track performance but worse steady-state precision and anti-jamming performance compared with a type II system.

3.3.2 Type II System

The open-loop transfer function of a type II system is expressed as Equation 5.

$$W(s) = \frac{K(\tau s + 1)}{s^2(Ts + 1)} \qquad \textit{Eqn. 5}$$

Where:

T corresponds to the inertia time constant of the control system

τ corresponds to the proportional-differential time constant of the control system

K corresponds to the open-loop gain of the control system

The open-loop logarithm frequency characteristics of a type II system are shown in Figure 4.

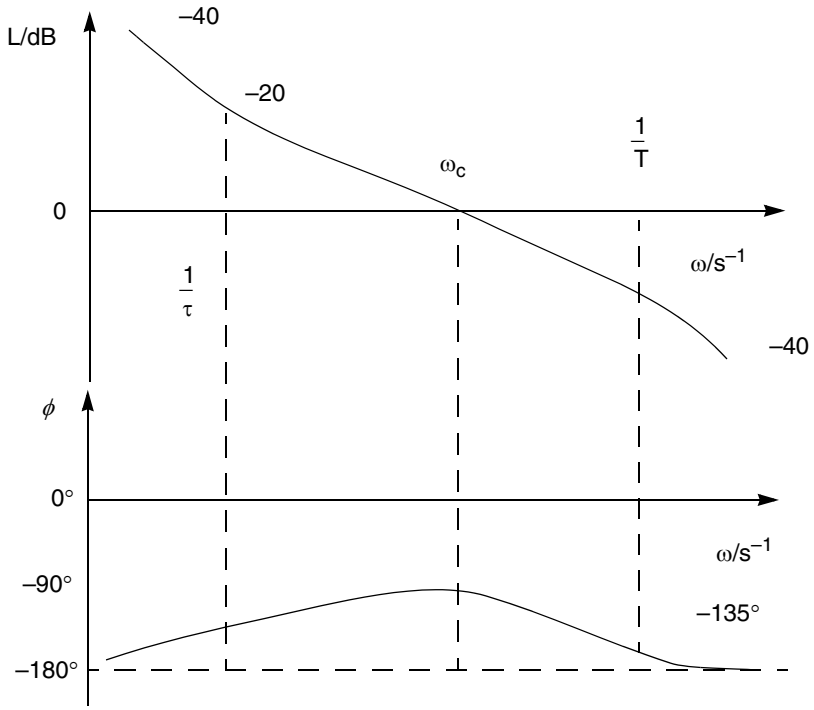

Figure 4. Bode Diagram of Type II System

According to Figure 4, to assure the system stability, the proportional-differential factor in the numerator of Equation 5 is used to lift the phase-frequency characteristics over the minus 180 degree level line. The width of medium frequency band *h* can be calculated with Equation 6.

$$h = \frac{1}{T} \Big/ \frac{1}{\tau} = \frac{\tau}{T} \qquad \textit{Eqn. 6}$$

So, the width of medium-frequency band *h* needs to be designed to assure enough system stability range. At the same time, to assure the stability of the system, the zero-cross frequency must be designed to meet the following inequality:

$$\frac{1}{\tau} < \omega_c < \frac{1}{T}$$

Then, the phase angle margin is:

$$0^\circ < \gamma = 180^\circ - 180^\circ + \text{arctg}\omega_c\tau - \text{arctg}\omega_c T < 90^\circ$$

Considering the stability margin and band width of system, the zero-cross frequency ω_c must be designed as a compromise with respect to system stability and speed.

Compared with a type I system, a type II system has better steady-state precision and anti-jamming performance but worse track performance based on various inputs and disturbing signals.

4 System Design Concept

4.1 System Architecture

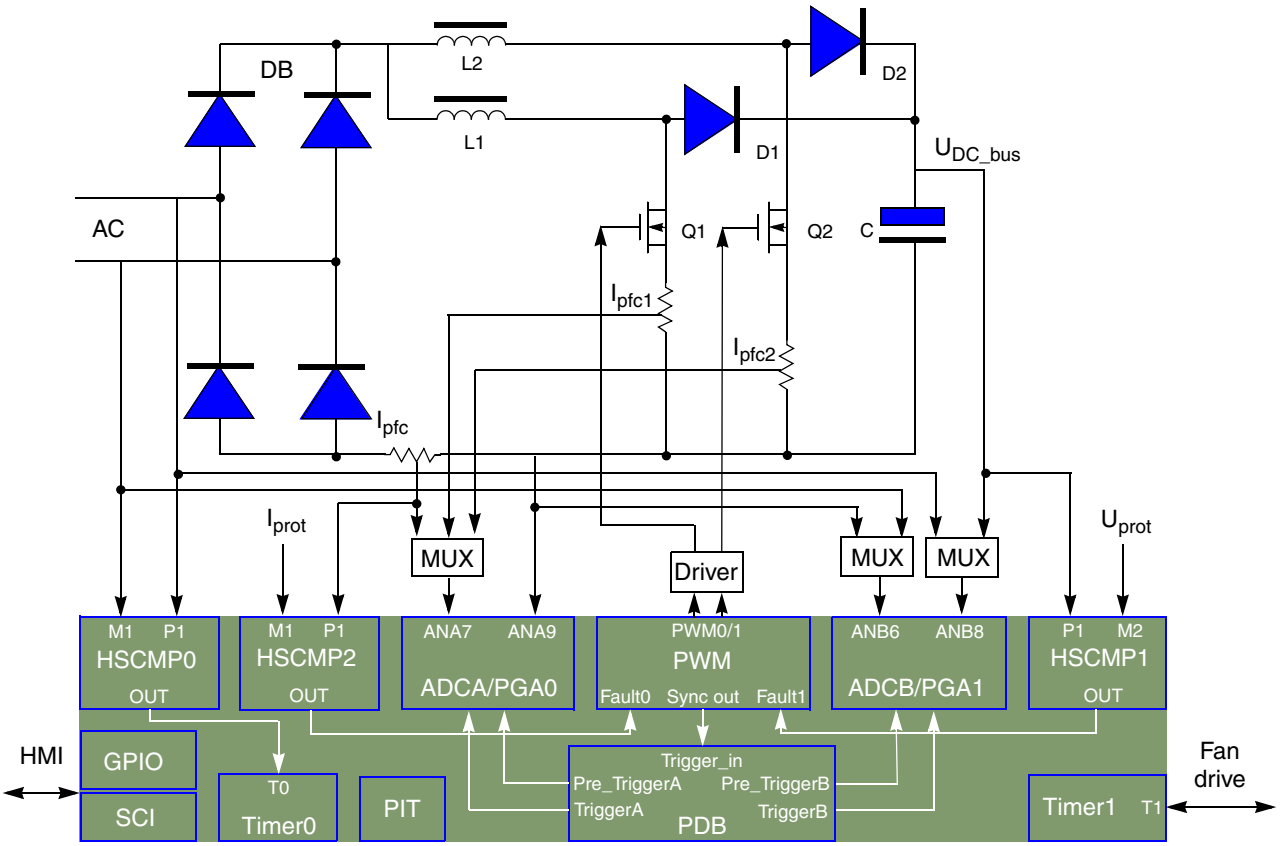

Figure 5. System Block Diagram for Single-Phase Two-Channel Interleaved Boost PFC

This application system incorporates the PFC high-voltage power stage, fan power stage, sensing stage, driver stage, auxiliary power supply stage, and control stage base on the MC56F8006, plus the human-machine interface stage (see Figure 7).

The PFC high-voltage power stage provides a high voltage/strong current route, which includes an input diode bridge rectifier DB, a two-channel interleaved boost PFC converter (each channel incorporating PFC inductance L, PFC diode D, and PFC switch Q) and a DC bus capacitor C.

The fan power stage provides the adjustable voltage output to power the fans, so that the speed of the fans can be adjusted according to the ambient temperature in the PFC converter.

The sensing stage is used to sense the required voltage and current signals and then condition these sensed signals to meet the requirements of the ADC input port.

The driver stage is used to isolate the high voltage/strong current stage from the low voltage/weak current stage, and amplify the PWM signal to drive the power switches in the power stage.

The auxiliary power supply stage is used to provide all types of stable power supply required by sensing, driver, control, and HMI stages.

In the MC56F8006 control stage, the PDB/PGA/ADC modules are used to convert the voltage, current, and temperature analog signals to accurate digital values synchronized with the PWM for system control and protection requirements. HSCMP0/Timer0 are used to capture the positive zero-cross time of the input voltage for the software phase-locked loop. HSCMP1 and HSCMP2 are used to judge the input over-current condition and DC bus over-voltage condition respectively, and protect the power stage through the flexible fault function of the PWM module. Timer1 is used to drive the power switch in fan power stage for fan speed regulation according to the sensed ambient temperature. The PIT is used to create a time base for timing sequence management. The SCI is used to communicate with a PC or other MCU; GPIOs are used to receive the button signals and indicate system information through LEDs.

The human-machine interface stage is used to receive external commands and indicate system information.

4.2 System Specification

This application meets the following performance specifications:

- Hardware used:
  - MC56F8006 control board
  - PFC board integrated with power, sensing, driver, auxiliary power supply, and HMI interface stages (230 V/50 Hz nominal input voltage, 360 V nominal DC bus voltage and 1 kW nominal power output)
- Control technique incorporates:
  - Inner inductance current loop (12.5 kHz control frequency, 25 kHz switching frequency)
  - Outer DC bus voltage loop (12.5 kHz control frequency)
  - Input voltage software phase-locked loop (50 Hz control frequency)
  - Reference current generation
  - Fan speed control
  - Input over- and under-voltage process
- Manual interface and monitor:
  - Power switch
  - LEDs for system information
- FreeMASTER software monitor:
  - FreeMASTER software graphical control page (required output voltage, actual output voltage, actual input current, actual input voltage control, and system status)
  - FreeMASTER software voltage scope (observe input voltage, output voltage, input current, duty cycle, and RMS input voltage)
- Fault protection:
  - DC bus over-voltage
  - System over-current

— Input over-voltage and under-voltage

4.3 System Control Process

Because the two PFC converter channels are independently controlled in this application, the control scheme may be designed according to a traditional single-channel PFC converter. The function of the PFC converter is to control the input current to get the ideal input power factor, and provide the required stable level of DC bus voltage for the load. At the same time, to obtain excellent steady- and dynamic-state performance, it is recommended to use the control scheme of an outer DC bus voltage and inner inductance current loop system.

The inner inductance current loop is meant to:

- control the system input current to closely follow the reference current
- accelerate the dynamic process by providing permitted maximum current output if the outer DC bus voltage loop is in a dynamic process
- provide a timely anti-jamming function against line fluctuation

So, to achieve the best possible functioning of the inner inductance current loop, you should use a PI regulator and design the inner inductance current loop as a type I system. Also, to improve the anti-jamming performance against line fluctuation for the inner inductance current loop, the rectified input voltage is added into the inner inductance current loop as the feed-forward, which has been proved feasible from Equation 2.

The outer DC bus voltage loop is meant to:

- control the DC bus voltage to quickly follow the change of reference voltage and implement non-error control in steady state
- determine the permitted maximum current output through limiting the voltage regulator output
- provide a timely anti-jamming function against the change of load

So, to achieve the best possible functioning of the outer DC bus voltage loop, you should use a PI regulator and design the outer DC bus voltage loop as a type II system.

Figure 6 shows the system control scheme of a single-phase two-channel interleaved boost PFC converter. The control system has an outer loop of DC bus voltage regulation, a phase-locked loop of input voltage, and two independent inner loops of inductance current regulation for the two-channel interleaved PFC converter. When the start command is accepted, the reference DC bus voltage is calculated through a ramp according to the required DC bus voltage. The comparison between the reference DC bus voltage and the actual measured DC bus voltage generates a DC bus voltage error. Based on the error, the DC bus voltage regulator generates the amplitude of the total reference inductance current. Simultaneously, the PLL of the input voltage generates the phase of the total reference inductance current. Combining the two outputs of the DC bus voltage regulator and the PLL of the input voltage, the total reference inductance current can be obtained. In order to share the total inductance current by the two interleaved channel boost PFC converters, the reference inductance current of each channel boost PFC converter can be calculated through dividing the total reference inductance current by two. Based on the error between the reference inductance current and the actual inductance current of each channel boost PFC converter, the inductance current regulators will generate output voltages. Combining the feed-forward of the rectified input voltage

and the output voltages of the inductance current regulators, the modulating voltage can be obtained separately for each channel PWM modulator.

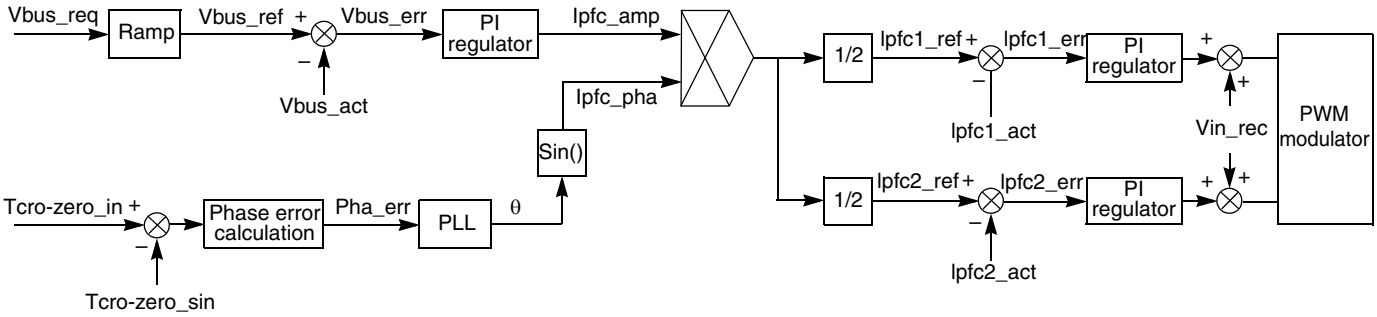

Figure 6. System Control Scheme of Single-Phase Two-Channel Interleaved Boost PFC Converter

Besides processing the main control loop, the total input current and ambient temperature are measured, and the RMS input voltage is calculated during the control process. This information is then used to protect the power stage from over-voltage, under-voltage, over-current, and/or over-temperature conditions.

5 Hardware Design

5.1 System Hardware Structure

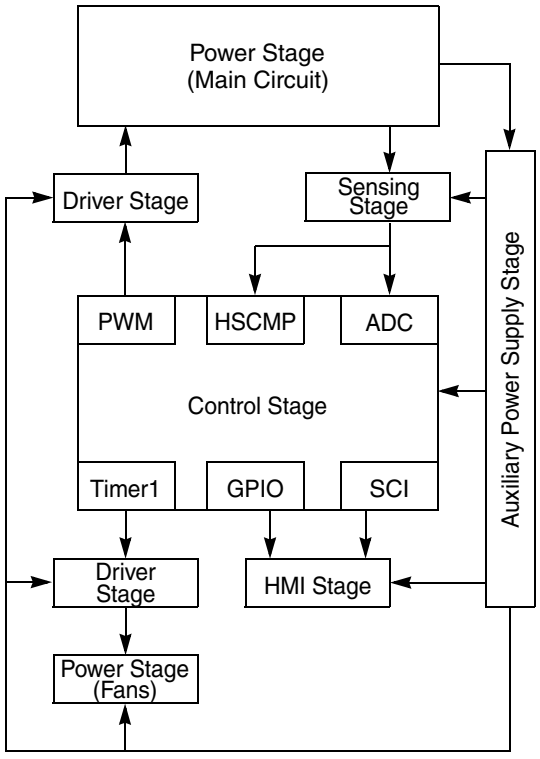

Figure 7. System Hardware Structure Block Diagram

The hardware structure of the single-phase two-channel interleaved boost PFC converter system is shown in Figure 7. The hardware system comprises an MC56F8006 control stage (control board), power stage, sensing stage, driver stage, auxiliary power supply stage, and HMI interface stage (PFC board).

5.2 MC56F8006 Control Board

The system described in this document uses the small MC56F8006-based system that includes the MC56F8006 DSC, JTAG interface, manual reset circuit, and pin interface.

5.3 PFC Board

5.3.1 Main Power Circuit

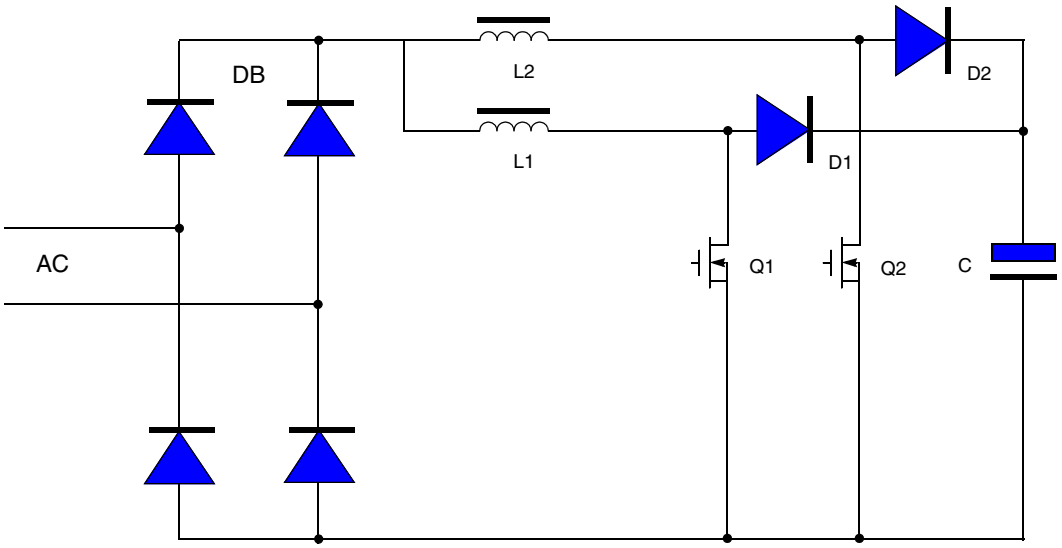

Figure 8. Main Power Topology Circuit

The PFC main power circuit incorporates an input diode bridge rectifier DB, two-channel interleaved boost PFC converter (each channel incorporates PFC inductance L, PFC diode D and PFC switch Q) and DC bus capacitor C.

5.3.1.1 Design of the Input Diode Bridge Rectifier

The input diode bridge rectifier selection is based on reverse voltage and forward current. Considering the low input voltage and overload requirements, a diode bridge rectifier with continuous forward current of 10 A and reverse voltage of 600 V is suitable in this application.

5.3.1.2 Design of the PFC Inductance

It is critical to select a suitable core for inductance design, because the core determines the inductance value per turn based on magnetic circuit and the permitted maximum inductance value based on dimension.

The required PFC inductance value can be calculated using the following formula.

$$L = \frac{\sqrt{2} \cdot V_{in} \cdot D}{f_s \cdot \Delta i} \qquad \textit{Eqn. 7}$$

Where:

V_{in} corresponds to input voltage RMS value

D corresponds to duty cycle

f_s corresponds to switching frequency

Δ_i corresponds to inductance current ripple

Based on the selected core and inductance value, it is possible to determine the number of turns in the windings. At the same time, the cross-sectional area of the winding can be calculated according to the maximum inductance current and suitable current density. After the number of turns and cross-section area are determined, the window coefficient of the core can be calculated to verify the feasibility of the selected core.

5.3.1.3 Design of the PFC Switch

To design the power switch, this application selects the following method to calculate an equivalent flat-topped current.

$$I_{pft} = \frac{D_{\max}}{\eta} \cdot \frac{P_{out}/2}{V_{\min(REC)}} \qquad \textit{Eqn. 8}$$

Where:

P_{out} corresponds to nominal output power

$V_{min(REC)}$ corresponds to minimum rectified input voltage RMS value

D_{max} corresponds to maximum duty cycle

η corresponds to converter efficiency

The reverse voltage and loss must be considered as well. For this application, a power switch with 600 V reverse voltage is suitable, and the low $r_{ds(on)}$ value is selected to reduce the conduction loss and improve the whole converter efficiency.

5.3.1.4 Design of the PFC Diode

The PFC diode selection is based on reverse voltage, forward current, and switching speed. The PFC diode selection in this design is critical, and it is important to use a diode with a fast recovery characteristic.

5.3.1.5 Design of the DC Bus Capacitor

The DC bus capacitor is needed to meet the requirement of hold time for load first when the line input powers down. The RMS current ripple and voltage level also need to be considered. An electrolytic capacitor of 470 µF / 450 V is suitable for this application.

5.3.2 Fan Power Circuit

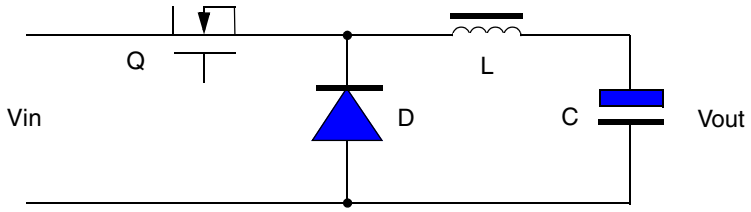

Figure 9. Fan Power Topology Circuit

The fan power circuit uses the buck topology, which is controlled in open-loop mode, to provide the adjustable voltage output to the fans. In this way, the speed of the fans can be adjusted according to the ambient temperature in the PFC converter. The input of the fan power circuit is derived from the auxiliary power supply.

5.3.3 Sensing Circuit and Driver Circuit

The sensing circuit is used to convert the high voltage and strong current signals into low voltage signals, and then to condition these sensed signals to meet the requirements of the ADC input port. All sensing circuits comprise a follower circuit and a clamp circuit in this application, except for the input voltage sensing circuit, where a bias circuit is added to transform the AC signal into a DC signal.

The power switches are driven using driver IR2121. This driver has current detection and a limiting loop to limit the driven power switch current. The protection circuit detects over-current in the driven power switch and limits the gate drive voltage. Cycle-by-cycle shutdown is programmed by an external capacitor, which directly controls the time interval between detection of the over-current limiting condition and the latched shutdown.

5.3.4 Auxiliary Power Supply Circuit

The auxiliary power supply uses flyback topology. This approach has many inherent advantages such as wide operating voltage range, isolation structure between primary side and secondary side, and multi-output support. The auxiliary power supply provides four outputs: one +24 V DC, one +15 V DC, one –15 V DC, and one +5 V DC for all hardware stages. The other voltage levels (such as +3.3 V DC) are all derived from the four group voltage levels.

5.3.5 Human Machine Interface Circuit

An SCI interface is provided to communicate with a PC. Through the FreeMaster application software, the PC can set commands to change the system status and receive system feedback information to monitor the system operation.

Also, a power switch is provided to power on or shut down the converter through a GPIO input, and LED indicators are provided to indicate the system status through GPIO outputs.

6 Software Design

6.1 System Software Organization

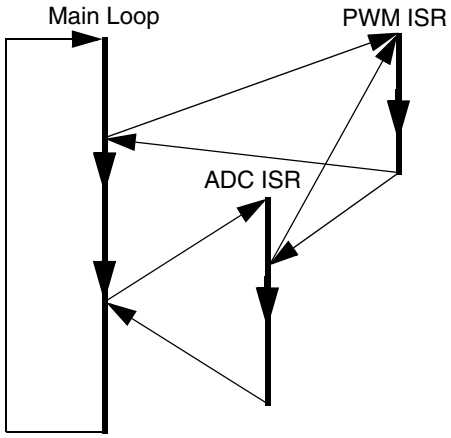

Figure 10. System Software Framework Diagram

As shown in Figure 10, the software of this application mainly contains three threads:

- The Main loop thread
- The ADC ISR thread
- The PWM ISR thread

Additionally, there are system clock initialization, CPU initialization, peripheral initialization, and variable initialization routines. These ensure that the software runs correctly before the Main loop.

6.2 Main Loop Description

After a processor reset, the Main loop thread performs the following tasks:

- System set up:
  - Clock
  - COP
  - Core
  - ADC
  - PGA

  - PDB
  - HSCMP
  - Timer
  - PWM
  - SCI
  - GPIO
- Initialization of variables
- Interrupt source selection and enabling
- Time base management
- SCI communication processing
- Run/stop control
- Data processing
- Fault management
- LED indication control

The flowchart of the Main loop thread is shown in Figure 11.

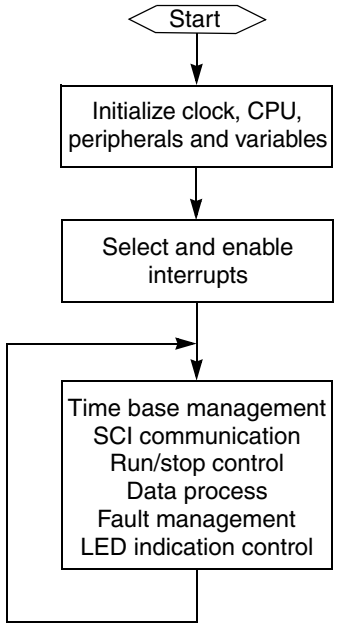

Figure 11. Main Loop Flowchart

6.3 ADC ISR Description

The ADC interrupt thread performs the entire single-phase two-channel interleaved PFC algorithm and fan speed regulation control. These tasks are:

- Sense the input voltage, PFC1 inductance current, PFC2 inductance current, DC bus voltage, PFC input current, and PFC ambient temperature
- DC bus voltage control (PI regulation)

- Phase-locked loop control of input voltage (PI regulation)
- Reference inductance current generation
- PFC1 inductance current control (PI regulation)
- PFC1 PWM generation
- PFC2 inductance current control (PI regulation)
- PFC2 PWM generation
- Fan speed control
- PFC input current process

To achieve better control system performance, the ADC interrupt service routine (ISR) is divided into four groups in this application. The ADC interrupt thread control sequence is shown in Figure 12. A PWM frequency of 25 kHz is chosen. The sampling and control frequency of the inductance current and DC bus voltage is 12.5 kHz, corresponding to an 80 μs synchronization with the PWM reload frequency. Such a frequency is high enough to generate the proper current shape and doesn't load the DSC core more than necessary. Also, the control frequency of the input voltage PLL is designed to the input voltage frequency. This is because the sampling frequency of the input voltage positive zero-cross is equal to the input voltage frequency, and the fan speed control subroutine is executed every 80 μs to regulate the fan speed according to the change of ambient temperature in the PFC converter. The flowchart of the ADC interrupt thread is shown in Figure 13.

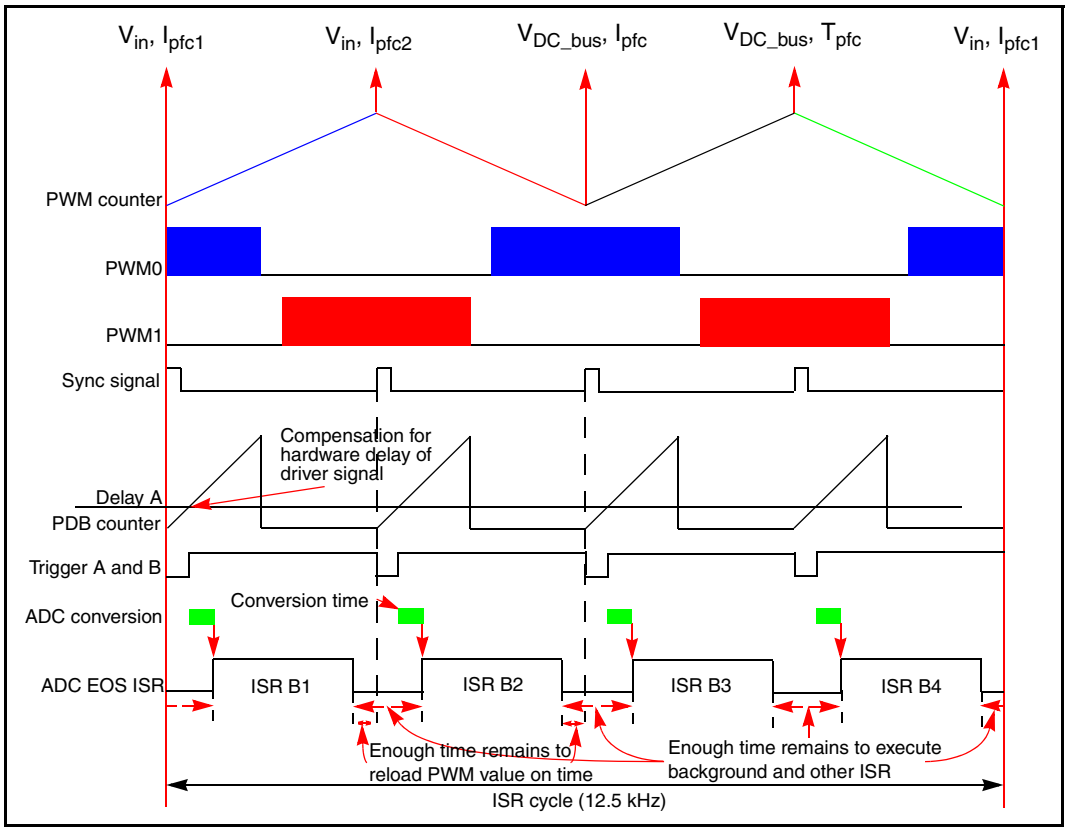

Figure 12. ADC Interrupt Control Sequence Diagram

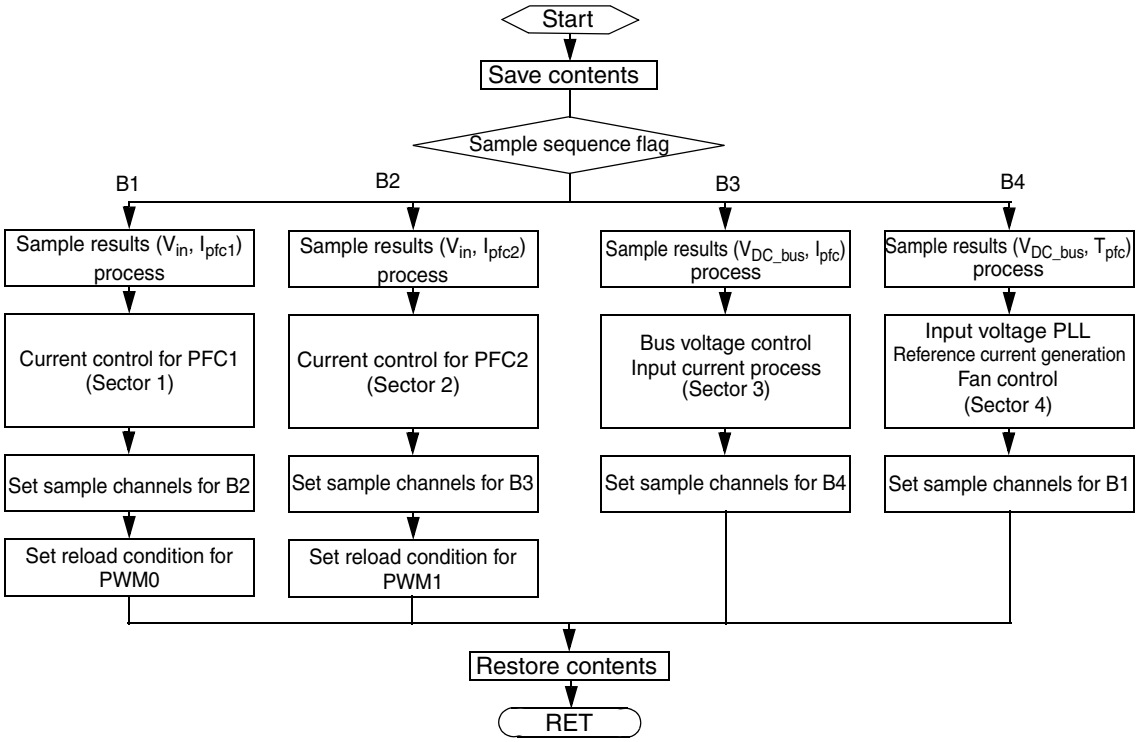

Figure 13. ADC ISR Flowchart

6.3.1 Proportional-Integral (PI) Regulator

The PI regulator is applied in the DC bus voltage, PFC inductance current, and phase-locked loop.

The expression of PI regulator is:

$$u(t) = K_P\left[e(t) + \frac{1}{T_I}\int_0^t e(t)dt\right] \qquad \textit{Eqn. 9}$$

Where:

$u(t)$ corresponds to the output signal of the regulator

$e(t)$ corresponds to the input error signal of the regulator

K_P corresponds to the proportional factor

T_I corresponds to the integral time constant

If the sampling period T is small enough, the discrete PI expression can be written:

$$u(k) = K_P\left[e(k) + K_I\sum_{j=0}^{k} e(j)\right] \qquad \textit{Eqn. 10}$$

Where:

k corresponds to the sampling order number

$u(k)$ corresponds to the output of regulator at the sampling time k

$e(k)$ and $e(k–1)$ correspond to the input errors at time k and $k–1$, respectively

Integral factor $K_I = T/T_I$

The proportional term and the integral term, respectively, are responsible for error sensitivity and the steady state error.

The incremental form of the PI regulator is expressed as:

$$\Delta u(k) = K_P\{[e(k) - e(k-1)] + K_I e(k)\} \quad \textit{Eqn. 11}$$

To improve dynamic performance of the control system, the output of PI regulator needs to be limited.

6.3.2 Input Voltage PLL

The input voltage PLL is used to create a pure sine wave phase as the reference phase of the PFC inductance current, so that the input current of the PFC converter has excellent *THDi* performance even if the input voltage is distorted. This will reduce the line noise for the PFC converter to the maximum possible extent.

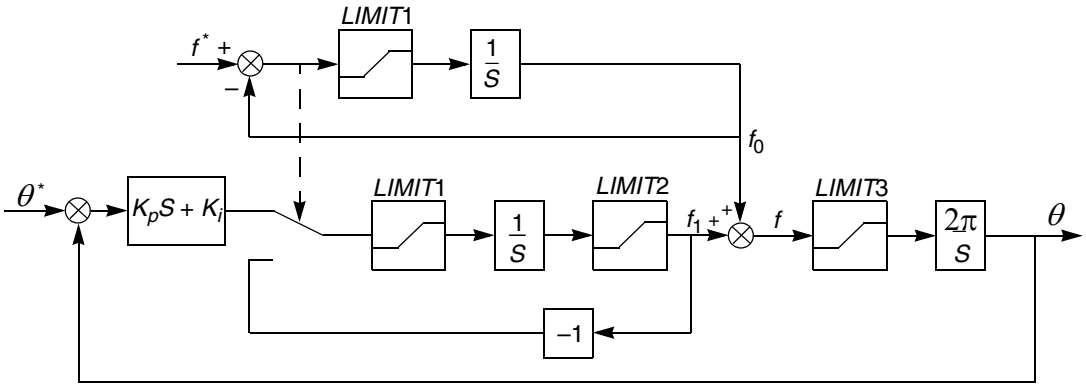

Figure 14. Input Voltage PLL Control Block Diagram

The input voltage PLL control block diagram of this application is shown in Figure 14. The PLL control system comprises a frequency-locked loop and a phase-locked loop. The frequency-locked loop is a simple integral control that ensures that the output frequency can track the target frequency quickly, and improves the dynamic performance of the phase-locked loop. The phase-locked loop system is a low-pass filter designed to output the fundamental phase of the input voltage as the reference phase of the PFC inductance current. Simultaneously, a good steady- and dynamic-state performance of the phase-locked loop system is required to assure excellent *THDi* performance of input current under any condition.

It is difficult to get the instantaneous phase of the single-phase input voltage. The positive zero-cross time of the input voltage is captured using HSCMP0 and Timer0 in this application, so the input of the input

voltage PLL controller is only the phase error on the positive zero-cross point. This determines that the maximum control frequency of the input voltage PLL is equal to the frequency of the input voltage.

6.3.3 Fan Speed Control

To reduce the system noise and improve system efficiency in a light load, the fan speed control is required. In this application, the fans are powered by a buck converter controlled in open-loop mode. The speed of the fans is regulated according to the change of ambient temperature in the PFC converter. Figure 15 shows the state machine for speed regulation of the fans. When the ambient temperature of the PFC converter rises, the speed of the fans will be increased to keep the system thermal conditions at the best possible level.

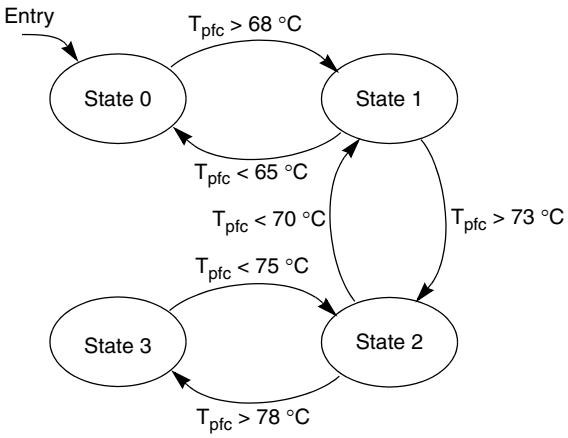

Figure 15. State Machine for Fan Speed Regulation

6.4 PWM ISR Description

The PWM interrupt thread performs the over-current protection function if an input over-current event occurs in the PFC converter. This interrupt is triggered by Fault0, which is configured as the automatic clear mode to support the cycle-by-cycle current limit function. When the interrupt is continuously triggered for a specified time in a set duration, the over-current fault will be latched and will shut down the PFC converter. Therefore the PWM interrupt has a higher priority than the ADC interrupt. The flowchart of the PWM interrupt thread is shown in Figure 16.

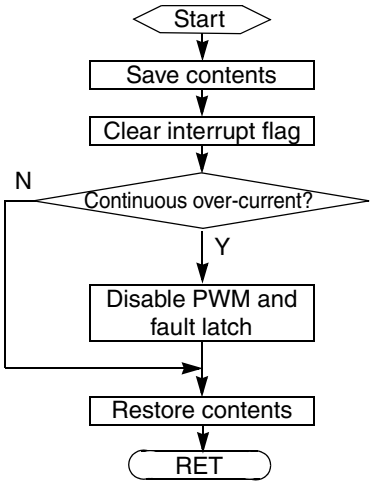

Figure 16. PWM ISR Flowchart

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