Freescale Semiconductor
Application Note

Document Number: AN3966
Rev. 0, 11/2009

PowerQUICC™ HDLC Support and Example Code

High-level data link control (HDLC) is a bit-oriented protocol that falls within layer 2, the data link layer, of the Open System Interconnection reference model. Many other layer 2 protocols are either based on or derived from HDLC.

HDLC is widely used in the telecommunications and networking industries. Freescale's PowerQUICC™ communications processors have extensive support for HDLC protocol through the communications processor module (CPM) and QUICC Engine™ technologies.

This application note explains how Freescale's existing PowerQUICC communications processors use the CPM and QUICC Engine technologies to support the HDLC protocol and provides HDLC example code.

Contents

1. HDLC Support in PowerQUICC Communications Controllers 2
2. TDM Interfaces and Time Slot Routing 4
3. HDLC Example Code 5
4. Revision History 6

freescale™ semiconductor

1 HDLC Support in PowerQUICC Communications Controllers

To meet the bandwidth and HDLC channel needs for a variety of applications, PowerQUICC processors provide the following types of controllers that support HDLC and AHDLC protocols.

- HDLC Protocol
  - — Fast communications controller (FCC)
  - — Slow communications controller (SCC)
  - — Fast universal communications controller (UCC)
  - — Multichannel controller (MCC)
  - — MCC Superchannel
  - — QUICC Multichannel Controller (QMC)
- Asynchronous HDLC
  - — SCC
  - — Slow UCC

Due to its limited application, asynchronous HDLC is not discussed in this application note.

Table 1 shows whether the existing PowerQUICC processor communication controllers use the CPM or the QUICC Engine block to support HDLC, MCC, MCC Superchannel, or QMC.

Table 1. HDLC Support on PowerQUICC Processors

Processors	HDLC	MCC	MCC Superchannel	QMC
MPC82x	CPM (SCC)	—	—	—
MPC85x MPC86x MPC87x MPC88x	CPM (SCC)	—	—	CPM (SCC)
MPC824x MPC8271 MPC8272	CPM (SCC)	—	—	CPM (SCC)
MPC825x MPC826x MPC8270 MPC8275 MPC8280	CPM (SCC)	CPM	CPM	—
MPC831x MPC834x MPC837x	—			
MPC832x	QUICC Engine block (Fast UCC)	—	—	QUICC Engine block (Slow UCC)
MPC8358 MPC8360	QUICC Engine block (Fast UCC)	QUICC Engine block	QUICC Engine block	QUICC Engine block (Slow UCC)

Table 1. HDLC Support on PowerQUICC Processors (continued)

Processors	HDLC	MCC	MCC Superchannel	QMC
MPC853x MPC8540 MPC8543 MPC8545 MPC8547 MPC8548 MPC8572	—			
MPC8541 MPC8555	CPM (FCC, SCC)	—	—	CPM (SCC)
MPC8560	CPM (FCC, SCC)	CPM	CPM	—
MPC8568	QUICC Engine block (Fast UCC)	QUICC Engine block	QUICC Engine block	QUICC Engine block (Slow UCC)

Note:
— = Not supported

1.1 HDLC (FCC, SCC, and Fast UCC)

In HDLC mode, the CPM uses a single FCC or a single SCC controller to process one HDLC channel, and the QUICC Engine block uses a single UCC controller to process one HDLC channel. The HDLC channel can usually handle the high bandwidth of HDLC traffic. For example, when a fast UCC is configured to operate in HDLC mode, the HDLC channel can handle 70 Mbps of traffic.

Because each communications controller can only support one HDLC channel, a PowerQUICC processor can only support a limited number of HDLC channels in this mode. This type of HDLC is ideal for applications that need either one high-bandwidth HDLC pipe or several high-bandwidth HDLC pipes like DS3.

1.2 MCC

The MCC is a dedicated controller that can handle as many as 256 channels of HDLC. This type of HDLC is ideal for applications that need a large number of HDLC channels, but each channel has relatively low bandwidth.

The channel-specific parameters of each MCC HDLC channel must reside in the DPRAM for CPM or MURAM for the QUICC Engine block. Thus, the maximum number of usable HDLC channels may be limited by the available DPRAM or MURAM space.

1.3 MCC Superchannel

MCC superchannel is a performance-enhancing mode. A superchannel is the combination of a group of regular MCC HDLC channels that are managed as a single channel. This allows the construction of a larger overall channel than that of a single normal MCC HDLC channel. Superchannel makes use of hardware resources of unused channels to enhance its performance.

This type of HDLC is ideal for applications where multiple time slots need to be aggregated into one HDLC channel. For example, all the time slots in a DS1 link are used to carry a single HDLC channel.

1.4 QMC

Like MCC, QMC is designed to support multiple HDLC channels. QMC can usually support up to 128 channels. However, QMC is not a dedicated controller; instead it operates on top of an FCC/SCC for CPM or a UCC for the QUICC Engine block. QMC does not support superchannel. In addition, QMC may not support all the features supported by MCC; for example, QMC may not support bit inversion.

This type of HDLC is ideal for applications where a large number of HDLC channels are needed, but each channel has relatively low bandwidth. QMC is usually used when MCC is not available.

The channel-specific parameters of each QMC HDLC channel must reside in the DPRAM for CPM or MURAM for QUICC Engine. Thus, the maximum number of usable HDLC channels may be limited by the available DPRAM or MURAM space.

Because QMC uses microcode to emulate channelization functionality, it consumes a relatively high percentage of RISC resources. If other protocols are enabled, the RISC load might also be a factor in deciding the maximum number of QMC HDLC channels.

2 TDM Interfaces and Time Slot Routing

HDLC is usually associated with time division multiplexing (TDM). PowerQUICC processors that support HDLC usually also provide TDM interfaces, that is, a serial interface (SI) and a time-slot assigner (TSA). PowerQUICC processors provide up to eight TDM interfaces: TDMa, TDMb, TDMc, TDMd, TDMe, TDMf, TDMg, and TDMh.

The SI is a physical interface that can be connected to both standard TDM interfaces, such as T1/E1, and custom TDM interfaces as long as the bandwidth does not surpass the maximum bandwidth allowed. For example, four E1 lines can be connected to four serial interfaces (for example, TDMa, TDMb, TDMc, and TDMd) and routed to 128 MCC HDLC channels. This uses up to 20 I/O pins. The four E1 lines can also be multiplexed into one TDM stream using external hardware and then connected to one SI (TDMa) and routed to 128 MCC HDLC channels. This only uses a maximum of five I/O pins.

The TSA can route time slots to MCC or any UCC/FCC/SCC. When routing to MCC, the TSA can multiplex/demultiplex time slots to specified HDLC channels. When routing to a UCC/FCC/SCC, TSA can only multiplex/demultiplex time slots to a specified UCC/FCC/SCC, that is, one channel per controller.

The TSA routing is configured through SI RAM. Although it is possible to change routing configuration through shadow SI RAM, the TSA is not designed to do real-time time slot level switching. In many applications, an external time slot interchange (TSI) is needed to perform real-time time slot switching.

Besides TDM TSA, each QMC also has its own TSA that can only multiplex/demultiplex time slots to specified HDLC channels. For MCC superchannel, the demultiplexing of time slots on the transmitter side is done by MCC while the multiplexing of time slots on the receiver side is done by TDM TSA.

3 HDLC Example Code

The following MPC8360E example code projects are provided as four separate CodeWarrior® projects:

- MPC8360E-UCC-HDLC
- MPC8360E-QMC-HDLC
- MPC8360E-MCC-HDLC
- MPC8360E-MCC-SC-HDLC

All example code has been tested on an MPC8360EA-MDS board with loopback at the TDM TSA. These projects can be relatively easily ported to other PowerQUICC processors.

3.1 MPC8360E UCC HDLC Example Code

The example in Figure 1 shows a single HDLC channel on UCC8. UCC8 is connected to TDMc, and one time slot is routed between the TDMc TSA and UCC8. TDMc SI is put in loopback mode.

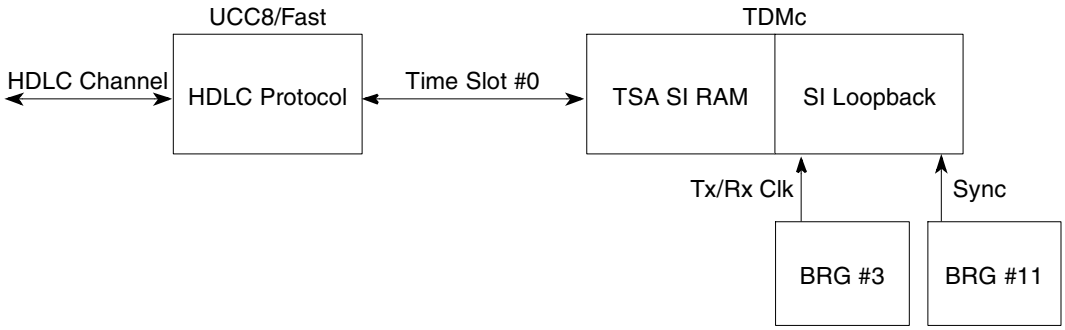

Figure 1. MPC8360E UCC HDLC Configuration

3.2 MPC8360E MCC HDLC Example Code

The example in Figure 2 shows 24 HDLC channels on the MCC. The MCC is connected to TDMc, and 24 time slots are routed as separate channels between the TDMc TSA and the MCC. TDMc SI is put in loopback mode.

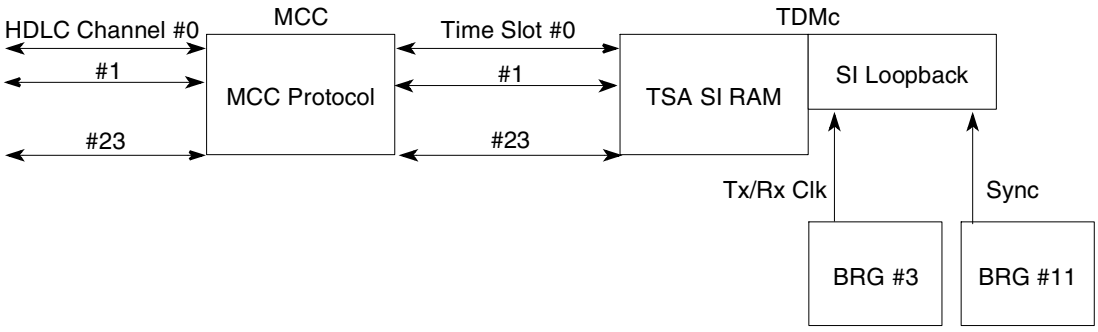

Figure 2. MPC8360E MCC HDLC Configuration

3.3 MPC8360E MCC Superchannel HDLC Example Code

The example in Figure 3 shows a single HDLC channel (superchannel) on the MCC. The MCC is connected to TDMc and 24 time slots are routed as one channel from the TDMc TSA to the MCC. The 24 time slots are routed as separate channels from the MCC to TDMc. TDMc SI is put in loopback mode.

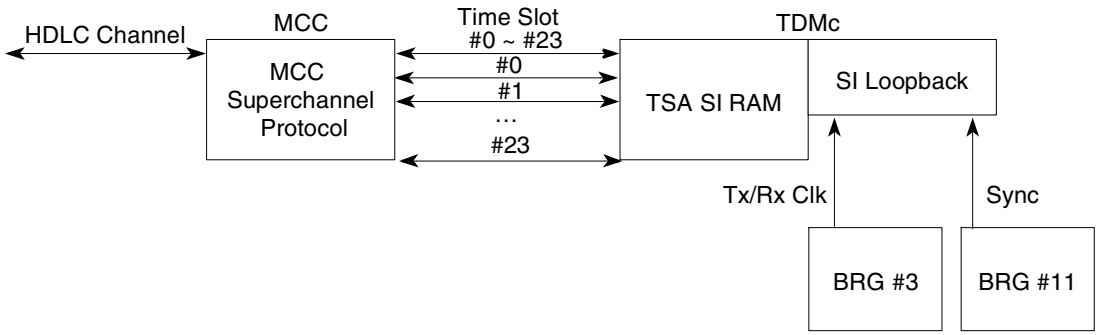

Figure 3. MPC8360E MCC Superchannel HDLC Configuration

3.4 MPC8360E QMC HDLC Example Code

The example in Figure 4 shows 24 HDLC channels on UCC2, which is configured for QMC. UCC2 is connected to TDMc, and 24 time slots are routed as one channel between the TDMc TSA and UCC2. TDMc SI is put in loopback mode.

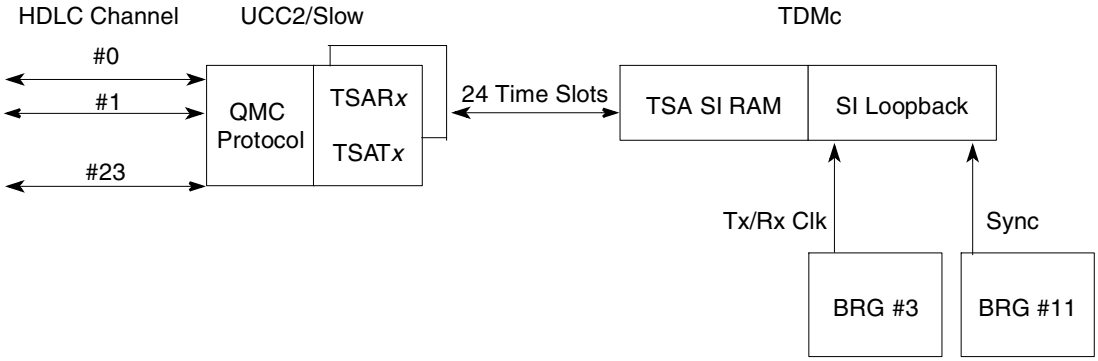

Figure 4. MPC8360E QMC HDLC Configuration

4 Revision History

Table 2 provides a revision history for this application note.

Table 2. Document Revision History

Rev. Number	Date	Substantive Change(s)
	11/2009	Initial Release

THIS PAGE INTENTIONALLY LEFT BLANK

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
http://www.freescale.com/support

USA/Europe or Locations Not Listed:
Freescale Semiconductor, Inc.
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
1-800-521-6274 or
+1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku
Tokyo 153-0064
Japan
0120 191014 or
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor
Literature Distribution Center
1-800 441-2447 or
+1-303-675-2140
Fax: +1-303-675-2150
LDCForFreescaleSemiconductor
@hibbertgroup.com

Document Number: AN3966
Rev. 0
11/2009