Freescale Semiconductor
Application Note

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PowerQUICC and QorIQ DDR3 SDRAM Controller Register Setting Considerations

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This application note expands on the description of the double data rate (DDR3) memory controller programmable registers in the PowerQUICC and QorIQ processor reference manuals. The applicable device reference manual defines the function of each field in the programmable registers. This document focuses on why and when to select certain configurations of the register bits and fields to achieve efficient DDR programming. To obtain a comprehensive understanding of the memory controller functionality and the basic operation of the DDR3 memory, see the following recommended documentation:

- Applicable reference manual
- Applicable device errata
- Applicable processor revision conversion guides
- Manufacturer data sheet on the memory selected

Many of the PowerQUICC and QorIQ documents are available at the Freescale website listed on the back cover of this document.

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1 Configuration guidelines

When selecting values for the memory controller registers, use the following steps:

1. Obtain the data sheet for the DDR SDRAM chip (or DIMM) used.
2. Using the values provided in the DDR data sheet, configure the register values per corresponding parameters. Values can be stated in the following ways in the DDR data sheet:
   — As the number of memory clocks, and it can be directly used for configuring the registers
   — In units of fractions of a second, and the value must be divided by the memory clock period to obtain the number of clocks. If the memory frequency clock is lower than the DDR data sheet rating, the actual memory frequency should be used to calculate the memory clock period. For example, if a DDR3-1067 data sheet provides a value of 15 ns for a given parameter (for example, tRP min = 15 ns), and the memory clock operates at 333.5 MHz (or a data rate of 667 Mbps), then the number of clocks is calculated by first finding the operating memory period (1/333.5 MHz = 3.0 ns) and next dividing the value by period 15 ns/3.0 ns = 5 clk. As indicated, a higher-rated memory can operate in lower frequencies. The DDR3-1067 is a common DDR3 memory, but per the JEDEC specification, DDR3-1067 (or any other JEDEC-compliant DDR3 DRAM) can operate at a data rate down to 600 Mbps.
3. Set the remaining memory register settings as specified in the applicable device reference manual and per additional information provided in this application note.

Based on the most commonly observed user-error in the memory controller register setting for DDR3, special attention must be paid to the following items:

- Selecting and validating the following fields:
  — DDR_SDRAM_CLK_CNTL[CLK_ADJUST]
  — DDR_WRLVL_CNTL[WRLVL_START]
  — TIMING_CFG_5[R/WODT_ON, R/WODT_OFF]
- Selecting and verifying $\overline{\text{CAS}}$ latency, write latency, and additive latency
- Confirming that all DDR mode register values match DDR controller configuration registers, especially the $\overline{\text{CAS}}$ latency, additive latency, burst type and write recovery settings
- Verifying whether the registered or unbuffered DIMMs are used
- Verifying the minimum value of four clock cycles are observed for the tWTR, tRRD, and tRTP fields

4. Disable the clocks that are not used via the DDRCLKDR register. By default, all clocks are operational, but not all clock signals are used in a given application. Therefore, by disabling the unused clocks, it first lowers the power consumption and then lowers the unused switching activity in the part. DDRCLKDR is not a part of the memory controller register set; it is located in the global utility register section.

Table 1 lists the memory controller programmable registers in this document.

Table 1. Summary of register settings

Offset	Register name	Register description	Section/page
0x000	CS*n*_BOUNDS	Chip-select *n* memory bounds register	2.1/4
0x080	CS*n*_CONFIG	Chip-select *n* configuration register	2.2/5
0x0C0	CSn_CONFIG_2	Chip-select n configuration 2 register	2.3/6
0x100	TIMING_CFG_3	DDR SDRAM timing configuration 3 register	2.4/7
0x104	TIMING_CFG_0	DDR SDRAM timing configuration 0 register	2.5/9
0x108	TIMING_CFG_1	DDR SDRAM timing configuration 1 register	2.6/10
0x10C	TIMING_CFG_2	DDR SDRAM timing configuration 2 register	2.7/12
0x110	DDR_SDRAM_CFG	DDR SDRAM control configuration 1 register	2.8/14
0x114	DDR_SDRAM_CFG_2	DDR SDRAM control configuration 2 register	2.9/17
0x118	DDR_SDRAM_MODE	DDR SDRAM mode configuration register	2.10/19
0x11C	DDR_SDRAM_MODE_2	DDR SDRAM mode configuration 2 register	2.11/21
0x124	DDR_SDRAM_INTERVAL	DDR SDRAM interval configuration register	2.12/23
0x130	DDR_SDRAM_CLK_CNTL	DDR SDRAM clock control register	2.13/23
0x160	TIMING_CFG_4	DDR SDRAM timing configuration 4 register	2.14/24
0x164	TIMING_CFG_5	DDR SDRAM timing configuration 5 register	2.15/25
0x170	DDR_ZQ_CNTL	DDR ZQ calibration control	2.16/27
0x174	DDR_WRLVL_CNTL	DDR write leveling control	2.17/28
0x180	DDR_SDRAM_RCW_*n*	DDR register control words n	2.18/29
0x190	DDR_WRLVL_CNTL_*n*	DDR write leveling control n	2.19/29
0x200	DDR_SDRAM_MODE_*n*	DDR SDRAM mode configuration {3...8}	2.20/30
0xB28	DDRCDR_1	DDR control driver register 1	2.21/30
0xB2C	DDRCDR_2	DDR control driver register 2	2.22/32

2 Register definitions

This section describes the registers and settings discussed in this application note.

2.1 Chip-Select *n* Memory Bounds Register (CS*n*_BOUNDS)

The selections in the chip-select *n* memory bounds register (CS*n*_BOUNDS), which is shown in Figure 1, are based on the size, and starting and ending values of selected memory.

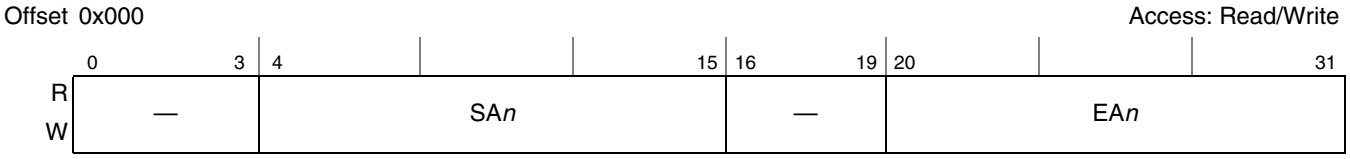

Figure 1. Chip-Select n Memory Bounds Register (CS*n*_BOUNDS)

Table 2 describes the CS*n*_BOUNDS register fields.

Table 2. CS*n*_BOUNDS Register field descriptions

Bits	Name	Description
0–3	—	Reserved
4–15	SA*n*	Starting address for chip select (bank) *n* This value is compared against the 12 msbs of the 36-bit address.The manufacturer data sheet for the selected memory should be used to obtain the size of memory. The starting address is usually selected to be 0x0000_0000_0 for the first chip select (CS0), which is represented by 0 in this field. When there is more than one chip select, the starting address should consider the CS0 end address to avoid overlapping of memory space in each chip select. For example, a two-ranked, 2-GB DDR3 DIMM (each rank of 1 GB), can select the 0 for the starting address of first rank (CS0). The starting address of the second rank (CS1) can be set to 1 GB at 0x0_4000_0000, which is represented by 0x040 in this field. Another possibility is that the second rank can start at any location after 1 GB; for example, at 39 GBs at 0x9_C000_0000, which is represented by 0x9C0 in this field. Additional examples are as follows: • 512 MBs --> 0x020 • 1 GB --> 0x040 • 4 GBs --> 0x100 • 8 GBs --> 0x200
16–19	—	Reserved
20–31	EA*n*	Ending address for chip select (bank) *n* This value is compared against the 12 msbs of the 36-bit address. The end address can be set to the desired value up to the maximum value of the size of the selected memory. If the end address is set to less than the “starting address + DRAM size,” it works, but the unassigned memory space remains unused. For example, a single-rank, 1-GB DDR3 memory DIMM with the starting address of 0 can have the max ending address of 0x0_3FFF_FFFF to include the entire 1-GB memory space, which is represented by 0x03F in this field. In this example, if a smaller value than 0x03F is selected for the end address, the unassigned memory space remains unused. Additional examples are as follows: • 512 MBs --> 0x01F • 1 GB --> 0x03F • 4 GBs --> 0x0FF • 8 GBs --> 0x1FF

2.2 Chip-Select Configuration Register (CS*n*_CONFIG)

The chip-select configuration register (CS*n*_CONFIG), shown in Figure 2, enables DDR chip-select *n* and sets the number of row and column bits used for this chip-select.

Offset 0x080 Access: Read/Write

	0	1	2	3	4 7	8	9 11	12	13 15
R W	CS_*n*_EN	—	INTLV_EN	—	INTLV_CTL	AP_*n*_EN	ODT_RD_CFG	—	ODT_WR_CFG

	16 17	18 20	21 23	24 28	29 31
R W	BA_BITS_CS_*n*	—	ROW_BITS_CS_*n*	—	COL_BITS_CS_*n*

Figure 2. Chip-Select Configuration Register (CS*n*_CONFIG)

Table 3 describes the CS_*n* CONFIG register fields.

Table 3. CS_*n* CONFIG Register field descriptions

Bits	Name	Description	Recommended settings
0	CS_*n*_EN	Chip-select *n* enable This bit should be set if chip-select *n* is used in the memory configuration. For example, set CS0_CONFIG[CS_0_EN] to chip-select 0 in the memory configuration.	—
1	—	Reserved	0
2	INTLV_EN	Memory controller interleave enable This field is only available in devices with two or four memory controllers. Set this bit to enable interleaving between the two or four memory controllers. This field is only available in CS0_CONFIG register. Size of the memory interleaved between the two memory controllers must be the same in the CS0_BOUNDS register. The data bus widths of the two controllers must be the same. In addition, when enabling this bit, CS0_CONFIG[INTLV_CTL] field must be set to a valid and same selection in both memory controllers. For further details on memory controller interleaving, see *DDR Interleaving for PowerQUICC and QorIQ Processors* (AN3939).	—
3	—	Reserved	0
4–7	INTLV_CTL	This field is only available in devices with two or four memory controllers. When interleaving between two memory controller is enabled, choose a valid value from available selections. Cache line, page, bank, and super-bank interleaving options are available. For further details on memory controller interleaving, see *DDR Interleaving for PowerQUICC and QorIQ Processors* (AN3939).	—
8	AP_*n*_EN	Chip-select *n* auto-precharge enable Chip-select *n* is auto precharged by setting this field (AP_*n*_EN = 1). In addition, chip-select *n* is auto precharged if both this field (AP_*n*_EN = 0) and the precharge interval field (DDR_SDRAM_INTERVAL[BSTOPRE] = 0) are cleared. This field is usually cleared leaving the decision for auto-precharged or not auto-precharged to the value selected for the precharge interval field (that is, DDR_SDRAM_INTERVAL[BSTOPRE]).	0

Table 3. CS_*n* CONFIG Register field descriptions (continued)

Bits	Name	Description	Recommended settings
9–11	ODT_RD_CFG	ODT for reads configuration This setting is topology-dependent. During the read cycle, the memory controller is the target and DDR3 memory is the source. Typically, for one DIMM module, ODT is disabled for reads. For two modules, ODT is asserted to the standby module (the DIMM that is not active) during reads. In addition, regardless of whether one or two modules are used only during reads, the on-chip ODT is asserted to memory controller (enabled through DDR_SDRAM_CFG2[ODT_CFG]). Therefore, this field, which controls assertion of the ODT signal to DDR3 memory during the read, is typically disabled for one module and enabled for two modules for the inactive module. This is not a requirement, and DRAM vendor documents need to be consulted for vendor-specific recommendation. For further information on DRAM ODT settings, see the Micron technical note “tn_41_08” available on their website.	Application dependent
12	—	Reserved	—
13–15	ODT_WR_CFG	ODT for writes configuration During the write cycle, the memory controller is the source and DDR3 memory is the target. For one DIMM module with one rank, assert the ODT to the active module. For one DIMM module with two rank, assert the ODT only to rank1 to the active module. For two DIMM modules, assert the ODT to the standby module. The reason for asserting or not asserting ODT is to balance the line impedance between the source and the target to avoid unwanted reflections of signals. This is not a requirement, and DRAM vendor documents need to be consulted for vendor specific recommendation. For further information on DRAM ODT settings, see the Micron technical note “tn_41_08” available on their website.	1 —> Assert ODT only during writes to CS0.
16–17	BA_BITS_CS_*n*	Number of bank bits for SDRAM on chip-select *n* The value of number of banks is obtained from the memory manufacturer’s data sheet. For DDR3, eight banks are typically selected.	—
18–20	—	Reserved	—
21–23	ROW_BITS_CS_*n*	Number of row bits for SDRAM on chip-select *n* The number of rows is obtained from the memory manufacturer’s data sheet.	—
24–28	—	Reserved	—
29–31	COL_BITS_CS_*n*	Number of column bits for SDRAM on chip-select *n* The number of columns is obtained from the memory manufacturer’s data sheet.	—

2.3 Chip-Select n Configuration 2 Register (CS*n*_CONFG_2)

The chip-select *n* configuration 2 register (CS*n*_CONFG_2) is shown in Figure 3.

Figure 3. Chip-Select n Configuration 2 Register (CS*n*_CONFG_2)

Table 4 describes the CS*n*_CONFG_2 register fields.

Table 4. CS*n*_CONFG_2 Register field descriptions

Bits	Name	Description
0–4	—	Reserved
5–7	PARS_CFG	Partial array self-refresh config This is an optional feature for DDR3 DRAM. Therefore, users should check the memory manufacturer's data sheet for the partial array self-refresh availability before enabling this field. This feature works for both DDR2 and DDR3, if the option is available in DRAM. Instead of putting the entire memory in self-refresh mode, only a section of it is put in self-refresh mode; the remaining data is not maintained and may be lost. This feature could be useful if a section of memory needs to be preserved during a self-refresh event. By only keeping a small section of memory in self-refresh mode, some power savings can be achieved. Setting this field to a value other than 0 causes the selected partial self-refresh to be implemented when memory is put in self-refresh mode. Partial array self-refresh (PASR) can be enabled for any chip select using the CS*n*_CONFIG_2[PASR_CFG] fields. If PASR is enabled for a given chip select, then the sub-bank and row decode are swapped, and the sub-bank is decoded as the most significant portion of the DRAM address (see section, "DDR SDRAM Address Multiplexing," in the applicable device reference manual). If this field is a non-zero value, then it overrides the 3 least significant bits in DDR_SDRAM_MODE_2[ESDMODE2] during the automatic initialization for chip select *n*. In addition, if a non-zero value is programmed in this field, then the address decode for chip select *n* is optimized for partial array self-refresh, as shown in "DDR SDRAM Address Multiplexing." For exact selection of values for this field, see the memory manufacturer's data sheet. When using self-refresh, setting this field allows the user to select a partial section of memory to be placed in self-refresh instead of the entire memory space. Following are a few of the selection listed per JEDEC: 000 Full array 001 Half array (BA[2:0] = 000,001, 010, and 011) 010 Quarter array (BA[2:0] = 000, and 001) 011 1/8 array (BA[2:0] = 000)
8–31	—	Reserved

2.4 DDR SDRAM Timing Configuration 3 Register (TIMING_CFG_3)

The DDR SDRAM timing configuration 3 register (TIMING_CFG_3), shown in Figure 4, sets the number of clock cycles between various SDRAM control commands.

Offset 0x100 Access: Read/Write

	0	6	7	8	11	12	15	16	18	19	20	28	29	31
R W	—		EXT_ACTTOPRE	—		EXT_REFREC		—		EXT_CASLAT	—		CNTL_ADJ	

Figure 4. DDR SDRAM Timing Configuration 3 Register (TIMING_CFG_3)

Table 5 describes the TIMING_CFG_3 register fields.

Table 5. TIMING_CFG_3 Register field descriptions

Bits	Name	Description	Recommended setting
0–6	—	Reserved	—
7	EXT_ACTTOPRE	Extended activate to precharge interval (tRAS) Determines the number of clock cycles from an activate command until a precharge command is allowed. This field is concatenated with TIMING_CFG_1[ACTTOPRE] to obtain a 5-bit value for the total activate to precharge. Note that a 5-bit value of 0_0000 is the same as a 5-bit value of 1_0000. Both values represent 16 cycles. 0 0 clocks 1 16 clocks	From manufacturer's data sheet
8–10	—	Reserved	—
11–15	EXT_REFREC	Extended refresh recovery time (tRFC) Controls the number of clock cycles from a refresh command until an activate command is allowed. This field is concatenated with TIMING_CFG_1[REFREC] to obtain an 8-bit value for the total refresh recovery. Note that hardware adds an additional 8 clock cycles to the final 8-bit value of the refresh recovery. tRFC = {EXT_REFREC || REFREC} + 8. For example, if tRFC = 127.5 ns from the DDR3 data sheet, and the frequency of operation is an 800-MHz data rate (that is, tCK = 2.5 ns) the result is: number of clock cycles for refresh recovery = 127.5 ns/2.5 ns = 51 clks if EXT_REFREC = 4'b0010 is set (that is, 32 clock cycles) then 51 – 32 = 19 clock cycles remain. Set REFREC = 4'b1011 (that is, 19 clock cycles, 11 + 8) The same example by using the formula is as follows: tRFC = {EXT_REFREC || REFREC} + 8 = {4'b0010 || 4'b1011} + 8 = 8'b00101011 + 8 = 43 + 8 = 51	From manufacturer's data sheet
16–18	—	Reserved	0
19	EXT_CASLAT	Extended MCAS latency from READ command This field is the number of clock cycles between registration of a READ command by the SDRAM and the availability of the first output data. If a READ command is registered at clock edge *n* and the latency is *m* clocks, data is available nominally coincident with clock edge *n* + *m*. This field is concatenated with TIMING_CFG_1[CASLAT] to obtain a 5-bit value for the total CAS latency. Note that if this bit is set, 8 clocks are added to the programmed value in TIMING_CFG_1[CASLAT]. 0 0 clocks 1 8 clocks	From manufacturer's data sheet
20–28	—	Reserved	—
29–31	CNTL_ADJ	Control adjust This field controls the amount of delay to add to the lightly loaded control signals with respect to all other DRAM address and command signals. The signals affected by this field are MODT[0:3], MCS[0:3], and MCKE[0:3]. This field provides an option if adjusting of control signals are required. The usage is application-specific. The typical value is 0.	0

2.5 DDR SDRAM Timing DDR SDRAM Timing Configuration 0 Register (TIMING_CFG_0)

The DDR SDRAM timing configuration 0 register (TIMING_CFG_0), shown in Figure 5, sets the number of clock cycles between various SDRAM control commands.

Offset 0x104 Access: Read/Write

	0 1	2 3	4 5	6 7	8	9 11	12 15	16 19	20 23	24 27	28 31
R W	RWT	WRT	RRT	WWT	—	ACT_PD_EXIT	PRE_PD_EXIT	—	ODT_PD_EXIT	—	MRS_CYC

Figure 5. DDR SDRAM Timing Configuration 0 Register (TIMING_CFG_0)

Table 6 describes the TIMING_CFG_0 register fields.

Table 6. TIMING_CFG_0 field descriptions

Bits	Name	Description	Recommended setting
0–1	RWT	Read-to-write turnaround (tRTW) This field specifies how many extra cycles are to be added between a read-to-write turnaround. If 0 clocks are chosen, the DDR controller uses a fixed number based on the CAS latency and write latency. Choosing a value other than 0 adds extra cycles past this default calculation. By default, the DDR controller determines the read-to-write turnaround as CL – WL + BL/2 + 2: • CL is the CAS latency rounded up to the next integer. • WL is the programmed write latency. • BL is the burst length. Considering that WL = CWL for DDR3, and CWL is always = or < CL, by substituting it in the equation, the default turnaround cycles always become equal to BL/2 + 2 or more cycles. JEDEC calls for a minimum value of BL/2 + 2, which is always met with a value of zero in this field. However, this is not an issue because this field is used to resolve a contention if one is encountered. When there are two or more memory controller are available and Interleaved this field should be set to 1. Otherwise, this field is usually cleared.	• 1 when two or more memory controllers are interleaved • 0 when not interleaving
2–3	WRT	Write-to-read turnaround (tWTR) This field specifies how many extra cycles are to be added between a write-to-read turnaround. If 0 clocks are chosen, the DDR controller uses a fixed number based on the read latency and write latency. Choosing a value other than 0 adds extra cycles past this default calculation. By default, the DDR controller determines the write-to-read turnaround as WL – CL + BL/2 + 1: • CL is the CAS latency rounded down to the next integer. • WL is the programmed write latency. • BL is the burst length. Considering that WL = CWL and CWL in most cases CWL= CL or = CL –1, substituting it in the equation, the default turnaround equation is BL/2 or more. This field is not to be confused with the TIMING_CFG_1[WRTORD], which requires the tWTR parameter from the SDRAM data sheet. This field is used to resolve a contention if one is encountered. When there are two or more memory controllers each with two chip selects available and Interleaved this field should be set to 1; otherwise, this field is usually cleared.	• 1 when two or more memory controllers each with two chip selects are interleaved. • 0 when not interleaving

Table 6. TIMING_CFG_0 field descriptions (continued)

Bits	Name	Description	Recommended setting
4–5	RRT	Read-to-read turnaround This field specifies how many extra cycles are to be added between reads to different chip selects. By default, three cycles are required between read commands to different chip selects. Extra cycles may be added with this field. **Note:** If 8-beat bursts are enabled, five cycles is the default. This field is usually cleared. But, in the case of two slots with each slot using a dual ranked DIMM, this field should be set to 2 to prevent ODT overlapping.	• 2 when two slots with each slot using a dual ranked DIMM • 0 when two slots are not used
6–7	WWT	Write-to-write turnaround This field specifies how many extra cycles are to be added between writes to different chip selects. By default, 2 cycles are required between write commands to different chip selects. Extra cycles can be added with this field. **Note:** If 8-beat bursts are enabled, 4 cycles is the default. This field is usually cleared. But when two slots with each slot using a dual ranked DIMM, this field should be set to 2 to prevent ODT overlapping.	0
8	—	Reserved	0
9–11	ACT_PD_EXIT	Active power down exit timing For DDR3, this field should be set to tXP value.	From manufacturer's data sheet
12–15	PRE_PD_EXIT	Precharge power down exit timing For DDR3: • If DDR_SDRAM_MODE[PD] = 0 (Slow power down), set this field to tXDLL. • If DDR_SDRAM_MODE[PD] = 1 (Fast power down), set this field to tXP.	From manufacturer's data sheet
16–19	—	Reserved	—
20–23	ODT_PD_EXIT	ODT power down exit timing For DDR3, this field should be set to 3'b001.	1
24–27	—	Reserved	—
28–31	MRS_CYC	Mode register set cycle time (tMRD) This field should be based on tMRD.	From manufacturer's data sheet

2.6 DDR SDRAM Timing Configuration 1 Register (TIMING_CFG_1)

The DDR SDRAM timing configuration 1 register (TIMING_CFG_1), shown in Figure 6, sets the number of clock cycles between various SDRAM control commands.

Offset 0x108 Access: Read/Write

	0 1 3	4 7	8 11	12 15	16 19	20 23	24 25 27	28 29 31
R W	PRETOACT	ACTTOPRE	ACTTORW	CASLAT	REFREC	WRREC	ACTTOACT	WRTORD

Figure 6. DDR SDRAM Timing Configuration 1 Register (TIMING_CFG_1)

Table 7 describes the TIMING_CFG_1 register fields.

Table 7. TIMING_CFG_1 field descriptions

Bits	Name	Description	Recommended setting
0–3	PRETOACT	Precharge-to-activate interval (tRP) This field should be based on tRP. Using the minimum from the specification yields the best possible performance.	From manufacturer's data sheet
4–7	ACTTOPRE	Activate to precharge interval (tRAS) This field should be based on tRAS.	From manufacturer's data sheet
8–11	ACTTORW	Activate to read/write interval for SDRAM (tRCD) This field should be based on tRCD.	From manufacturer's data sheet
12–15	CASLAT	$\overline{\text{MCAS}}$ latency from READ command This field should be based on the corresponding CL value, which can be obtained from the manufacturer's data sheet depending on the operation frequency. For DDR3, the minimum value of CAS_LAT is 5 clock cycles. The CAS value selected here should be identical to the value in the corresponding field in DDR_SDRAM_MODE[SDMODE].	From manufacturer's data sheet
16–19	REFREC	Refresh recovery time (tRFC) This field should be based on tRFC. If the tRFC value obtained from the SDRAM data sheet is larger than the max value provided by this field, TIMING_CFG_3[EXT_REFREC] should be used to accommodate the difference.	From manufacturer's data sheet
20–23	WRREC	Last data to precharge minimum interval (tWR) This field should be based on tWR. If on-the-fly burst chop configuration is enabled, that is, DDR_SDRAM_CFG_2[OBC_CFG] = 1, then the value of this field should be tWR + 2 (clock cycles). The WR value selected should be identical to the value in the corresponding field in DDR_SDRAM_MODE[SDMODE] only when DDR_SDRAM_CFG_2[OBC_CFG] = 0. When DDR_SDRAM_CFG_2[OBC_CFG] = 1, the value in the corresponding field in DDR_SDRAM_MODE[SMODE] should be based on tWR and should NOT be set to tWR + 2 (clock cycles).	From manufacturer's data sheet
24–27	ACTTOACT	Activate-to-activate interval (tRRD) This field should be based on tRRD. The minimum value for this field is 4 clock cycles. Therefore, if the data sheet's minimum value is fewer than 4 clocks, give this field a value of 4 clock cycles.	From manufacturer's data sheet
28–31	WRTORD	Last write data pair to read command issue interval (tWTR) This field should be based on tWTR. The minimum value for this field is 4 clock cycles. Therefore, if the data sheet's minimum value is fewer than 4 clocks, give this field a value of 4 clock cycles. If on-the-fly burst chop configuration is enabled, that is, DDR_SDRAM_CFG_2[OBC_CFG] = 1, then the value of this field should be tWTR + 2 (clock cycles).	From manufacturer's data sheet

2.7 DDR SDRAM Timing Configuration 2 Register (TIMING_CFG_2)

The DDR SDRAM timing configuration 2 register (TIMING_CFG_2) is shown in Figure 7.

Offset 0x10C Access: Read/Write

	0–3	4–8	9–12	13–15	16–18	19–21	22–23	25–26	31
R W	ADD_LAT	CPO	WR_LAT	—	RD_TO_PRE	WR_DATA_DELAY	CKE_PLS	FOUR_ACT	

Figure 7. DDR SDRAM Timing Configuration 2 Register (TIMING_CFG_2)

Table 8 describes the TIMING_CFG_2 register fields.

Table 8. TIMING_CFG_2 Register field descriptions

Bits	Name	Description	Recommended setting
0–3	ADD_LAT	Additive latency Additive latency (AL) can be used to make commands and data buses efficient. This means that within the sustainable bandwidth of DDR3 interface, AL selection can improve efficiency. For DDR3, AL can be selected to be CL –1 or CL –2. The AL value selected should be identical to the value in the corresponding field in DDR_SDRAM_MODE[ESDMODE].	—
4–8	CPO	$\overline{\text{MCAS}}$-to-preamble override As stated in the applicable device reference manual, the CPO value defines the number of DRAM cycles between the time when the controller issues a read command and when the corresponding DQS preamble is valid for the memory controller. CPO is a timing calculation that starts when a read command is issued from the controller and ends when the corresponding preamble strobe from the DDR memory is expected to be received back and recognized in the memory controller. The CPO value has memory controller, SDRAM memory, and printed circuit board (PCB) dependencies with a minimum and maximum value. Therefore, the min and max values result in an acceptable window of operation where the CPO value is valid. The CPO value is obtained from this window of operation. Therefore, if the window operation allows it, several values can be operational and the center value should be selected for the best option. Application note “Programming the PowerQUICC III/PowerQUICC II Pro DDR SDRAM Controller” (AN2583) provides a detailed explanation and calculation example that should be studied for a complete understanding of the CPO value and its calculation. For DDR3, automatic CPO should be selected. The automatic CPO selection controller automatically determines a correct CPO value for each byte lane. However, if a CPO value other than automatic CPO is selected for this field, the same value applies to all byte lanes.	Automatic CPO should be selected.
9–12	WR_LAT	Write latency This field should be set to CAS write latency (CWL). The value of CWL is frequency-dependent and provided in the manufacturer’s data sheet.	From manufacturer’s data sheet
13–14	—	Reserved	—

Table 8. TIMING_CFG_2 Register field descriptions (continued)

Bits	Name	Description	Recommended setting
15–18	RD_TO_PRE	Read to precharge (tRTP) This field should be based on tRTP. The minimum value for this field is 4 clock cycles. Therefore, if the data sheet min value is fewer than 4 clocks, give this field a value of 4 clock cycles. If on-the-fly burst chop configuration is enabled, that is, DDR_SDRAM_CFG_2[OBC_CFG] = 1, then the value of this field should be tRTP + 2 (clock cycles). There is no need to consider additive latency (AL) if the required controller automatically adds to AL to meet the relevant timing requirement.	From manufacturer's data sheet
19–22	WR_DATA_DELAY	Write command to write data strobe timing adjustment If write leveling is enabled (that is, DDR_WRLVL_CNTL[WRLVL_EN] = 1) WR_DATA_DELAY field is ignored by the memory controller. When fly-by DDR3 topology is used, the write leveling register must be enabled to compensate for introduced skews between clock and strobe signals. For rare cases where write leveling is disabled (that is, DDR_WRLVL_CNTL[WRLVL_EN] = 0) then this field should be configured so that the first rising edge of MDQS (strobe) for a write operation meets the DRAM tDQSS specification. tDQSS is a JEDEC-defined timing parameter ensuring that, during a write operation, the controller issues the strobe no earlier than 75 percent, and no later than 125 percent, of the rising edge of the clock. There can be more than one valid setting, and when more than one selection is valid, the center value is the best option. In many cases, ½ clock delay is the recommended value for this field. The value selected for the write data delay should closely follow the DDR_SDRAM_Clock_Ctrl [CLK_ADJUST] field value. In addition, CLK_ADJUST shifts MCK/MCK_B (clock) with respect to where the ADDR/CMD (address/command) is launched. In contrast, WR_DATA_DELAY shifts transmit DQS/DQS_B/DQ/ECC/DM with respect to where the ADDR/CMD was launched. Therefore, if WR_DATA_DELAY is not changed to match the CLK_ADJUST change, a timing skew is added between MCK and DQS.	—
23–25	CKE_PLS	Minimum CKE pulse width (tCKE) This field should be based on tCKE.	From manufacturer's data sheet
26–31	FOUR_ACT	Window for four activates (tFAW) This field should be based on tFAW.	From manufacturer's data sheet

2.8 DDR SDRAM Control Configuration Register (DDR_SDRAM_CFG)

The DDR SDRAM control configuration register (DDR_SDRAM_CFG) is shown in Figure 8.

Offset 0x110 Access: Read/Write

	0	1	2	3	4	5–7	8–9	10	11–12	13	14	15
R W	MEM_EN	SREN	ECC_EN	RD_EN	—	SDRAM_TYPE	—	DYN_PWR	DBW	8_BE	NCAP	3T EN

	16	17–23	24–25	26	27	28	29	30	31
R W	2T_EN	BA_INTLV_CTL	—	x32_EN	PCHB8	HSE	—	MEM_HALT	BI

Figure 8. DDR SDRAM Control Configuration Register (DDR_SDRAM_CFG)

Table 9 describes the DDR_SDRAM_CFG register fields.

Table 9. DDR_SDRAM_CFG Register field descriptions

Bits	Name	Description
0	MEM_EN	DDR SDRAM interface logic enable Clear this bit first. After all the DDR controller registers are configured, there must be at least a 500 μs delay before this bit is set. This bit enables the memory controller; therefore, all the registers must be configured. There must also be a delay to ensure that the JEDEC requirement of at least 500 μs from the deassertion of RESET to DRAM until CKE can be active has been met before the memory controller begins its initialization process. An example of an acceptable sequence where MEM_EN is set is as follows: 1. Perform POR or an HRESET. From assertion of HRESET, MCKE = 0 until MEM_EN is set. 2. Assert the DDR3 DRAM reset signal. Assertion of DRAM reset can be done with HRESET assertion. 3. Wait 200 μs before deasserting DRAM reset. 4. Write all DDR registers in memory controller as described in the applicable device reference manual and in this application note, except for MEM_EN bit. 5. Wait 500 μs. All DDR registers except the MEM_EN bit must be set before this 500-μs wait. 6. Set MEM_EN = 1. This causes the memory controller to perform the initialization sequence. 7. Once the initialization sequence is complete, the memory controller is ready for normal operation
1	SREN	self-refresh enable SREN must be enabled (SREN = 1) for the self-refresh command to be issued. There are three ways to enter self-refresh mode: core going to sleep (by power management), software forced (by enabling FRC_SC), external hardware interrupt (by enabling SR_IE). If SREN is disabled (SREN = 0) and any self-refresh entry modes are applied, only MCKE is negated and a self-refresh command is not issued.
2	ECC_EN	ECC enable Note that when HID1[RFXE] = 1, uncorrectable read errors (that is, multi-bit errors) cause the assertion of *core_fault_in*, which causes the core to generate a machine check interrupt unless HID1[RFXE] is disabled (by clearing HID1[RFXE] = 0). If RFXE is zero and an uncorrectable read error occurs, ERR_DISABLE[MBED] must be cleared and ERR_INT_EN[MBEE] and ECC_EN must be set to ensure an interrupt is generated. 0 No ECC errors are reported. No ECC interrupts are generated. (ECC is disabled). 1 ECC is enabled.

Table 9. DDR_SDRAM_CFG Register field descriptions (continued)

Bits	Name	Description
3	RD_EN	Registered DIMM enable Memory DIMM is either registered or unbuffered. This information is obtained from the DIMM manufacturer data sheet. A registered DIMM has an additional latch operation. This operation is used to buffer the address and command signals, and then re-issue them all at the same time with clock centered to all buffered signals. RD_EN informs the controller that registered DIMMs are used so it can account for one clock cycle delay automatically. If a registered DIMM is used, consult the DRAM data sheet to ensure if 2T or 3T timing is allowed before setting the DDR_SDRAM_CFG[2T_EN] and DDR_SDRAM_CFG[3T_EN] registered fields. In cases where 2T and 3T timing is not allowed, these fields should be cleared, which means 1T timing should be used.
4	—	Reserved
5–7	SDRAM_TYPE	Type of SDRAM device to be used The controller applies different processes for different types of memory. This field informs the controller of the type of memory with which it is to communicate.
8–9	—	Reserved
10	DYN_PWR	Dynamic power management mode 0 Dynamic power management mode is disabled. 1 Dynamic power management mode is enabled. If there is no ongoing memory activity, the SDRAM CKE signal is negated.
11–12	DBW	DRAM data bus width 00 64-bit bus is used. 01 32-bit bus is used. 10 16-bit bus is used.
13	8_BE	8-beat burst enable 0 4-beat bursts are used on the DRAM interface. 1 8-beat bursts are used on the DRAM interface. For all PowerQUICC/QorIQ parts other than P4080: • If a 64-bit data bus is used (that is, DDR_SDRAM_CFG[DBW] = 00,) then this field must be set to 0 (4-beat burst). • If a 32-bit data bus is used, then this field should be set to 1 (8-beat burst). • If a 16-bit data bus option is available and used, this field should be set to 1 (8-beat burst). For P4080 parts: • This field should be set to 1 (8-beat burst).
14	NCAP	Non-concurrent auto-precharge Some older DDR DRAMs do not support concurrent auto precharge. If one of these older DRAM devices is used, this bit should be set. Otherwise, in most cases where concurrent auto precharge is supported, this bit should be cleared.
15	3T_EN	Enable 3T timing This field cannot be set if DDR_SDRAM_CFG[2T_EN] is also set, and cannot be used with a 32-bit bus if 4-beat bursts are used. When this field is set, the DRAM command/address are held for 3 full cycles on the DRAM bus for every DRAM transaction. However, the chip select is only held for the third cycle. **Note:** 3T timing may not be used with 4-beat bursts, unless DDR_SDRAM_CFG_2[OBC_CFG] is set. **Note:** When registered DIMMs are used, consult the data sheet to determine if 3T timing is allowed before enabling this field.

Table 9. DDR_SDRAM_CFG Register field descriptions (continued)

Bits	Name	Description
16	2T_EN	Normally, 1T is used, which means address and control signals are on for 1 clock cycle. The 2T selection is used when there are timing issues that require 2 clock cycles for the address and control signal to last. This selection is typically used for heavily loaded systems, such as those with two unbuffered DIMMS. **Note:** When registered DIMMs are used, consult the data sheet if 2T timing is allowed before enabling this field.
17–23	BA_INTLV_CTL	Bank (chip-select) interleaving control If more than one chip-select is used, bank interleaving can be enabled.
24–25	—	Reserved
26	x32_EN	x32 enable As stated in the applicable device reference manual, if zero is selected, either x8 or x16 discrete DRAM chips are used. Each data byte has a dedicated corresponding data strobe. • If x8 DRAM, then DQS0 is used to capture DQ[0:7], and DQS1 for DQ[8:15, …, DQS7 for DQ[56:63], and DQS8 is used to capture ECC[0:7]. • If x16 DRAM, DQS0 is used to capture DQ[0:7], DQS1 for DQ[8:15], DQS2 for DQ[16: 23],..., DQS6 for DQ[48:55], DQS7 for DQ[56:63], and DQS8 is used to capture ECC[0:7]. • If this bit is set, one x32 discrete DRAM chip is used. In this mode, DQS0 is used to capture DQ[0:31], DQS4 is used to capture DQ[32:63], and DQS8 is used to capture ECC[0:7].
27	PCHB8	Precharge bit 8 enable As stated in the applicable device reference manual, if x32_EN is cleared, PCHB8 should also be clearedl. 0 MA[10] is used to indicate the auto precharge and precharge all commands. 1 MA[8] is used to indicate the auto precharge and precharge all commands.
28	HSE	Global half-strength override This value can be modified based on the required drive strength. Half strength may work better when the memory load is light, for example, if one chip-select or one DIMM is used. If two DIMMs (or multiple chip selects) are used, the full-strength selection may be a better choice. This field selection is ignored (not applicable) if either bits 1 or 2 of the DDRCDR is set (hardware or software impedance auto calibration is enabled). However, if the impedance auto calibration is disabled, bits 1 and 2 of the DDRCDR are cleared this field are effective and the half or full-strength drive bit is set based on the selection HSE field. The half-strength drive load value is 40 Ω when DDR3 is used.
29	—	Reserved
30	MEM_HALT	DDR memory controller halt When this field is set. the memory controller does not accept a new transaction until it is cleared. This bit can be used when bypassing initialization and forcing MODE REGISTER SET and EXTENDED MODE REGISTER SET commands through software.
31	BI	Bypass initialization 0 The DDR controller cycles through initialization routine based on SDRAM_TYPE. 1 Initialization routine is bypassed. Software is responsible for initializing memory through DDR_SDRAM_MD_CNTL register.

2.9 DDR_SDRAM_CFG_2

The DDR SDRAM control configuration register 2 (DDR_SDRAM_CFG_2) is shown in Figure 9.

Offset 0x114 Access: Read/Write

	0	1	2	3	4	5	6	8	9	10	11	15
R	FRC_SR	SR_ IE	DLL_RST _DIS	—	DQS_CFG		—		ODT_CFG		—	
W												

	16	19	20	21	22	23	24	25	26	27	28	29	30	31
R	NUM_PR		—		QD_ EN	UNQ_ MRS_ EN	—	OBC_ CFG	AP_ EN	D_ INIT	—	RCW _ EN	CD_ DIS	MD_ EN
W														

Figure 9. DDR SDRAM Control Configuration Register 2 (DDR_SDRAM_CFG_2)

Table 10 describes the DDR_SDRAM_CFG_2 fields.

Table 10. DDR_SDRAM_CFG_2 field descriptions

Bits	Name	Description	Recommended setting
0	FRC_SR	Force self-refresh 0 The DDR controller operates in normal mode 1 The DDR controller enters self-refresh mode.	—
1	SR_IE	Self-refresh interrupt enable. The DDR controller can be placed in self-refresh mode by asserting a panic interrupt. DDR_SDRAM_CFG[SREN] must also be set when the panic interrupt is used.	—
2	DLL_RST_DIS	DLL reset disable As stated in the applicable device reference manual, the DDR controller typically issues a DLL reset to the DRAMs when exiting self-refresh. However, this function can be disabled by setting this bit during initialization. 0 The DDR controller issues a DLL reset to the DRAMs when exiting self-refresh. 1 The DDR controller does not issue a DLL reset to the DRAMs when exiting self-refresh.	—
3	—	Reserved	—
4–5	DQS_CFG	DQS configuration For DDR3, this field should always be set to 01, which indicates that a differential strobe signal is used.	—
6–8	—	Reserved	—
9–10	ODT_CFG	ODT configuration refers to the termination at the on-chip I/O (memory controller side). This field should be set to assert ODT to internal IOs only during reads to DRAM. Therefore, the value of 0b10 is recommended for this field, regardless of DDR3 SDRAM topology.	0b10 is recommended.
11–15	—	Reserved	—

Table 10. DDR_SDRAM_CFG_2 field descriptions (continued)

Bits	Name	Description	Recommended setting
16–19	NUM_PR	Number of posted refreshes The value of this field is application-dependent. It may be desirable to use more than one, which allows the refresh interval to be programmed to be longer. For example, if two are used, two refresh commands are issued to all enabled chip selects each time the refresh interval expires (two rows are refreshed). The benefit is that the controller can leave pages open longer before closing them and starting the refresh sequence. The one issue with posted refreshes is that the worst-case latency for a read can be worse because the controller keeps all pages closed while it issues the consecutive posted refreshes. In addition, configuring this field to 0b0000 does the same thing as configuring it to 0b0001. However, it is a better programming practice for one refresh command to be issued during each refresh sequence, therefore, give this field a value of 1 rather than 0. This field refers to the number of refreshes to be issued each refresh sequence. Therefore, if 8 is set, 8 consecutive refreshes are issued at each refresh sequence. The advantage of having more than one refresh would be observed for a smaller number of refesh recoveries, and precharged would be used. Some performance increases result. However, the controller will be unavailable for longer period of time in order to complete the consecutive refreshes. If application is time-delay-sensitive (that is, if the time it takes to complete the selected number of consecutive refreshes is longer than system can tolerate), it would cause a system failure.	—
20–21	—	Reserved	—
22	QD_EN	Quad-rank enable If available, this field should be set only when a quad-ranked DIMM is used. This bit must be cleared if quad-ranked DIMM is not used.	—
23	UNQ_MRS_EN	Unique MRS enable If available, this field determines if the DDR_SDRAM_MODE_{3.8} registers are used when initializing the memories for chip selects 1, 2, and 3. These can be used to provide unique values to the mode registers of the DRAM to allow different termination values for each rank.	—
24	—	Reserved	—
25	OBC_CFG	On-the-fly burst chop configuration. This bit determines if on-the-fly burst chop is used. This bit should only be set if DDR3 memories are used. If on-the-fly burst chop mode is not used with DDR3 memories, then fixed burst chop mode may be used if the proper turnaround times are programmed into TIMING_CFG_0 and TIMING_CFG_4. In addition, for parts other than P4080, DDR_SDRAM_CFG[8_BE] should be cleared for both on-the-fly burst chop mode or fixed burst chop mode when using a 64-bit data bus with DDR3 memories.	—
26	AP_EN	Set this bit to enable parity error checking. Only registered DIMMs provide an even parity error check function for the control, command, and address bus. Two pins called Par_In and Err_Out are used to perform this function. Par_In pin is used for the memory controller to send the even parity bits and any detected error is flagged on the Err_Out pin by the registered DIMM. If parity error checking is not used in a registered DIMM, disable this bit and leave the Par_In and Err_Out pins as no connects. for correct termination refer to the applicable device design checklist.	—

Table 10. DDR_SDRAM_CFG_2 field descriptions (continued)

Bits	Name	Description	Recommended setting
27	D_INIT	DRAM data initialization As stated in the applicable device reference manual, software sets this bit and hardware clears it. If software sets this bit before the memory controller is enabled, the controller automatically initializes the entire DRAM after it is enabled. Hardware automatically clears this bit when initialization completes. When this bit is cleared, no data initialization is in progress, and no data initialization is scheduled. This bit remains set until the initialization is complete. The value in DDR_DATA_INIT is used to initialize memory.	—
28	—	Reserved.	
29	RCW_EN	If DDR3 registered DIMMs are used, set this field to enable the controller to program the RDIMM with the register control words.	—
30	CD_DIS	If this bit is set, the corrupted data feature will be disabled. When the corrupted data feature is enabled, the DDR controller inverts the generated ECC code for any beat of data known to have corrupted data. When a read to the corrupted data is later generated, and error reporting is enabled, the ERR_DETECT[CDE] error will be set.	—
31	MD_EN	Set this bit if mirrored DIMM is used.	—

2.10 DDR SDRAM Mode Configuration Register (DDR_SDRAM_MODE)

As specified in the JEDEC standard, every DDR3 SDRAM has a mode and an extended mode register. The controller must configure the value of these registers in DDR3 memory during initialization. The range (and meaning) of legal values is specified by the DDR memory manufacturer. Therefore, review these two registers in the manufacturing data sheet before selecting the settings for the DDR SDRAM mode configuration register (DDR_SDRAM_MODE), shown in Figure 10. Note that the big-endian convention is used for this register (0 is high, 31 is low). In addition, values selected for the fields of these two registers should be the same and not different from the corresponding values in the controller register fields. For example, the $\overline{\text{CAS}}$ value selected in TIMING_CFG_1[CASLAT] should be the same as the value in the corresponding field, DDR_SDRAM_MODE[SDMODE]. The decoding for the mode and extended mode provided applies only to DDR3 SDRAM.

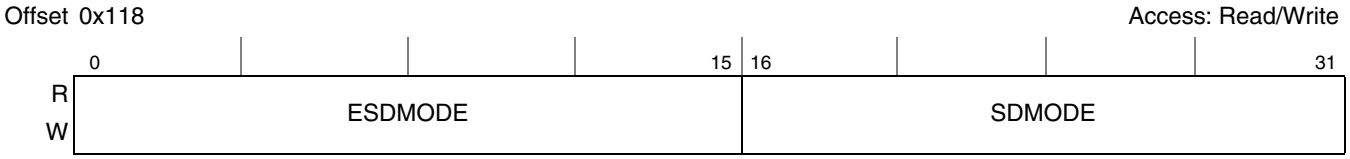

Figure 10. DDR SDRAM Mode Configuration Register (DDR_SDRAM_MODE)

Table 11 describes the DDR_SDRAM_MODE fields.

Table 11. DDR_SDRAM_MODE field descriptions

Bits	Name	Description	Recommended setting
0–1	ESDMODE [MRS]	The DDR controller automatically sets the MBA bits, which are used to determine which mode register is written. The values written to the extended mode register affect only the MA pins. Although the BA bits are automatically set, reading this register should provide the same data that was originally written to it.	01 Select the extended mode register, default
2	ESDMODE	Extended SDRAM mode. Reserved, should be set to 0.	0 Default value
3	ESDMODE [Q off]	0 Enables the output 1 Disables the output	0 Default value
4	ESDMODE [TDQS]	This bit should be cleared. The Freescale memory controller does not support TDQS.	0 Disable the TDQS
5	ESDMODE	Extended SDRAM mode. Reserved.	0 Default value
7	ESDMODE	Extended SDRAM mode. Reserved,	0 Default value
8	ESDMODE [WL]	Write leveling by the way of DRAMs. This bit should be set to 0. Memory controller does not use the write leveling by way of DRAMs; instead, it has a dedicated write leveling register (DDR_WRLVL_CNTL), which should be used if write leveling functionality is required.	0 Default value
6, 9, 13	ESDMODE [Rtt]	This field determines the DRAM on-die-termination value when DRAM ODT is enabled. The Rtt termination value applies to the DQ, DM, DQS, DQS#. There are several termination values available for selection. The selection of Rtt should be set based on system topology. Also, simulation results could be a good starting-point to select an appropriate DRAM termination values. Use registers CS*n*_CONFIG and TIMING_CFG_5 to determine when DRAM ODT is turned on or off. Use CS*n*_CONFIG to enable or disable the ODT setting on DRAM. Use TIMING_CFG_5 to determine when the ODT will be enabled and for how long it is applied.	001 60 Ω Rtt 010 120 Ω Rtt 011 40 Ω Rtt 100 20 Ω Rtt 101 30 Ω Rtt
11–12	ESDMODE [AL]	Additive latency This value should be identical to the value selected for SDRAM_TIMING_2[ADD_LAT].	00 Disabled 01 CL-1 10 CL-2
10,14	ESDMODE [ODS]	Depends upon system topology and frequency. There are two selections available. Simulation results should be a good starting-point for this setting. For lightly loaded systems (that is, one or two ranks), half drive strength may be used.	0 40 Ω Half drive strength 1 34 Ω full drive strength
15	ESDMODE [DLL]	Clear this bit. DLL should be enabled for normal operation. The main function of DLL is to synchronize the internal and external clocks in DDR3 DRAMs.	0 Normal operations
16–17	SDMODE [MR]	Clear this bit. However, it is ignored by the memory controller if it is accidentally set.	0 Mode Register
18	SDMODE	DDR_SDRAM mode. Reserved.	0 Default value
19	SDMODE [PD]	If dynamic power management is used (set in DDR_SDRAM_CFG), then the DRAM disables the DRAM DLL when using slow-exit active power-down. This yields more power savings.	0 Slow PD exit (use tXPDLL) 1 Fast PD exit (use tXP)

Table 11. DDR_SDRAM_MODE field descriptions (continued)

Bits	Name	Description	Recommended setting
20–22	SDMODE [WR]	Regardless of the value of DDR_SDRAM_CFG_2[OBC_CFG], the value of this bit should be based on the tWR obtained from the DRAM data sheet. When DDR_SDRAM_CFG_2[OBC_CFG] = 0, the value in this field should match the value of TIMING_CFG_1[WRREC]. But when DDR_SDRAM_CFG_2[OBC_CFG] = 1, the value in this field is two clock cycles value less than the value of TIMING_CFG_1[WRREC].	Write recover
23	SDMODE [DLL]	Clear this bit. The DDR controller should automatically reset the DRAM DLL during the initialization sequence.	0 Disable the DLL reset
24	SDMODE	Reserved	0 Default value
25–27, 29	SDMODE [CASLAT]	The value in this field must match the $\overline{\text{CAS}}$ latency programmed in TIMING_CFG_1. The DRAM data sheet should be consulted to select the proper $\overline{\text{CAS}}$ latency value.	$\overline{\text{CAS}}$ latency
28	SDMODE [BT]	This should be set to 0. Controller sets this value. Only sequential burst type is available in FSL memory controller.	Burst type 0 Sequential
30–31	SDMODE [BL]	The value in this field must match the Burst Length type programmed in the DDR_SDRAM_CFG_2[OBC_CFG]. Because the burst chop mode has a faster turn around times between read-write or write-read operations and also providing the flexibility to use 4- or 8-beat, on-the-fly burst-chop mode type is recommended, that is, DDR_SDRAM_CFG_2[OBC_CFG] = 1 and SDMODE[BL] = 01	Burst length type

2.11 DDR SDRAM Mode Configuration 2 Register (DDR_SDRAM_MODE_2)

As specified in the JEDEC standard, every DDR3 SDRAM has a mode register 2 and 3 (MR2 and MR3). The controller must configure the value of these registers in DDR3 memory during initialization. The range (and meaning) of legal values is specified by the DDR memory manufacturer. Therefore, review these two registers in the manufacturing data sheet before selecting the settings for the DDR SDRAM mode configuration 2 register (DDR_SDRAM_MODE), shown in Figure 11. Note that the big-endian convention is used for this register (0 is high, 31 is low). In addition, values selected for the fields of these two registers should be the same and not different from the corresponding values in the controller register fields. For example, the CWL value selected in TIMING_CFG_2[WR_LAT] should be the same as the value in the corresponding field, DDR_SDRAM_MODE[ESDMODE2]. The decoding for the mode and extended mode provided here applies only to DDR3 SDRAM.

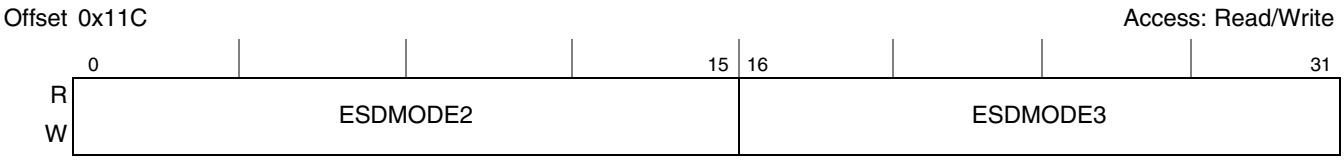

Figure 11. DDR SDRAM Mode Configuration 2 Register (DDR_SDRAM_MODE_2)

Table 12 describes the DDR_SDRAM_MODE_2 fields.

Table 12. DDR_SDRAM_MODE_2 field descriptions

Bits	Name	Description	Recommended setting
0–1	ESDMODE2 [MRS]	The DDR controller automatically sets the MBA bits, which are used to determine which mode register is written. The values written to the extended mode register affect only the MA pins. Although the BA bits are automatically set, reading this register should provide the same data that was originally written to it.	10 Select the extended mode register (MR2), default
2–4	ESDMODE2	Extended SDRAM mode. Reserved	0 Default value
5–6	ESDMODE2 [Rtt_wr]	Dynamic ODT can be enabled/disabled by this field. This field is used when two DIMM slot are used. When this field is enabled with two DIMM slots, for better signal integrity, during a write cycle, the value of ODT in this field is dynamically assigned to the unused DIMM slot. No other setting is required for this action to take place. Simply setting a value for this field will enable this feature in the DDR3 DRAMs. RZQ is the value of resistor externally connected to the RZQ pin of the DRAM. the value of RZQ resistor is 240 Ω. 00 Rtt_wr disabled 01 RZQ/4 10 RZQ/2 11 Reserved	0 Default value
7	ESDMODE2	Extended SDRAM mode. Reserved, should be set to 0.	0 Default value
8	ESDMODE2 [SRT]	Self-refresh Temperature. This is a DRAM related temperature setting operation during self-refresh. See the DRAM vender data sheet for details. A default value of 0 corresponds to the operation in 0 C to 85 C degrees.	0 Default value
9	ESDMODE2 [ASR]	Auto Self-Refresh (optional). See the DRAM data sheet for details and when and how to set this field. Default value of 0 corresponds to SRT default value.	0 Default value
10–12	ESDMODE2 [CWL]	CAS Write Latency (CWL). The value in this field must match the Write_latency programmed in TIMING_CFG_2[WR_LAT]. The DRAM data sheet should be consulted to select the proper CWL value.	—
13–15	ESDMODE2	Reserved	0 Default value
16–17	ESDMODE3 [MRS]	The DDR controller automatically sets the MBA bits, which are used to determine which mode register is written. The values written to the extended mode register affect only the MA pins. Although the BA bits are automatically set, reading this register should provide the same data that was originally written to it.	11 Select the extended mode register (MR3), default
18–28	ESDMODE3	Reserved	0 Default value
29	ESDMODE3 [MPR]	Clear this field. Controller sets this value. Only sequential burst type is available in FSL memory controller.	0 Default value
30–31	ESDMODE3 [MPR_RF]	Clear this field. Controller sets this value. Only sequential burst type is available in FSL memory controller.	0 Default value

2.12 DDR SDRAM Interval Configuration Register (DDR_SDRAM_INTERVAL)

The DDR SDRAM interval configuration register (DDR_SDRAM_INTERVAL) is shown in Figure 12.

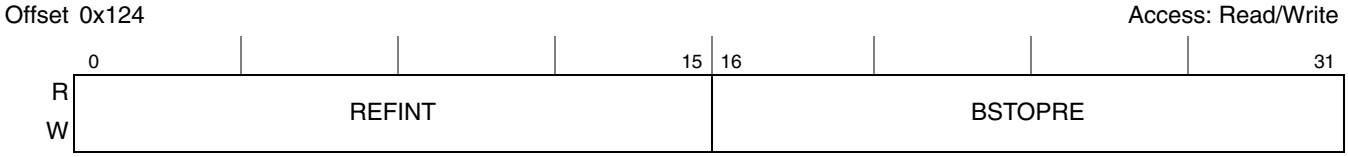

Figure 12. DDR SDRAM Interval Configuration Register (DDR_SDRAM_INTERVAL)

Table 13 describes the DDR_SDRAM_INTERVAL fields.

Table 13. DDR_SDRAM_INTERVAL field descriptions

Bits	Name	Description
0–15	REFINT	Refresh interval The refresh interval should be set as high as allowable by the DRAM specifications. This should be calculated by using tREFI in the DRAM specifications, which may depend on the operating temperature of the DRAM. In addition, to allow a memory transaction in progress to be completed when the refresh interval is reached and not violate the device refresh period, set the REFINT value to a value less than that calculated by using tREFI. If the DDR_SDRAM_CFG[NUM_PR] has a value higher than 1, the value selected for REFINT could be larger than tREFI. To calculate the max possible value when DDR_SDRAM_CFG[NUM_PR] is higher than 1, use the following formula: (tREFI/clk period) x (NUM_PR) = REFINT
16–31	BSTOPRE	Precharge interval The interval in memory bus clocks in which a page is kept open. The length of this interval is application-dependent. If the application software performs random memory access, this setting is not very important. However, if the software application uses a table lookup (same values in an already open page can be reused), the time that an already open page is kept open can help performance. If 0 is selected for this field then the DDR memory controller is in auto-precharge mode. When in auto-precharged mode, after every read or write operation, a memory page is opened and closed after completion. In contrast, if the memory controller is not in auto-precharge mode when a memory page is opened, it stays open for the number of clock cycles stated by this field.

2.13 DDR SDRAM Clock Register (DDR_SDRAM_CLOCK_CNTL)

The DDR SDRAM clock register (DDR_SDRAM_CLOCK_CNTL) is shown in Figure 13.

Figure 13. DDR SDRAM Clock Register (DDR_SDRAM_CLOCK_CNTL)

Table 14 describes the DDR_SDRAM_CLOCK_CNTL fields.

Table 14. DDR_SDRAM_CLOCK_CNTL field descriptions

Bits	Name	Description
0–4	—	Reserved
5–8	CLK_ADJ	Clock adjustment For lightly loaded systems (where ADDR/CMD and clock are fairly equally loaded in the system), this field is probably set to ½ DRAM cycle most of the time. This setting can be used to better center the output clock inside the ADDR/CMD valid eye at the DRAM. If the ADDR/CMD is more heavily loaded than the clock, values higher than ½ typically need to be used. For details, refer to Section 4.2, “CAS to Preamble Calculation” in application note *Programming the PowerQUICC™ III/PowerQUICC™ II Pro DDR SDRAM Controller* (AN2583). In addition, note that CLK_ADJUST shifts MCK/MCK_B (clock) with respect to where the ADDR/CMD (address/command) was launched. In contrast, WR_DATA_DELAY shifts transmit DQS/DQS_B/DQ/ECC/DM with respect to where the ADDR/CMD is launched. So, if WR_DATA_DELAY is not changed to match the CLK_ADJUST change, an offset is added between MCK and DQS.
9–31	—	Reserved

2.14 Configuration 4 Register (TIMING_CFG_4)

The DDR SDRAM timing configuration 4 register (TIMING_CFG_4), shown in Figure 14, sets the number of clock cycles between various SDRAM control commands.

Offset 0x160 Access: Read/Write

	0–3	4–7	8–11	12–15	16–29	30–31
R W	RWT	WRT	RRT	WWT	—	DLL_LOCK

Figure 14. DDR SDRAM Timing Configuration 4 Register (TIMING_CFG_4)

Table 15 describes the TIMING_CFG_4 fields.

Table 15. TIMING_CFG_4 field descriptions

Bits	Name	Description	Recommended setting
1–3	RWT	Read-to-write turnaround for same chip select. This field specifies how many cycles are added between a read-to-write turnaround for transactions to the same chip select. If a value of 0000 is chosen, then the DDR controller uses the value used for transactions to different chip selects, as defined in TIMING_CFG_0[RWT].	0 is recommended
4–7	WRT	Write-to-read turnaround for same chip select. This field specifies how many cycles are added between a write-to-read turnaround for transactions to the same chip select. If a value of 0000 is chosen, then the DDR controller uses the value used for transactions to different chip selects, as defined in TIMING_CFG_0[WRT].	0 is recommended
8–11	RRT	Read-to-read turnaround for same chip select. This field specifies how many cycles are added between reads to the same chip select. When burst-chop mode is used (that is, on-the-fly burst-chop or fixed burst-chop mode) this field must be set to a minimum value of 4’b0010. When a fixed 8-beat burst is selected, then this field should be cleared.	• With burst-chop mode use 4’b0010. • With fixed 8-beat burst use 4’b0000.
12–15	WWT	Write-to-write turnaround for same chip select. This field specifies how many cycles are added between writes to the same chip select. When burst-chop mode is used (that is, on-the-fly burst-chop or fixed burst-chop mode) this field must be set to a minimum value of 4’b0010. When a fixed 8-beat burst is selected, then this field should be cleared.	• With burst-chop mode use 4’b0010. • With fixed 8-beat burst use 4’b0000.
16–29	—	Reserved	0 Default value
30–31	DLL_LOCK	DDR SDRAM DLL lock time This provides the number of cycles that it takes for the DRAMs DLL to lock at POR and after exiting self-refresh. The controller waits the specified number of cycles before issuing any commands after exiting POR or self-refresh. The minimum requirement for DDR3 is 512 clock cycles.	2’b01, or 512 clock cycles for DDR3

2.15 DDR SDRAM Timing Configuration 5 Register (TIMING_CFG_5)

The DDR SDRAM timing configuration 5 register (TIMING_CFG_5). shown in Figure 15, sets the number of clock cycles between various SDRAM control commands.

Offset 0x164 Access: Read/Write

	0 2	3 7	8	9 11	12 14	15 19	20	21 23	24 31
R W	—	RODT_ON	—	RODT_OFF	—	WODT_ON	—	WODT_OFF	—

Figure 15. DDR SDRAM Timing Configuration 5 Register (TIMING_CFG_5)

Table 16 describes the TIMING_CFG_5 fields.

Table 16. TIMING_CFG_5 field descriptions

Bits	Name	Description	Recommended setting
0–2	—	Reserved	—
3–7	RODT_ON	Read to ODT on for DRAM This field specifies the number of cycles that pass from when a read command is placed on the DRAM bus until the assertion of the relevant ODT signal(s). In most cases DRAM ODT should be disabled during read cycles. If ODT to DRAM during the read cycle is not used, this field should be cleared.	0 is recommended
8	—	Reserved	—
9–11	RODT_OFF	Read to ODT off for DRAM This field specifies the number of cycles that the relevant DRAM ODT signal(s) remain asserted for each read transaction. In most cases, DRAM ODT should be disabled during read cycles. If ODT to DRAM during a read cycle is not used, this field should be cleared.	0 is recommended
12–14	—	Reserved	—
15–19	WODT_ON	Write to ODT on for DRAM This field specifies the number of cycles that pass from when a write command is placed on the DRAM bus until the assertion of the relevant ODT signal(s). In most cases, ODT is asserted with or one cycle after the write command is placed on the DRAM bus. From the DDR3 DRAM data sheet, ODTL on (that is, ODTL on = WL – 2 = ODTLcnw) cycles is required before the Rtt is applied. A valid Rtt must be present when DQS preamble is arriving at DRAM which is WL – 1. This means for the minimum, the ODT signal needs to be asserted 1 cycle after the write command is issued. If additive latency (AL) is not cleared and a value of CL– 1 or CL – 2 is selected, then ODT command can be issued AL number of cycles after the write command.	If AL = 0 • 5'b00010 for 1 clock, or, • 5'b00001 for 0 clock If AL <> 0 • AL number of clocks after write command
20	—	Reserved	—
21–23	WODT_OFF	Write to ODT off for DRAM This field specifies the number of cycles that the relevant ODT signal(s) remain asserted for each write transaction. Select 4 clock cycles. The memory controller automatically adds 2 clock cycles when an 8-beat burst is used. Therefore, regardless of burst type selection, fixed 8-beat, fixed 4-beat burst chop, or on-the-fly burst chop mode value of 4 clock cycles should be selected for this field.	3'b100 for any burst type selected
24–31	—	Reserved	—

2.16 DDR ZQ Calibration Control Register (DDR_ZQ_CNTL)

The DDR ZQ calibration control register (DDR_ZQ_CNTL), shown in Figure 16, provides the enable and controls required for ZQ calibration.

Offset 0x170 Access: Read/Write

	0	1–3	4–7	8–11	12–15	16–19	20–23	24–31
R W	ZQ_EN		ZQINIT		ZQOPER		ZQCS	

Figure 16. DDR ZQ Calibration Control (DDR_ZQ_CNTL)

Table 17 describes the DDR_ZQ_CNTL fields.

Table 17. DDR_ZQ_CNTL field descriptions

Bits	Name	Description	Recommended setting
0	ZQ_EN	ZQ Calibration enable. This bit determines if ZQ calibrating is used. This bit should only be set if DDR3 memory is used (DDR_SDRAM_CFG[SDRAM_TYPE] = 3'b111). DDR3 uses an external resistor connected from the DRAM's ZQ pin to GND. the ZQ calibration is done to calibration the DRAM output drivers and ODT values. When ZQ calibration is enabled, the memory controller sends the appropriate commands to DRAM so it can conduct the calibration.	1 to enable ZQ calibration
1–3	—	Reserved	—
4–7	ZQINIT	POR ZQ calibration time (tZQinit). This field should be based on tZQinit.	From manufacturer's data sheet
8–11	—	Reserved	0
12–15	ZQOPER	Normal operation full calibration time (tZQoper). This field should be based on tZQoper.	From manufacturer's data sheet
16–19	—	Reserved	0
20–23	ZQCS	Normal operation short calibration time (tZQCS). This field should be based on tZQCS.	From manufacturer's data sheet
24–31	—	Reserved	0

2.17 DDR Write Leveling Control Register (DDR_WRLVL_CNTL)

The DDR write leveling control register (DDR_WRLVL_CNTL), shown in Figure 17, provides controls for write leveling.

Offset 0x174 Access: Read/Write

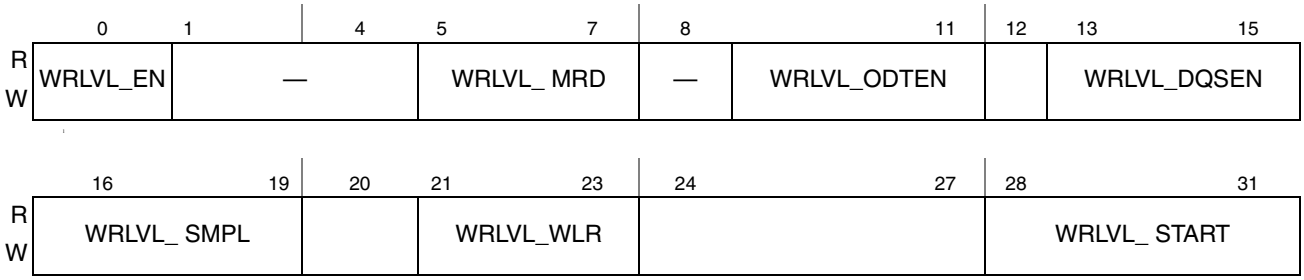

Figure 17. DDR Write Leveling Control Register (DDR_WRLVL_CNTL)

Table 18 describes the DDR_WRLVL_CNTL fields.

Table 18. DDR_WRLVL_CNTL field descriptions

Bits	Name	Description	Recommended setting
0	WRLVL_EN	Write leveling enable This bit determines if write leveling is used. If this bit is set, the DDR controller performs write leveling immediately after initializing the DRAM. This bit should only be set if DDR3 memory is used (DDR_SDRAM_CFG[SDRAM_TYPE] = 3'b111). In addition, write leveling is supported for both mirrored and non-mirrored DIMMs.	—
1–4	—	Reserved	—
5–7	WRLVL_MRD	First DQS pulse rising edge after margining mode is programmed (tWL_MRD). This field should be based on tWL_MRD.	From manufacturer's data sheet
8	—	Reserved	—
9–11	WRLVL_ ODTEN	ODT delay after margining mode is programmed This field should be set to a minimum of 16 clocks. The parameter tWL_ODTEN stated in the applicable device reference manual is removed from the recent JEDEC DDR3 specifications and hence it is not available in the DDR3 DRAM manufacturers data sheet. Programming this field to 16 clks is a requirement for the memory controller to correctly perform the write leveling function, rather than a JEDEC timing requirement.	3'b100 for 16 clocks
12	—	Reserved	—
13–15	WRLVL_ DQSEN	DQS/DQS delay after margining mode is programmed (tWL_DQSEN). This field should be based on tWL_DQSEN.	From manufacturer's data sheet
16–19	WRLVL_SMPL	Write leveling sample time This field determines the number of cycles that must pass before the data signals are sampled after a DQS pulse during margining mode. This field should be programmed to (tWLO + 6 clk) cycles.	From manufacturer's data sheet

Table 18. DDR_WRLVL_CNTL field descriptions (continued)

Bits	Name	Description	Recommended setting
20	—	Reserved	—
21–23	WRLVL_WLR	Write leveling repetition time This field determines the number of cycles that must pass between DQS pulses during write leveling. This field should be programmed to (tWLO + tWL_DQSEN + 6 clk) cycles.	From manufacturer's data sheet
24–27	—	Reserved	—
28–31	WRLVL_ START	Write leveling start time This field determines the value to use for the DQS_ADJUST for the first sample when write leveling is enabled during the initialization process. There are several valid selections for this field. Identify the valid values and select the center value to provide the best margins. For example, if values of 1/2, 5/8, and 3/4 clock delays produce a working DDR interface, a value of 5/8 clock delay should be selected.	—

2.18 DDR Control Words *n* Register (DDR_SDRAM_RCW_*n*)

The DDR_SDRAM_RCW_*n* register applies and is useful only when the following are true:

- The DDR3 registered DIMMs are used (that is, DDR_SDRAM_CFG[RD_EN] = 1)
- The default values of the register control words in the DDR3 registered DIMMs are not sufficient or acceptable for the customer-specific application.

There are a total of 16 RCW fields (4 bits each) in the DDR_SDRAM_RCW_*n* registers. When DDR_SDRAM_CFG[RCW_EN] is set during the initialization, the memory controller writes the DDR_SDRAM_RCW_*n* registers into the corresponding DDR3 DIMM register control words.

The RCW values in the RDIMM can be read via SPD located in SPD bytes 69–76. Each byte holds two RCW (that is, byte 69: RCW0 + RCW1; byte 70: RCW2 + RCW3,...). RCW 0–5 and 7–11 are JEDEC-predefined, and RCW 6, 7, and 12–16 are reserved and could contain vendor-specific information.

2.19 DDR Write Leveling Control 2 or 3 Register (DDR_WRLVL_CNTL_2 or 3)

If available, the DDR write leveling control 2 or 3 register sets adjustment for the DQS for each of the byte lanes individually. In memory controllers where these registers are available, each byte lane can be programmed to have a corresponding start delay for the very first write to the DDR3 DRAM. When write leveling is enabled the first write is used, during the initialization, in determining the skews introduced because of fly-by topology. DDR write leveling control 2 or 3 registers intended use are when there is no working values for DDR_WRLVL_CNTL[WRLVL_START] field. In memory controllers where these registers are not available, the value in DDR_WRLVL_CNTL[WRLVL_START] will be used to automatically determine the values for each of the byte lanes.

2.20 DDR SDRAM Mode Configuration (DDR_SDRAM_MODE_3...8)

If available, DDR_SDRAM_MODE_ 3...8 is a set of six registers used to load the mode configuration values for each individual chip select. This register is useful when different termination values (or perhaps other parameters) are desired for each individual chip select. In order for the controller to use these registers to individually program each chip select, DDR_SDRAM_CFG_2[UNQ_MSR_EN] should be set.

CAUTION

Do not set the common parameters (such as CAS_LAT) to different values. If this register is not available or not used, the DDR_SDRAM_MODE register will be used to program mode register in all chip selects.

2.21 DDR Control Driver Register 1 (DDRCDR_1)

DDR control driver register 1 (DDRCDR_1), shown in Figure 18, is used for the configuration of the driver strengths and on-die-termination (ODT) in the memory controller.

The list of available driver strengths is provided in the applicable device reference manual. The user can directly select and set an impedance driver from the list by writing to software driver calibration to override. Or use calibration to select an impedance driver that matches the value of resistors connected to MDIC[0:1] pins.

Calibrate the impedance values by using one of the following methods:

- Hardware calibration is done automatically by the memory controller during the initialization period by setting DHC_EN = 1. All DDR I/Os are set to the same calibrated value.
- Software calibration is achieved by following the procedure in the applicable device reference manual. Both hardware and software calibrations use the same process, but the hardware calibration is done automatically and software calibration is done by writing the software. The software calibration process must be done before the memory controller is enabled (that is, before MEM_EN = 1). All DDR I/Os are set to the same calibrated value.

If calibration is not used, or values other than calibrated values are desired, the driver strength values can be set in the following ways:

- Software can be overridden in the DDRCDR. The user can select from the available override impedance values in the DDRCDR to set driver strength. Set the DSO_x_EN fields with the desired value for the corresponding P and N fields. These settings should be set before the memory controller is enabled. The address and commands, data and strobe, and clock can have different driver strength settings.
- When DHC_EN, DSO_MDIC_EN and DSO_x_EN are cleared in the DDRCDR, the value in DDR_SDRAM_CFG[HSE] determines the driver strength.

Offset 0x174 Access: Read/Write

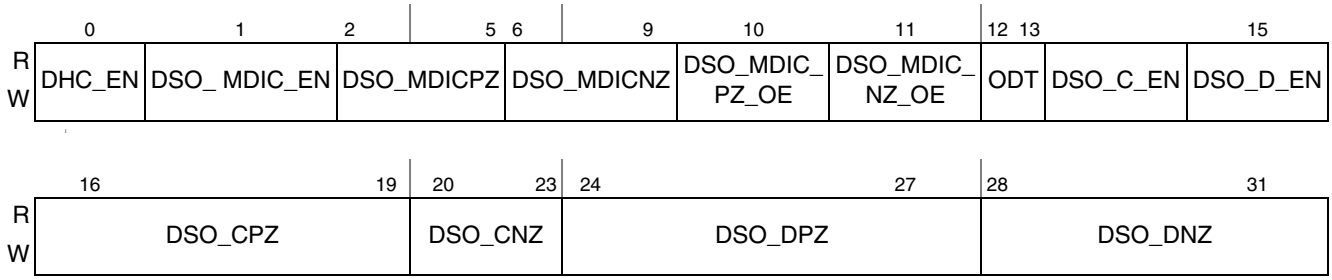

Figure 18. DDR SDRAM Control Driver 1 Register (DDRCDR_1)

Table 19 describes the DDRCDR_1 fields.

Table 19. DDRCDR_1 field descriptions

Bits	Name	Description
0	DHC_EN	By setting this bit, the hardware driver strength calibration takes place during the initialization of the memory controller. If the hardware driver strength calibration is desired, TIMING_CFG_1[DHC_EN] should be set before the memory controller is enabled (that is, DDR_SDRAM_CFG[MEM_EN] = 1). Ensure this field is cleared if software driver calibration is performed (that is, TIMING_CFG_1[DSO_MDIC_EN] is set).
1	DSO_MDIC_EN	Driver software override enable for memory driver impedance calibration. Follow the procedure provided in the applicable device reference manual to calibrate the drivers by software. By software calibration, all memory controller I/Os are calibrated to the same value.
2–5	DSO_MDICPZ	This field is used during the software driver calibration to override p-impedance.
6–9	DSO_MDICNZ	This field is used during the software driver calibration to override n-impedance.
10	DSO_MDIC_PZ_OE	This field is used during the software driver calibration to enable output to override p-impedance.
11	DSO_MDIC_NZ_OE	This field is used during the software driver calibration to enable output to override n-impedance.
12–13	ODT	ODT termination value for IOs in the memory controller This field is combined with DDRCDR_2[ODT] to determine the termination value. Note that the order of concatenation is (from left to right) DDRCDR_1[ODT], DDRCDR_2[ODT].
14	DSO_C_EN	Driver software override enable for address/command By setting this field to the value in the field, DSO_CPZ and DSO_CNZ is set for the address and command I/O driver strength.
15	DSO_D_EN	Driver software override enable for data/strobe/data mask By setting this field to the value in the field, DSO_DPZ and DSO_DNZ is set for the data/strobe/data mask I/O driver strength.
16–19	DSO_CPZ	This field is the value of p-impedance driver for address and command I/Os when TIMING_CFG_1[DSO_C_EN] is set.

Table 19. DDRCDR_1 field descriptions (continued)

Bits	Name	Description
20–23	DSO_CNZ	This field is the value of n-impedance driver for address and command I/Os when DSO_C_EN is set.
24–27	DSO_DPZ	This field is the value of p-impedance driver for data and strobe and data mask I/Os when DSO_D_EN is set.
28–31	DSO_DNZ	This field is the value of n-impedance driver for data and strobe and data mask I/Os when DSO_D_EN is set.

2.22 DDR SDRAM Control Driver 2 Register (DDRCDR_2)

The DDR SDRAM control driver 2 register (DDRCDR_2), shown in Figure 19, sets the number of clock cycles between various SDRAM control commands.

Offset 0xB2C — Access: Read/Write

	0	1–3	4–7	8–11	12–30	31
R	DSO_CLK_EN		DSO_CLKPZ	DSO_CLKNZ		ODT
W						

Figure 19. DDR SDRAM Timing Configuration 1 Register (DDRCDR_2)

Table 20 describes the DDRCDR_2 fields.

Table 20. DDRCDR_2 field descriptions

Bits	Name	Description
0	DSO_CLK_EN	Driver software override enable for clock By setting this field to value in the field, DSO_CLKPZ and DSO_CLKNZ are set for the clock I/O driver strength.
1–3	—	Reserved
4–7	DSO_CLKPZ	This field is the value of p-impedance driver for clock I/Os when DSO_CLK_EN is set.
8–11	DSO_CLKNZ	This field is the value of n-impedance driver for clock I/Os when DSO_CLK_EN is set.
12–30	—	Reserved
31	ODT	ODT termination value for IOs in the memory controller This field is combined with DDRCDR_1[ODT] to determine the termination value. Note that the order of concatenation is from left to right: DDRCDR_1[ODT], DDRCDR_2[ODT]

3 Revision history

This table provides a revision history for this application note.

Table 21. Document revision history

Rev. Number	Date	Description
4	11/2014	• In Table 7, “TIMING_CFG_1 field descriptions,” updated the WRREC field description. • In Table 11, “DDR_SDRAM_MODE field descriptions,” updated the WR field description.
3	01/2012	• In Table 11, “DDR_SDRAM_MODE field descriptions,” added the following field description for DDR_SDRAM_MODE[SDMODE]: “DDR_SDRAM mode. Reserved.” • In Table 11, “DDR_SDRAM_MODE field descriptions,” added bit 29 to the CASLAT field. • In Table 5, “TIMING_CFG_3 Register field descriptions,” updated the EXT_REFREC field bits from 12–15 to 11–15, and updated the field name from EXT_PREREF to EXT_REFREC. • In Table 6, “TIMING_CFG_0 field descriptions,” added information to the description and recommendation of WWT, RRT, RWT, and WRT fields. • In Table 7, “TIMING_CFG_1 field descriptions,” updated the PRETOACT field bits from 1–3 to 0–3, updated the ACTTOACT field bits from 25–27 to 24–27, and updated the WRTORD field bits from 29–31 to 28–31. • In Table 8, “TIMING_CFG_2 Register field descriptions,” updated the RD_TO_PRE field bits from 16-18 to 15-18, and updated the WR_DATA_DELAY field bits from 19–21 to 19–22. • In Section 2.19, “DDR Write Leveling Control 2 or 3 Register (DDR_WRLVL_CNTL_2 or 3),” added a sentence to clarify the intended use of these two registers, and modified the last sentence to clarify the descriptions of the WRLVL_START field. • In Figure 18, “DDR SDRAM Control Driver 1 Register (DDRCDR_1),” updated bit 14 to DSO_C_EN and bit 11 to DSO_MDIC_NZ_OE to conform with bit field descriptions. • In Table 4, “CSn_CONFG_2 Register field descriptions,” added the following sentence to the description of PARS_CFG: “When using self-refresh, setting this field allows the user to select a partial section of memory to be placed in self-refresh instead of the entire memory space.” • In Table 10, “DDR_SDRAM_CFG_2 field descriptions,” added the following text for the description of SR_IE: “Self-refresh interrupt enable. The DDR controller can be placed in self-refresh mode by asserting a panic interrupt. DDR_SDRAM_CFG[SREN] must also be set when the panic interrupt is used.” • In Table 10, “DDR_SDRAM_CFG_2 field descriptions,” added the following text for the description of RCW_EN: “If DDR3 registered DIMMs are used, set this field to enable the controller to program the RDIMM with the register control words.” • In Table 10, “DDR_SDRAM_CFG_2 field descriptions,” added the following text for the description of CD_DIS, “If this bit is set, the corrupted data feature will be disabled. When the corrupted data feature is enabled, the DDR controller inverts the generated ECC code for any beat of data known to have corrupted data. When a read to the corrupted data is later generated, and error reporting is enabled, the ERR_DETECT[CDE] error will be set.” • In Table 10, “DDR_SDRAM_CFG_2 field descriptions,” added the following text for the description of MD_EN: “Set this bit if mirrored DIMM is used.”
2	09/2010	• In Table 9, “DDR_SDRAM_CFG Register field descriptions,” modified the 8_BE (bit 13) field description. • In Table 11, “DDR_SDRAM_MODE field descriptions,” modified recommended settings for ESDMODE[ODS] (bits 10, 14) so that second encoding is 1. • In Table 16, “TIMING_CFG_5 field descriptions,” modified WODT_OFF (bits 15–19) field description by adding a parenthetical clarification about the type of burst-chop mode, if selected.In addition, updated WODT_OFF (bits 21–23) field description.

Table 21. Document revision history (continued)

Rev. Number	Date	Description
1	06/2010	In Section 1, "Configuration guidelines," changed the last sentence of the second sub-bullet to read as follows: "The DDR3-1067 is a common DDR3 memory, but per the JEDEC specification, DDR3-1067 (or any other JEDEC-compliant DDR3 DRAM) can operate at a data rate down to 600 Mbps."
0	01/2010	Initial public release

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