NXP

Freescale Semiconductor
Application Note

Layout Recommendations for the MC34848

1 Introduction

The 34848 is a high efficient eight-channel LED driver used in LCD backlight applications. It is designed to support up to 160mA per channel in scan mode and 80mA per channel in local dimming mode. However, it can be set to support higher LED currents (e.g. 120mA per each channel) and higher output voltages (e.g. 60V) which support higher power applications (e.g. 57W).

Using the device for high power applications requires having an optimized layout that can ensure proper device performance under extreme conditions. This application note provides general guidelines for laying out a proper PCB design in two-layers for the MC34848 device.

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2 Component (MC34848) Pad Design

The exposed pad provides the main thermal dissipation path for the device. Thermal performance of the QFN package mainly relies on the size of the exposed pad and the number of vias placed on the exposed pad (See **Figure 1**)
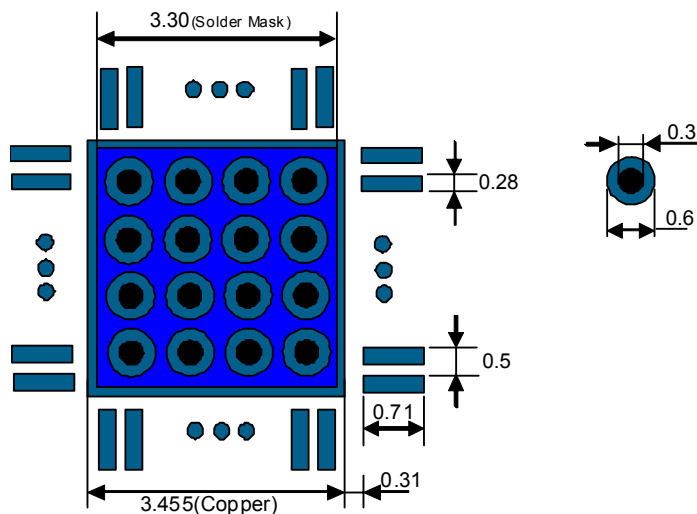
2.1 Detail Recommendations (Dimension: mm)

Figure 1. Recommended Via Placement

3   Components Placement

Noise Sensitive Components

- Compensation components (R, C on the COMP pin)
- OVP voltage divider resistors (resistors which connect to the OVP pin)
- CPLL components (R, C on the CPLL pin)
- R_{Iset} resistor (resistor which connect to the ISET pin)
- CS pin low-pass filter components

Noisy Components

- Power Inductor
- External NMOS (Boost Switch)
- Schottky Diode
- Input/Output Capacitor
- LEDs

Components need to be placed close to the IC (MC34848)

- All noise sensitive components
- DC decoupling capacitors (capacitors which connect between PVCC, DVDD and ground)
- Internal LDO output capacitor (capacitors which connect to VDC, VLOGIC pins)

Note: Place noisy components as far away as possible from all noise sensitive component and their traces. When noise traces and noisy sensitive traces cross each other on different layers of the PCB, ensure they are at a 45 or 90 degree angle from each other. This is to avoid possible noise coupling between the traces.

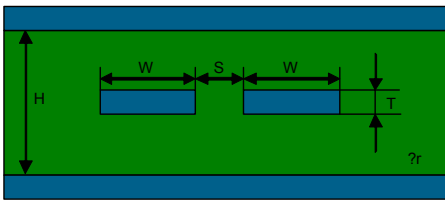# 4   Differential Traces Layout Considerations

Coupled Microstrip
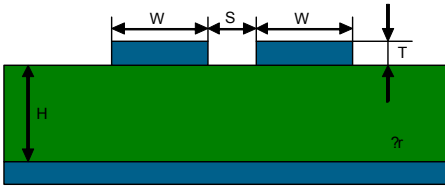
$$Z_{DIFF} \approx 2 \times Z_0 \left(1 - 0.48 e^{-0.96\frac{S}{h}}\right) \Omega$$

$$Z_0 = \frac{60}{\sqrt{0.457\varepsilon_r + 0.67}} \ell n \left(\frac{4h}{0.67(0.8W + t)}\right) \Omega$$

Coupled Stripline

$$Z_{DIFF} \approx 2 \times Z_0 \left(1 - 0.374 e^{-2.9\frac{S}{h}}\right) \Omega$$

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ell n \left(\frac{4b}{0.67\pi(0.8W + t)}\right) \Omega$$

Notes:

For FR-4, ε_r = 4.6, ZDIFF "Rterm., Zo" Rterm./2 (If the transmission impedance should be calculated from the transmission source (FPGA) or needs to subtract the calculated impedance as much as missing impedance).

The distance between two pairs should be > 2S.

The distance between a pair and a TTL/CMOS signal should be > 3S at a minimum. Even better, locate the TTL/CMOS signals on a different plane isolated by a ground plane or put ground trace between the pair and the TTL/CMOS signals at least.(In the case of a guard ground trace the distance should be >2S away).

It is recommended to keep S < W and S < h when designing for low EMI.

5   PCB Layout Recommendations

This section provides PCB layout recommendations (See **Figure 2**).
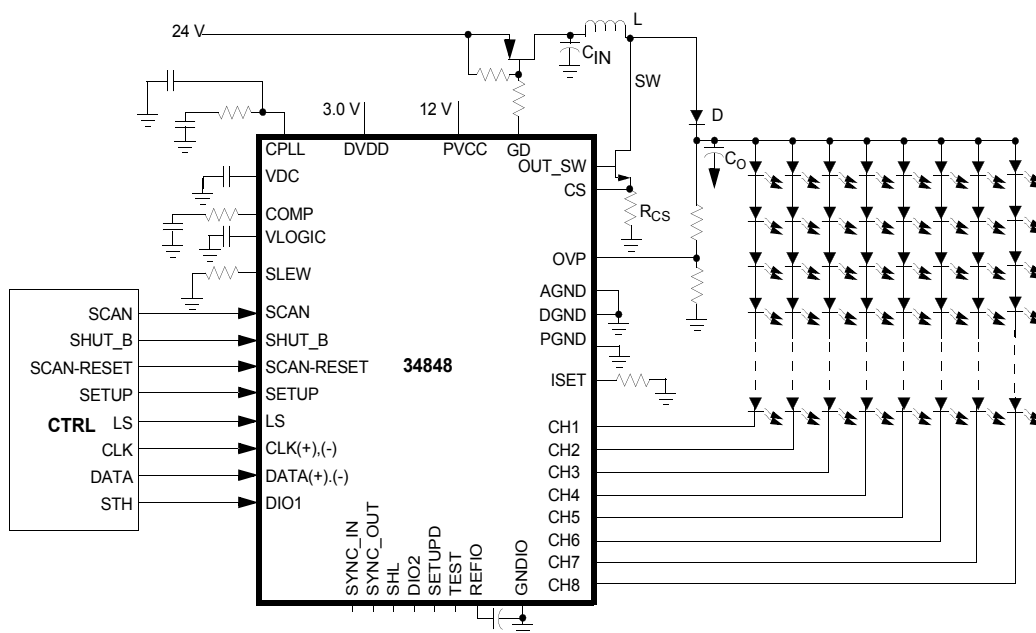
Figure 2. Simplified Application Drawing

1. Make the surface for the power line (between C_{IN}-L, L-D, (L,D) -SW Node, D-C_O, C_O-C_{IN}) and try to put it in one plane. Make this surface length as short and thick as possible and also make it as thick as possible (i.e. try to reduce the impedance of these surfaces).

2. Separate above listed power trace/surface from the sensitive trace or components.

3. Separate C_{IN}-C_O ground surface from the rest of other ground and connect this surface close (or between C_{IN} ground point and the connector ground surface) to the input connector ground pins.

4. Connect the R_{CS} resistor (current sense resistor) to the signal ground which is close to the IC ground.

5. Avoid the signal trace pass beneath the noisy inductor.

6. For traces which connected to PVCC, DVDD, CHx pins, use at least 12 mil width trace (For the multi IC applications, make as wide as possible). And, for the other traces, except differential signal (CLK+/-, DATA+/-), use at least 7 mil width trace. For traces connected to REFIO, VDC, VLOGIC pins, chose the width between 7~12 mil for the trace width (thicker than normal traces).

7. Underneath the exposed pad, put as large signal ground plain as possible to dissipate the heat generated by the IC. On the Exposed Pad, put at least 16 vias (drill: 0.3mm, pad: 0.6mm) (See **Figure 1**)

8. Put differential pairs in one plain and isolate the pair with the ground plains on the adjacent plain(s).

9. When connecting the Power surface/trace with 1oz copper thicknesses, use the following:
    The width of the surface/trace should be wider than 1mm/A.
    The connection of the power surface/trace should use multiple vias (as many as possible)

10. All the trace angles should be less than or equal to 45°C.

6   MC34848 Multi-EVB Layout Example

6.1   Assembly Layer Top, Silk Screen Top
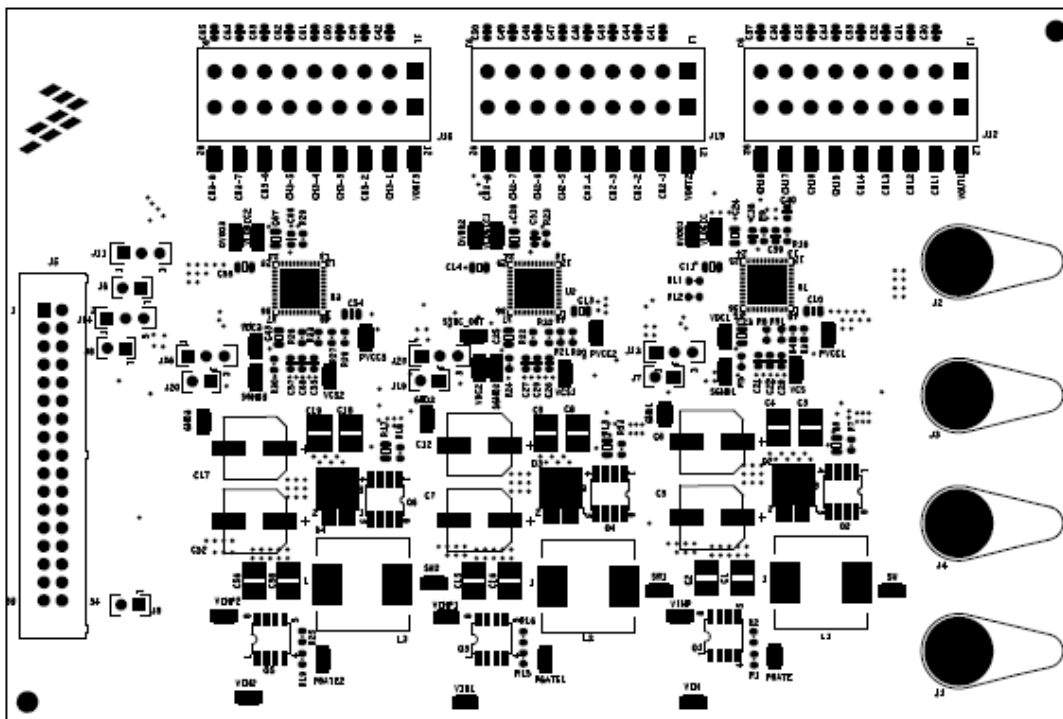
6.2   Top Layer Routing

Connect R_{CS} to the signal ground with the connection to the power ground. This is done to suppress the voltage difference of two different grounds, since this generates an error on the VCS reading which is used by the boost circuit (See PCB Layout Recommendations on page 5, Step 4)

Make as wide and short as possible for connecting the SW Node, power ground to suppress the noise generated by the huge switching current. (See PCB Layout Recommendations on page 5, Step 1)
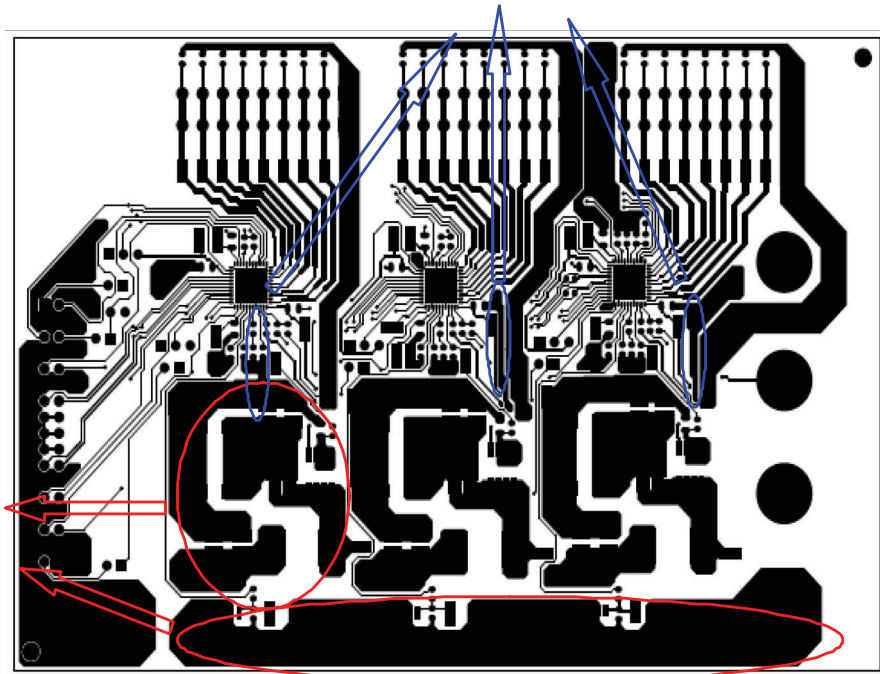
Figure 3. Top Layer Routing

6.3   Bottom Layer Routing

Underneath the exposed pad, put as large signal ground plain as possible to dissipate the heat generated by the IC. On the Exposed Pad, put at least 16 vias (drill: 0.3mm, pad: 0.6mm) (See PCB Layout Recommendations on page 5, Step 7)

Avoid the signal trace pass beneath the noisy inductor (See PCB Layout Recommendations on page 5, Step 5)
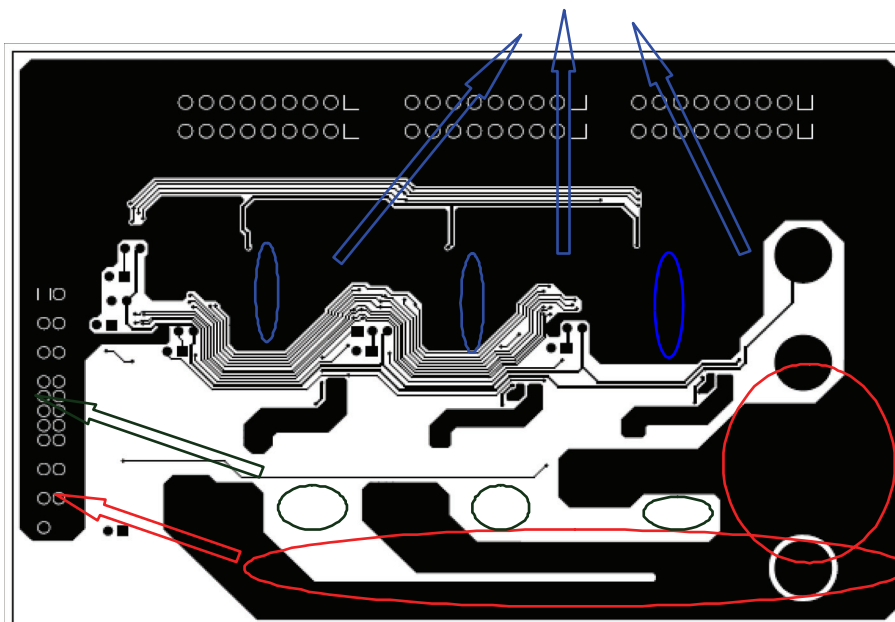
Separate C_{IN}-C_O ground surface from the rest of other ground and connect this surface close (or between C_{IN} ground point and the connector ground surface) to the input connector (See PCB Layout Recommendations on page 5, Step 3)

Figure 4. Bottom Layer Routing

6.4   Drill Data

On the exposed pad of the ICs, put at least 16 vias (Pad ≥ 0.6, Hole ≥ 0.6) to maximize the thermal performance of the ICs. (See PCB Layout Recommendations on page 5, Step 7)

Use multiple vias to connect between the power traces.
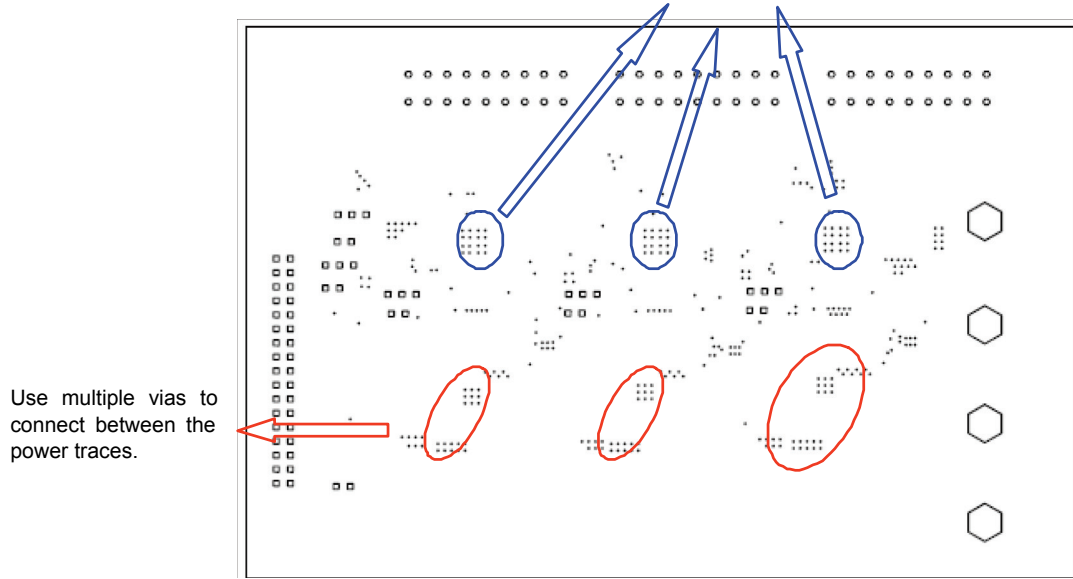
Figure 5. Drill Data

7 References

1. Quad Flat Pack No-Lead Application Note: AN1902

2. PCB Layout Design Guide for Analog Applications: AN3962

3. LVDS Owner's Manual _National Semiconductor: LVDS Owner's Manual 4th Edition

4. MC34848 Data sheet

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