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Application Note

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Hardware Design Guide

MPC5604E Microcontroller

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Contents

1 Introduction

The MPC5604E microcontroller is the newer member of the 32-bit microcontroller family built on Power Architecture® technology. This device is targeted at the chassis and safety market segment visual-based driver assistance, especially the CMOS Vision Sensor Gateway, Radar Sensor Gateway, and Infotainment Network Gateway.

The purpose of this application note is to describe possible hardware considerations for developing hardware design solutions. It covers topics such as clock generation, decoupling, and voltage regulator and power considerations. Detailed reference design schematics and descriptions of the main components are also contained within this document. Some hardware recommendations are also provided.

2 MPC5604E package option overview

The MPC5604E is available in two package options. All of the packages are Low-profile Quad Flat Packages (LQFP). Table 1 shows two available packages and the primary differences from the 64 LQFP standard package.

Table 1. MPC5604E package option

Package	Main difference
64 LQFP	Primary device with the base features.
100 LQFP	All features from 64 LQFP package extended for Nexus 2+. The 100-pin package is not a production package. It is used for software development only.

3 Power supply

The MPC5604E is designed for a wide range of applications. Based on system requirements and available power supplies, some applications may require different methods of powering the device. There are two options for powering the MCU. The first option requires a 3.3-V supply and few external components to power the MCU. In this case, the MCU will generate its own 1.2-V supplies. The second option is to provide 3.3V and 1.2V from an external power supply.

NOTE

The difference between the overall power dissipation of the MPC5604E in Internal Voltage Regulation mode and External Voltage Regulation mode is 4mA (extended power consumption for internal voltage regulation mode).

Recommended operating conditions are as follows:

- Internal Voltage Regulation mode: 3.0–3.6V
- External Voltage Regulation mode: 1.15–1.32V core voltage , 3.0–3.6V V_{DD_IO} +-10%

The MPC5604E has up to four power supply signals (depending on the selected voltage regulation mode).These signals, listed below, are internally multiple bounded to the internal power signals listed in Table 2.

1. V_{DD_HV}: I/O, flash memory, and oscillator voltage
2. V_{DD_LV} : core supply, PLL, and flash memory voltage
3. $V_{DD\_HV\_ADC}$: ADC0 supply
4. $V_{DD\_HV\_S\_BALLAST}$: ballast source/supply voltage

Table 2. External versus internal multiple-bounded power signals

Pin name	Pin number (64LQFP)	Internal signals multiple bounded	Nominal voltage	Description
$V_{DD\_HV\_S\_BALLAST}$	23	$V_{DD\_HV\_S\_BALLAST0\_1.2V}$	1.2V[1]	Internal Regulation mode: carries the entire core logic current.
		$V_{DD\_HV\_S\_BALLAST1\_1.2V}$		
		$V_{DD\_HV\_S\_BALLAST0\_3.3V}$	3.3V[2]	External Regulation mode: used as a signal to bypass regulator.
		$V_{DD\_HV\_S\_BALLAST1\_3.3V}$		
$V_{DD\_HV\_ADC}$	21	$V_{DD\_HV\_ADC0}$	3.3V	ADC0 supply voltage with respect to ground ($V_{SS\_HV\_ADC}$).
		$V_{DD\_HV\_ADR0}$		ADC0 high reference voltage with respect to ground ($V_{SS\_HV\_ADC}$).

Table continues on the next page...

Table 2. External versus internal multiple-bounded power signals (continued)

Pin name	Pin number (64LQFP)	Internal signals multiple bounded	Nominal voltage	Description
V_{DD_HV}	11	$V_{DD\_HV\_IO0\_0}$	3.3V	Input/output supply voltage (supply).
		$V_{DD\_HV\_OSC0}$		Crystal oscillator amplifier supply voltage.
	38	$V_{DD\_HV\_IO0\_2}$		Input/output supply voltage (supply).
		$V_{DD\_HV\_FLA1}$		Code and data flash supply voltage.
	55	$V_{DD\_HV\_IO0\_3}$		Input/output supply voltage (supply).
		$V_{DD\_HV\_FLA0}$		Code and data flash supply voltage.
V_{DD_LV}[3]	35	$V_{DD\_LV\_COR0\_1}$	1.2V	1.2-V supply pins for core logic and code flash. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR0\_1}$ pin.
		$V_{DD\_LV\_FLA1}$		Code and data flash supply voltage
	58	$V_{DD\_LV\_COR0\_2}$		1.2-V supply pins for core logic and code flash. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR0\_1}$ pin.
		$V_{DD\_LV\_FLA0}$		Code and data flash supply voltage
	7	$V_{DD\_LV\_COR0\_3}$		1.2-V supply pins for core logic and code flash. Decoupling capacitor must be connected between these pins and the nearest $V_{SS\_LV\_COR0\_1}$ pin.
		$V_{DD\_LV\_PLL}$		PLL supply voltage

1. Value valid for internal voltage regulation mode.
2. Value valid for external voltage regulation mode.
3. Requirement to use the smallest length of traces possible, and decoupling capacitors of 0.6 µF per pin must be placed near each pair of V_{DD_LV} / V_{SS} pins.

CAUTION

The MPC5604E requires high-voltage (V_{DD_HV}) and low-voltage (V_{DD_LV}) supply pins to be shorted on the board. The ADC supply ($V_{DD\_HV\_ADC}$) should be managed independently from other high-voltage supplies. (It may still be supplied from the same high-voltage source, but caution must be taken while routing it on the board).

3.1 External Voltage Regulation mode

In External Regulation mode, the core supply is provided externally using a switched regulator. This saves on-chip power consumption by avoiding the voltage drop over the ballast transistor. The external supply mode is selected via a board-level supply change at the $V_{DD\_HV\_S\_BALLAST}$ pin.

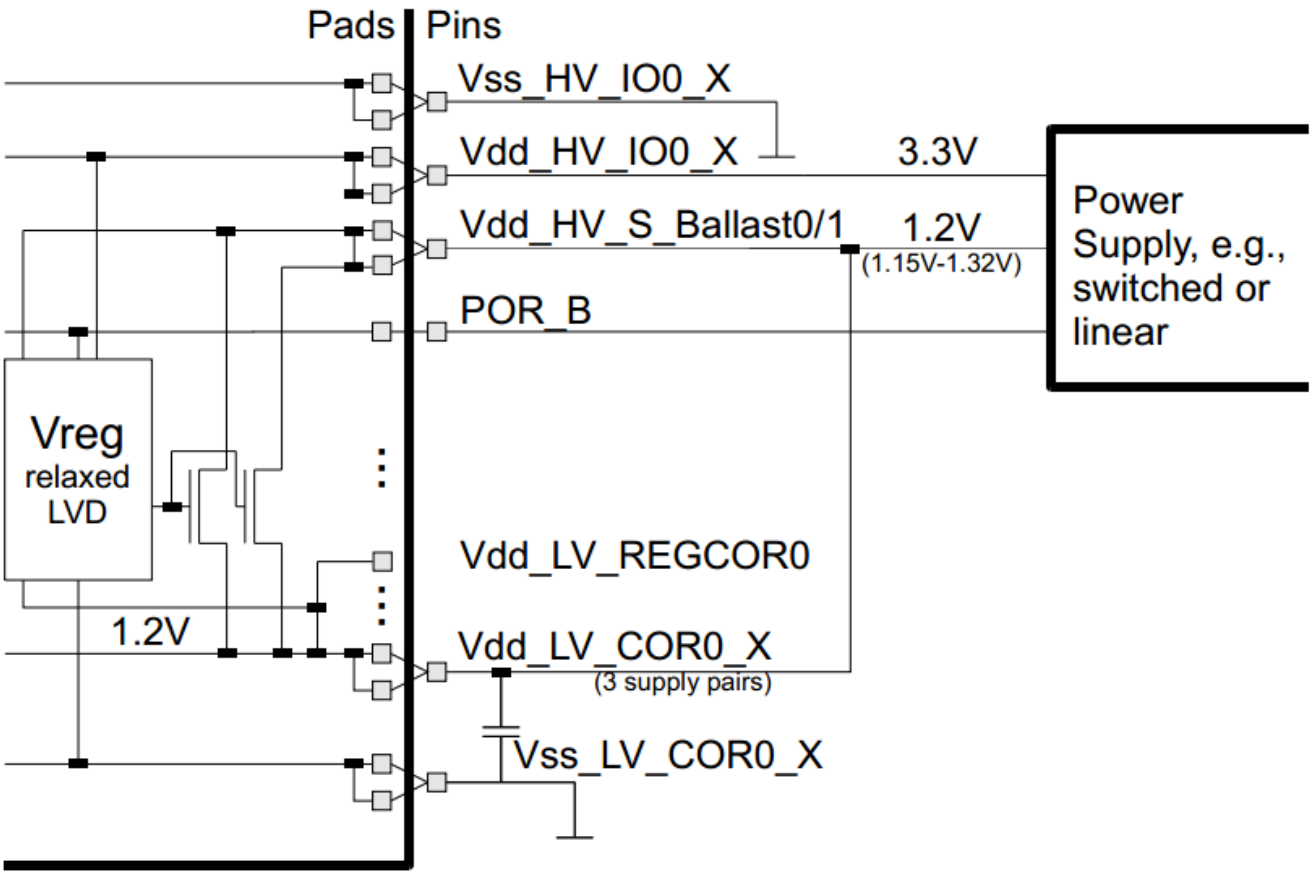


Figure 1. External Voltage Regulation mode

NOTE

POR_B is the power-on reset pin. If this pin is NOT controlled from outside, it must be tied to VDD_HV in Internal and External Voltage Regulation modes.

3.2 Internal Voltage Regulation mode

This is the core logic supply. In Internal Regulation mode, the core supply is derived from the main supply via an on-chip linear regulator driving the internal PMOS ballast transistors. The PMOS ballast transistors are located in the pad ring and their source connectors are directly bonded to a dedicated pin.

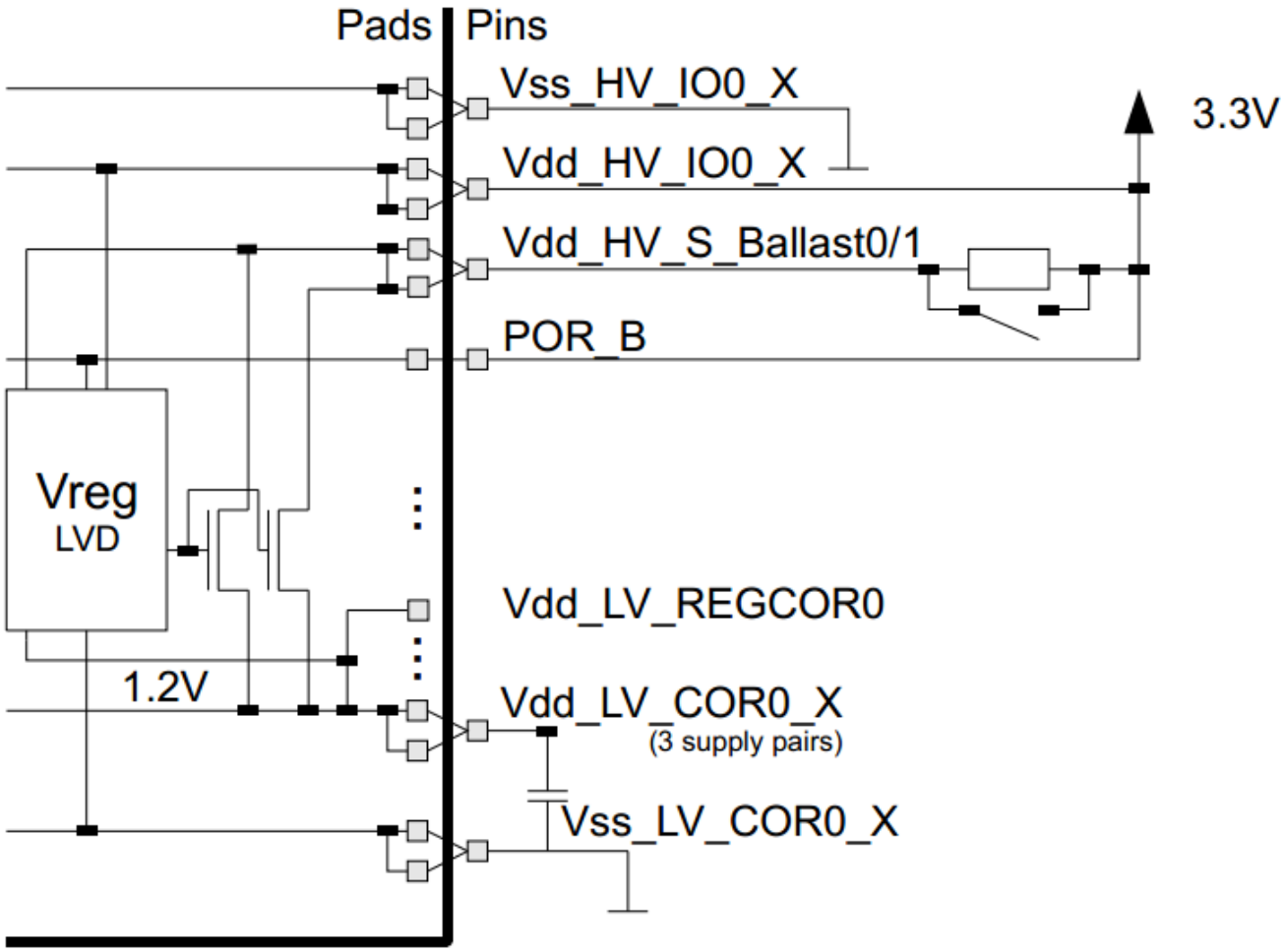


Figure 2. Internal Voltage Regulation mode

3.3 Decoupling capacitors

The ballast transistor requires capacitors to be added for decoupling and stability. Large capacitors are for regulator stability. The number of capacitors is not important—only the overall capacitance and the overall ESR value are important. Small capacitors are for power supply decoupling, although they do contribute to the overall capacitance values. They should be located close to the device pin.

- C_{DEC2} between each digital supply voltage pair V_{DD_HV}/V_{SS_HV}
- C_{REG} between each low-voltage digital supply pair V_{DD_LV}/V_{SS_LV}
- C_{DEC1} between each internal regulator supply voltage $V_{DD\_HV\_S\_BALLAST}$ and the nearest V_{SS_HV} (value depends on external regulator characteristics)
- 100 nF between ADC analog supply and analog ground (V_{DD_ADC}/V_{SS_ADC} pair)

NOTE

Required capacitor values listed in the table include a de-rating factor of 40%, covering tolerance, temperature, and aging effects. These factors are taken into account to assure proper operation under worst case conditions. X7R type materials are recommended for all capacitors, based on ESR characteristics.

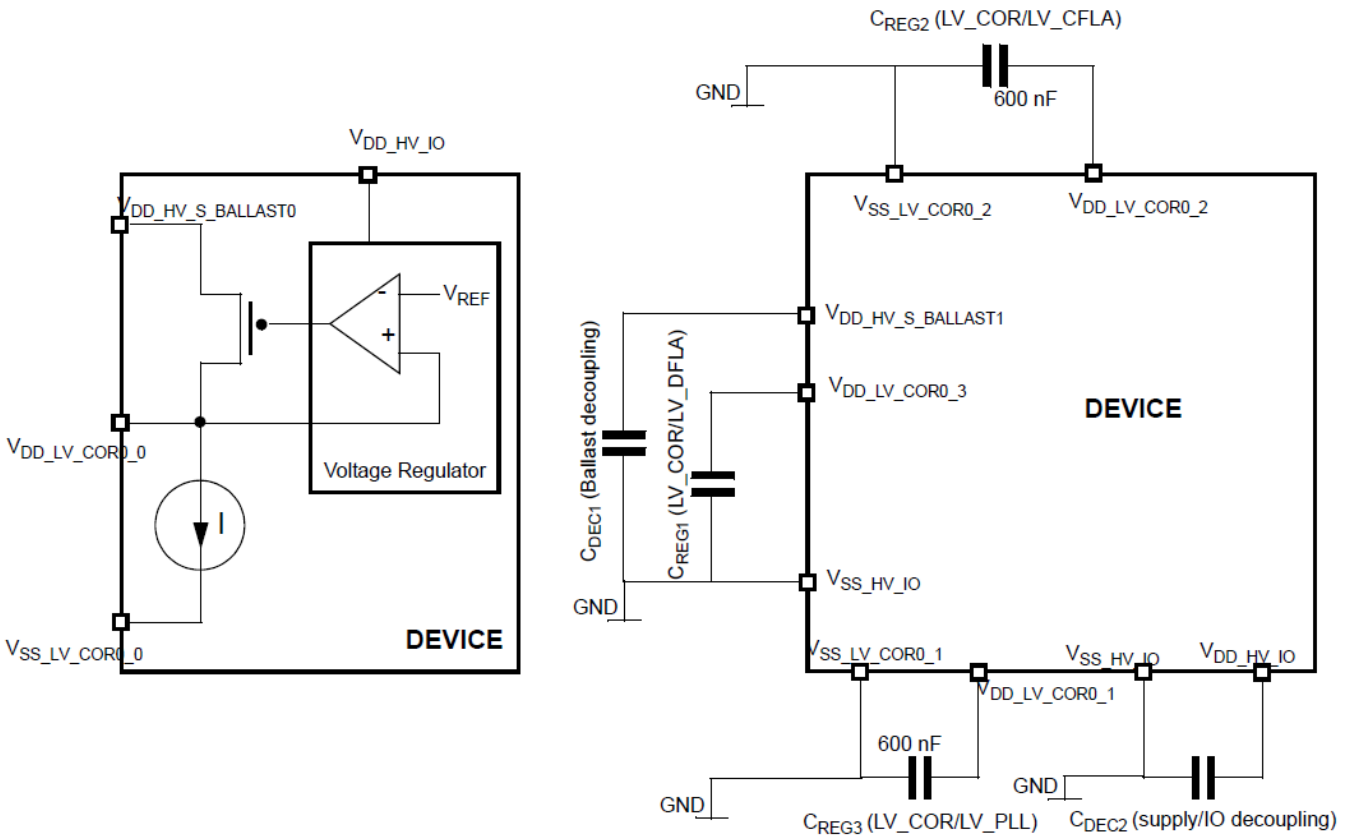


Figure 3. Voltage regulator capacitance connection

Table 3. Decoupling capacitors

Symbol	Parameter	Value			Unit
		Min	Typ	Max	
C^{REGn}	Internal voltage regulator external capacitance	200	—	600	nF
R^{REG}	Stability capacitor equivalent serial resistance	0.05	—	0.2	Ω
C_{DEC1}	Decoupling capacitance ballast	100[1]	470[2]	—	nF
		400			
C_{DEC2}	Decoupling capacitance regulator supply	100nF	1µF	—	—

1. This value is acceptable to guarantee operation from 3.0–3.6 V

2. External regulator and capacitance circuitry must be capable of providing I_{DD_BV} while maintaining supply V_{DD_BV} in the operating range.

3.4 Reset pin requirement

The /RESET pin is open-drain bidirectional (input and output) with Schitt trigger characteristics and a noise filter. Externally asserting the /RESET pin low resets the device. When reset happens internally or externally, the MCU drives the /RESET pin low internally until the reset sequence finishes.

CAUTION

Do not connect the /RESET pin to a strong high voltage level without a pullup resistor. A push-pull output driver is not allowed to switch the /RESET pin.

The /RESET pin has an internal weak pullup. If the open drain reset circuit and its relative switch need a capacitor in order to filter its input signal, an external pullup can speed up the charger of this capacitor.

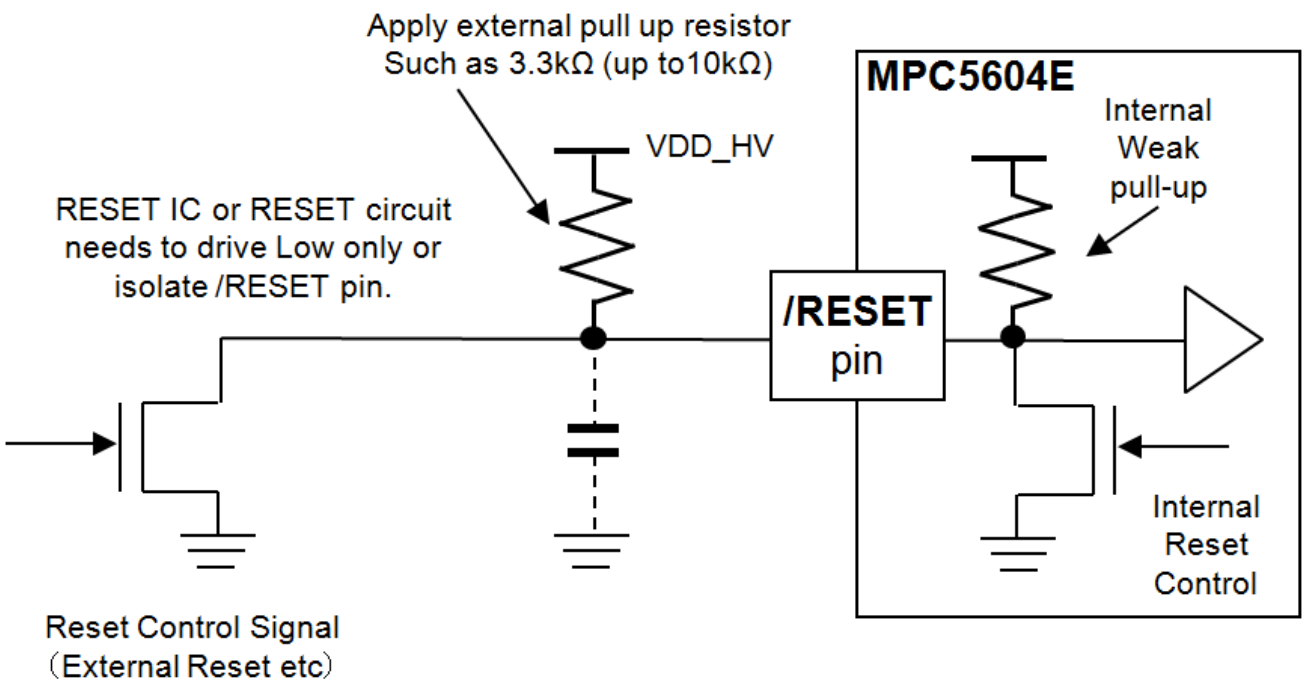


Figure 4. /RESET pin—recommended connection

Table 4. /RESET electrical characteristics

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
W_{FRST}	/RESET input filtered pulse	—	—	—	40	ns
W_{NFRST}	/RESET input not filtered pulse	—	500[1]	—	—	ns

Table continues on the next page...

Table 4. /RESET electrical characteristics (continued)

Symbol	Parameter	Condition	Value			Unit
			Min	Typ	Max	
$\|I_{WPU}\|$	Weak pullup current absolute value[2]	VDD = 3.3 V ± 10%	10	—	150	µA

1. /RESET pin must be externally asserted low at least 500 ns so that the MCU can recognize RESET assertion.
2. This indicates /RESET pin has an internal weak pullup.

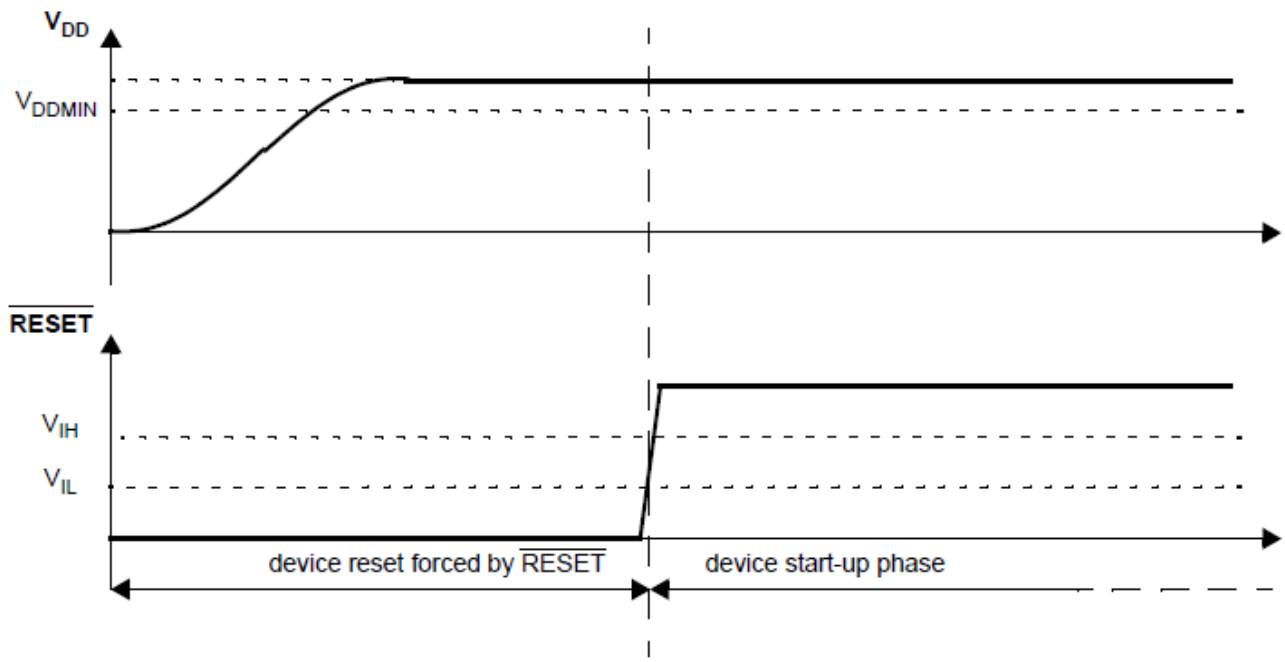


Figure 5. Startup reset requirements

NOTE

If the external reset circuit doesn't assert the /RESET pin after the device reset sequence finishes, the MCU releases the /RESET pin.

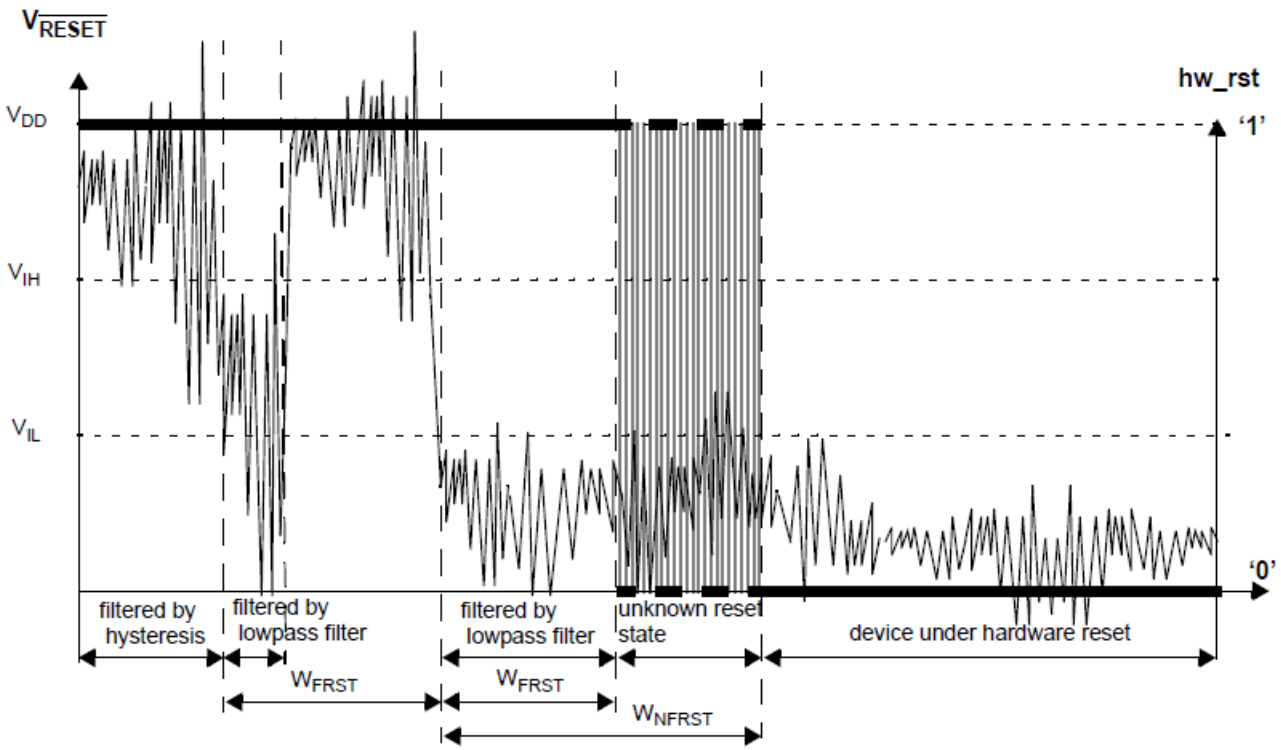


Figure 6. Noise filtering on reset signal

CAUTION

If the power-on reset pin (POR_B) is NOT controlled from outside, it must be tied to VDD_HV on internal and extenrnal voltage regulation modes.

4 Clock circuitry

The MPC5404E has three clock sources

- Internal RC oscillator (IRC)
- External oscillator clock (XOSC)
- 64 MHz PLL (FMPLL)

The IRC is internal and does not have to be considered from a hardware design perspective.

The XOSC works in a range from 4MHz to 40MHz. The crystal oscillator circuit includes an internal oscillator driver and external crystal circuity. It provides an output clock that can be provided to the PLL or used as a reference clock to specific modules depending on system requirements.

Referring to the schematic of the on-chip oscillator (Figure 7), the key items are described in the following section. The oscillator circuit provides a reference clock signal to the on-chip PLL. The oscillator circuit contains:

- A crystal
- Two capacitors

An external bias resistor (R1) is not required as there is an internal bias resistor within the recommended crystals. However, it is recommended that you leave space for one on the printed-circuit board to accommodate different crystal configurations in the future.

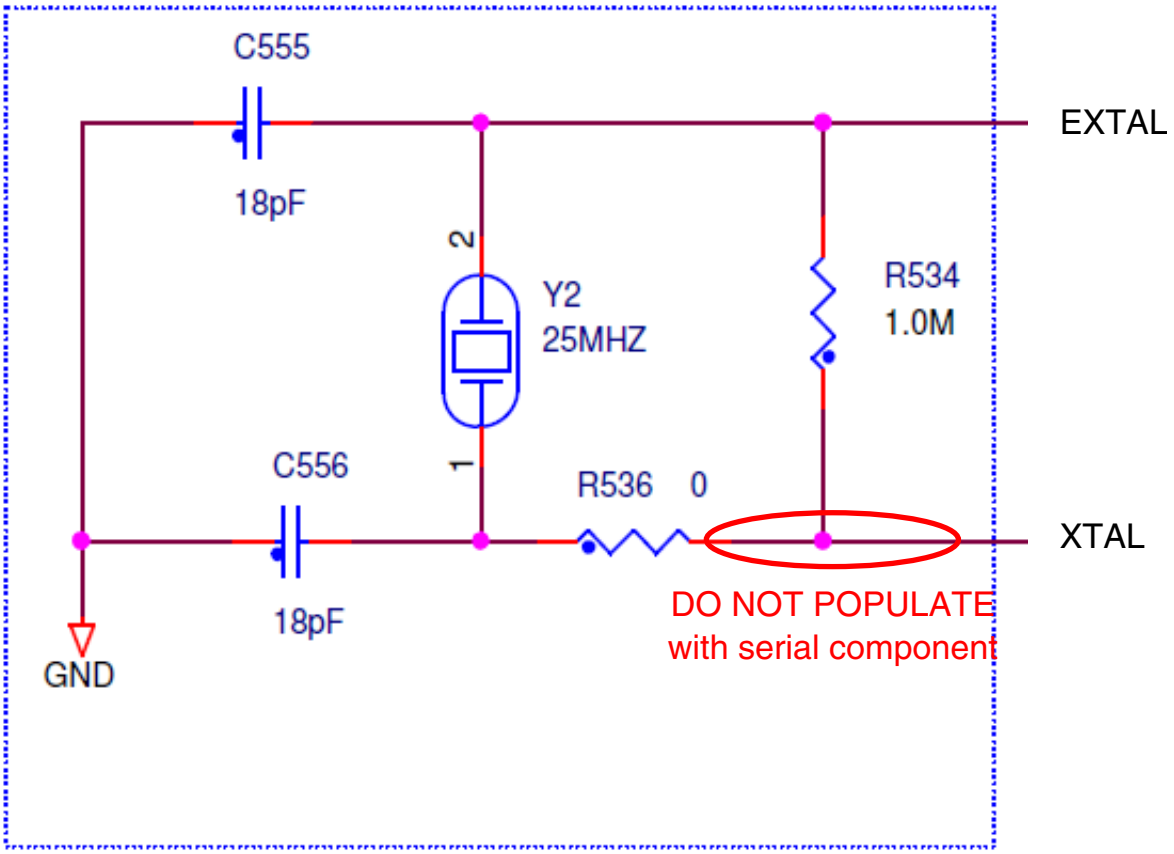


Figure 7. External crystal circuit

The load capacitors are dependent on the specifications of the crystal and on the board capacitance. It is recommended that you have the crystal manufacturer evaluate the crystal on the evaluation board/printed-circuit board.

4.1 Frequency Modulated PLL (FMPLL)

The FMPLL allows the generation of high-speed system clocks from a 4 MHz to 40 MHz input clock. Furthermore, the FMPLL supports programmable frequency modulation of the system clock. The PLL has the following major features:

- Input clock frequency from an 4 MHz to 40 MHz
- Voltage controlled oscillator (VCO) range from 256 MHz to 512 MHz
- Reduced frequency divider (RFD) for reduced frequency operation without forcing the PLL to re-lock
- Frequency modulated PLL
  - Modulation enabled/disabled through software
  - Triangle wave modulation
- Programmable modulation depth (±0.25% to ±2% deviation from center frequency)
  - Programmable modulation frequency dependent on reference frequency
- Self-clocked mode (SCM) operation
- Input supply is the same as the core supply: 1.2 V

The MPC56xx devices can use either the on-chip oscillator with an external crystal or an external reference clock as the reference clock to the device. This reference is qualified in multiple manners before the PLL will begin lock operation. The “pre” FMPLL circuitry consists of an automatic level-controlled amplifier, a comparator, a loss of clock detector, and a predivider.

5 Oscillator hardware recommendations

Use the lowest frequency crystal possible and set the multiplication factor bits to obtain the proper system operating frequency which is generated from the PLL. (Using lower crystal values and higher multiplication factors causes higher jitter on the PLL. There is a trade-off between jitter and oscillator current. Higher crystal values have higher operating currents) .

- The oscillator circuit has currents flowing at the crystal's fundamental frequency. Also, if the oscillator is clipped, then higher order harmonics will be present as well. In order to minimize the amount of emissions generated from these currents, the oscillator circuit should be kept as compact as possible.
- VSS _HV which is multiple bounded to VSS_HV_OSC0 internal signal should be connected directly to the ground plane so that return currents can flow easily between VSS _HV_OSC and the two capacitors (C1 and C2).
- EXTAL is the output of the oscillator.
- Do not install a series component (note: some crystal manufacturers may require a series resistor on the oscillator output either for reducing the driver current or for frequency limiting to reduce harmonic distortion from the oscillator circuit)
- Avoid other high frequency signals near the oscillator circuitry
- Shield the crystal with an additional ground plane underneath the crystal

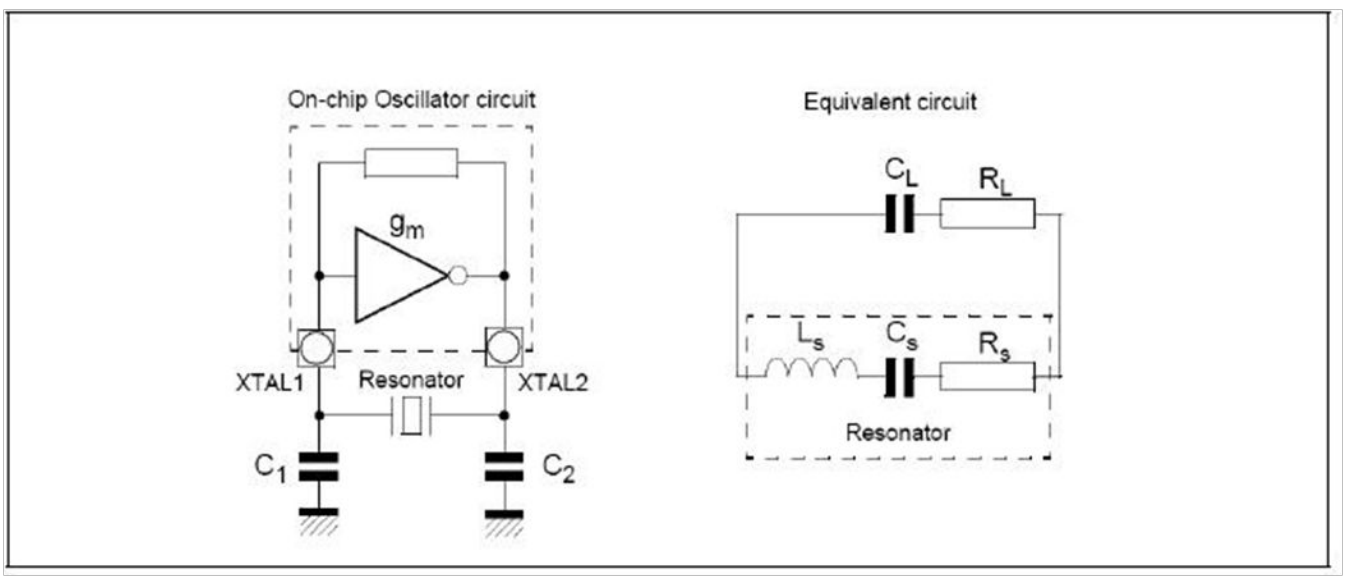


Figure 8. On-chip oscillator circuit

Table 5. Main oscillator electrical characteristics

Symbol		Parameter	Min	Max	Unit
f_{OSC}	SR	Oscillator frequency	4	40	MHz
g_m	P	Transconductance	4	15.846	mA/V
V_{OSC}	T	Oscillation amplitude on EXTAL pin	1.3	2.25	V
t_{OSCSU}	T	Start-up time[1, 2]		5	ms

1. The start-up time is dependent upon crystal characteristics, board leakage, etc., high ESR and excessive capacitive loads can cause long start-up time.
2. Value captured when amplitude reaches 90% of EXTAL

6 Boot configuration

The boot configuration pins select the device's boot operating mode. The following table shows the boot options.

Table 6. Reset boot configuration

FAB	ABS[0]	ABS[2]	Boot ID	Boot mode
1	0	0	—	Serial boot LinFle without autobaud
1	1	0	—	Serial boot FlexCA without autobaud
1	0	1	—	Serial boot via LinFlex or FlexCAN in autobaud
0	—	—	Valid	SC (Single chip)
0	—	—	Not valid	Safe mode

In Single-Chip Boot mode, the hardware searches the flash boot sector for a valid boot ID. As soon the device detects a bootable sector, it jumps within this sector and reads the 32-bit word at offset 0x4. This word is the address where the startup code is located (reset boot vector). Then the device executes this startup code. A user application should have a valid instruction at the reset boot vector address. If a valid RCHW is not found, the BAM code is executed. In this case, the BAM moves the MPC5604E into static mode.

Serial Boot mode allows the device to boot over either the LinFlex (SCI) (a simple, standard RS-232D type interface) or via the FlexCAN module. Both interfaces are monitored until activity is seen on one interface. Once an initial activity is seen on an interface, that interface becomes the boot interface. The boot protocol allows software to be downloaded into the device via the serial interface. Control will be passed to that software once loaded into memory. See the documentation for each device for additional information on the serial boot process.

CAUTION

I^2C0 peripheral share port pins C5 and C6 with reset boot configuration functions ABS[2] and FAB. It is reccomended that the logic circuit be used to achieve proper boot sequence and I^2C functionality.

7 Analog-to-Digital Converter (ADC)

The MPC5604E includes one 10-bit analog-to-digital converter (ADC) with the following features:

- Support for 4 external channels
- One internally connected channel for the the temperature sensor
- One internally connected channel for the internal 1.2 V rail
- One internally connected channel for the internal 3.3 V rail
- One internally connected channel for the VGate current

The ADC module has an independent supply and reference voltage that allows for an isolated analog voltage supply input pin VDD_HV_ADC, resulting in a low noise voltage source. The VDD_HV_ADC must be at the same voltage as the digital voltage supply VDD_HV, in addition to the VSS_HV_ADC analog ground for further supply isolation.

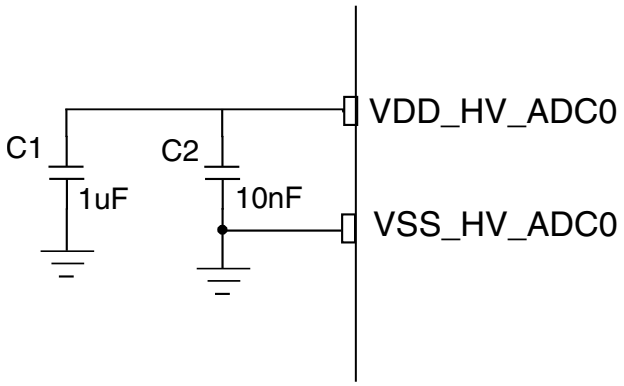
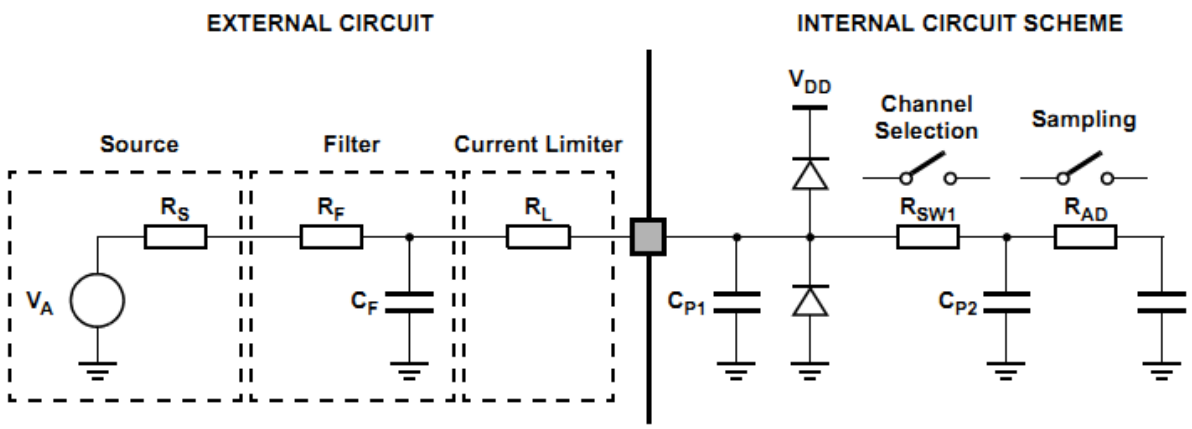


Figure 9. ADC voltage supply connection

Analog signals should not run parallel to clock or any noisy signals such as XTAL and EXTAl and should cross at right angles if necessary.

To preserve the accuracy of the ADC, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective; the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; further, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed with the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC in mind. For more information, refer to the ADC electrical characteristics in the *MPC5604E Microcontroller Data Sheet*.



R_S Source Impedance
R_F Filter Resistance
C_F Filter Capacitance
R_L Current Limiter Resistance
R_{SW1} Channel Selection Switch Impedance
R_{AD} Sampling Switch Impedance
C_P Pin Capacitance (two contributions, C_{P1} and C_{P2})
C_S Sampling Capacitance

Figure 10. Input equivalent circuit

8 Recommended debug connectors and connector pinout definitions

Table 7 shows the recommended connectors for different applications for the MPC55xx and MPC56xx.

Table 7. Recommended connectors

Connector style	Target system part number	Connector type
14-pin BERG JTAG only	3M 2514-6002UB	JTAG-only configuration
25-position (2 × 25, 50-pin) Samtec	Samtec ASP-148422-01	Full Nexus configuration
38-pin MICTOR	Tyco 767054-1[1]	Full Nexus configuration

1. Other compatible part numbers are 2-5767004-2 (RoHS compliant), 2-767004-2, 767061-1, and 767044-1.

NOTE

Whichever connector is chosen, "keep-out" areas may be required by some tools. Consult the preferred tool vendor to determine any area that must remain clear around the debug connector. Some tool vendors may include an extension cable to minimize "keep-out" areas, but using an extension will degrade the signal. In many cases, this degradation will be insignificant, but the amount of degradation depends on many factors, including clock frequency and target board layout.

8.1 MPC5500 and MPC5600 JTAG connector

The figure below shows the pinout of the recommended JTAG connector to support the MPC5500 and MPC5600 devices. If there is enough room allowed in the target system, a full Nexus connector is preferred over the simple 14-pin JTAG connector since it allows a higher degree of debug capability. It can be used as a minimum debug access or for BSDL board testing.

The recommended connector for the target system is the Tyco part number 2514-6002UB.

NOTE

This pinout is similar to the Freescale MCORE and DSP JTAG/OnCE connector definitions.

Table 8. Recommended JTAG connector pinout

Description	Pin	Pin	Description
TDI	1	2	GND
TDO	3	4	GND
TCK	5	6	GND
$\overline{\text{EVTI}}$[1]	7	8	—
$\overline{\text{RESET}}$	9	10	TMS
VREF	11	12	GND
$\overline{\text{RDY}}$[2]	13	14	JCOMP

1. $\overline{\text{EVTI}}$ is optional and was not included in the original (very early) definitions of the JTAG-only connector.
2. The $\overline{\text{RDY}}$ signal is not available on all packages or on all devices. Check the device pinout specification. In general it is not available in packages with 208 signals or less.

NOTE

Freescale recommends that a full Nexus connector be used for all tool debug connections, regardless of whether Nexus trace information is needed. Adapters for a JTAG class 1 14-pin connector (tool side) to the full Nexus MICTOR connectors (board side) are available from P&E Microcomputer Systems (http://www.pemicro.com), part number PE1906, and from Lauterbach (http://www.lauterbach.com), order number LA-3723 (CON-JTAG14-MICTOR). Lauterbach also has an adapter that will connect a MICTOR connector (tool side) to a 14-pin JTAG connector (board side). This adapter is order number LA-3725 (CON-MIC38-J14-5500).

8.2 MPC56xx high-speed parallel trace connector

For high-speed trace applications, the MICTOR-38 connector is not optimized for best signal integrity when using more than eight Message Data Out signals (MDO). Twelve MDO pins push the capability of the connector from a signal integrity standpoint. When moving to devices that support the full 16-bit MDO, a Samtec ERF8 series connector is highly recommended. The part number of the Samtec connector is shown in the following table.

Table 9. Recommended high-speed parallel trace connector part number

Connector	Part number (Samtec)	Style	Description
HP50	ASP-148422-01	Samtec ERF8 series, 25 position by 2 row	Vertical mount for MCU module

The Samtec ERF8 series of connectors is intended for high-speed applications requiring a minimal footprint with a reliable, latching connection. The recommended connector has two rows of twenty-five contacts each with a spacing of 0.8 mm. The connector provides isolation between the high-speed trace signals and the low-speed JTAG and control signals. It also provides ample ground connections to ensure signal integrity.

The following picture is courtesy of Samtec U.S.A (http://www.samtec.com/search/NEXUS.aspx).

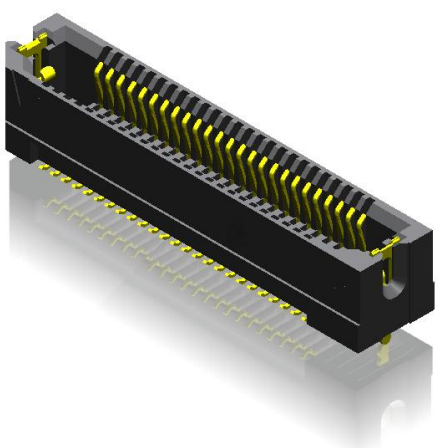


Figure 11. HP50 (ASP-148422-01) connector

Table 10 shows the recommended pinout for the Samtec connector.

Table 10. MPC56xx high-speed parallel trace connector

Position	Signal	Direction[1]	Pin number	Pin number	Direction[1]	Signal	IEEE-5001-2011 GEN_IO signal name
	GND [2]					GND[2]	
1	$\overline{\text{MSEO0}}$	Out	1	2	Out[3]	VREF	
2	$\overline{\text{MSEO1}}$	Out	3	4	In	TCK	
3	GND		5	6	In	TMS	
4	MDO0	Out	7	8	In	TDI	
5	MDO1	Out	9	10	Out	TDO	
6	GND		11	12	In	JCOMP	
7	MDO2	Out	13	14	Out	$\overline{\text{RDY}}$	
8	MDO3	Out	15	16	In	$\overline{\text{EVTI}}$	
9	GND		17	18	Out	$\overline{\text{EVTO}}$	
10	MCKO	Out	19	20	In	$\overline{\text{RESET}}$	
11	MDO4	Out	21	22	Out	$\overline{\text{RSTOUT}}$	GEN_IO0
12	GND		23	24		GND	
13	MDO5	Out	25	26	Out	CLKOUT	
14	MDO6	Out	27	28	In/Out	TD/WDT	GEN_IO1
15	GND		29	30		GND	
16	MDO7	Out	31	32	In/Out	DAI1	GEN_IO2
17	MDO8	Out	33	34	In/Out	DAI2	GEN_IO3
18	GND		35	36		GND	
19	MDO9	Out	37	38		ARBREQ	GEN_IO4
20	MDO10	Out	39	40		ARBGRT	GEN_IO5
21	GND		41	42		GND	
22	MDO11	Out	43	44	Out	MDO13	
23	MDO12	Out	45	46	Out	MDO14	
24	GND		47	48		GND	
25	MDO15	Out	49	50		N/C[4]	
	GND[2]					GND[2]	

1. Viewed from the MCU.
2. The connector locking mechanism provides additional ground connections on each end of the connector.
3. This is an output from the connector standpoint. It may or may not be from the MCU.
4. No connection — should be left open. Reserved for MDO16 on devices with more than sixteen MDO signals (future compatibility). In some applications this may be used as an SRAM voltage detect to determine when voltage for a standby SRAM is disconnected.

8.3 Minimum external circuitry

In general, other than the connector, no additional circuitry is required for the Nexus/JTAG debug circuitry. The MPC5500 and MPC5600 devices include internal pull devices that ensure the pins remain in a safe state; however, if there is additional circuitry connected to the Nexus/JTAG pins, or long traces that could be affected by other signals (due to crosstalk from high-current or high-speed signals), a minimum number of external pull resistors can be added to insure proper operation under all conditions.

Table 11. Optional minimum debug port external resistors

Nexus/JTAG signal	Resistor direction and value	Description
JCOMP	10 kΩ pulldown	Holds debug port in reset and prevents any debug commands from interfering with the normal operation of the MCU.
$\overline{\text{RESET}}$	4.7 kΩ pullup	The $\overline{\text{RESET}}$ input should be driven from an open collector output; therefore, it requires a pullup resistor for the MCU.
TD/WDT[1]	10 kΩ pulldown	With no tool attached, this signal should be held low and may or may not be connected to a pin of the MCU, depending on the system definition.
$\overline{\text{EVTI}}$	10 kΩ pullup	A pullup resistor prevents debug mode from being forced after reset if debug mode is enabled (JCOMP = high). It also prevents breakpoints from being forced if debug mode is enabled. **NOTE:** In almost all situations, a resistor is not required on this signal.

1. This is an optional signal and is not actually required for the MCU.

In addition to the pullup and pulldown resistors, some systems may want to use buffers between the Nexus/JTAG connector inputs and the MCU. This will prevent over-voltage conditions from causing damage to the MCU signals. Normal systems should not require this circuitry, but it is helpful in systems that can be exposed to improper connections that provide voltages that are outside the operating conditions of the MCU. A common circuit to use is the Texas Instruments SN74CBTLV3861[1]. This device is a bus switch that implements a bidirectional interface between two terminals with less than 5 Ω of resistance. It should be powered by the same supply that powers the debug port. The device enable should be connected to ground for the interface to be enabled whenever the debug port on the MCU is powered. This circuit provides a high impedance to the tool when the debug port is powered off.

NOTE

It is recommended that at least the reduced port configuration Nexus signals be made available (somewhere) on production boards. This facilitates debugging of new boards and analysis of errors in software, even on boards that have restricted space and normally provide a JTAG-only connection. If the Nexus signals are available on the production board, an adapter could be built to provide a Nexus connection on boards that do not have a complete footprint for one of the standard Nexus connectors. Likewise, the JTAG connector does not have to be populated on production boards and could even utilize a smaller connector footprint that could be used with an adapter to the standard debug connections.

1. SN74CBTLV3861-Q1 is automotive qualified if required.

9 Example communication peripheral connections

There are a wide range of peripheral pins available on the MCU. Many of these have fairly standard definitions for their use. This section provides example connections for some of the most commonly used communications peripherals, such as LIN, CAN, Ethernet, and RS-232 communication interfaces.

Table 12 summarizes the maximum communication speed and general overview information for the different types of interfaces.

Table 12. Communication module comparison

Common name	Standard	Distributed timebase	Speed (maximum supported)	Channels	Time triggered	Arbitration
RS-232D	EIA RS-232 revision D	No	115.2 kbit/s	Single	No	None (optional flow control)
LIN	LIN 1.0, LIN 2.0, and LIN 2.1[1]	No	100 kbit/s[2]	Single	No	None (master/ slave)
CAN	Bosch 2.0B ISO11898	No	1 Mbit/s[3]	Single	No (additional function)	CSMA (Carrier Sense Multiple Access)
Ethernet	IEEE 802.3	No[4]	100 Mbit/s	Single	No	CSMA/CD

1. Many Freescale devices only support the LIN 1.0 and 2.0 standards. LIN2.1 requires a different sampling scheme.
2. Typical speed is 10 or 20 Kbps, but supports a fast mode of 100 Kbps.
3. Two different speed classes are supported by CAN, a fast (250K to 1M bps) and a low speed CAN (5K to 125K bps).
4. Distributed timebase is not native by IEEE802.3 but there is hardware support for a PTP protocol that allows a distributed timebase to be used.

In a typical system, the battery reverse bias and over-voltage protection may be shared between all of the communication devices in the target system. Figure 12 shows a typical protection.

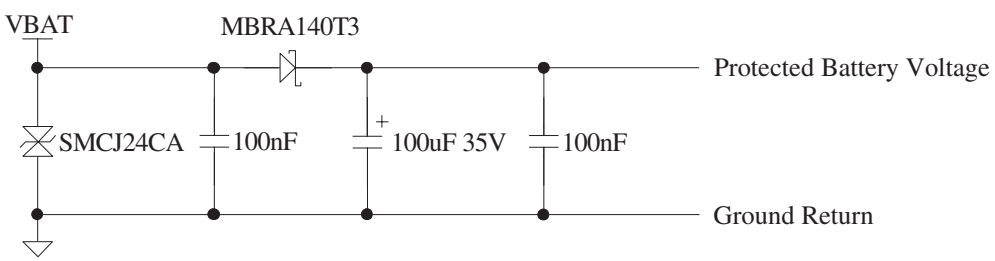


Figure 12. Typical protection circuit

9.1 Example LIN interface for LINFlex

Local Interconnect Network (LIN) is a commonly used low-speed network interface that consists of a master node communicating with multiple remote slave nodes. Only a single wire is required for communication and is commonly included in the vehicle wiring harness. Figure 13 shows a typical interface implemented using the Freescale MC33661 LIN transceiver.

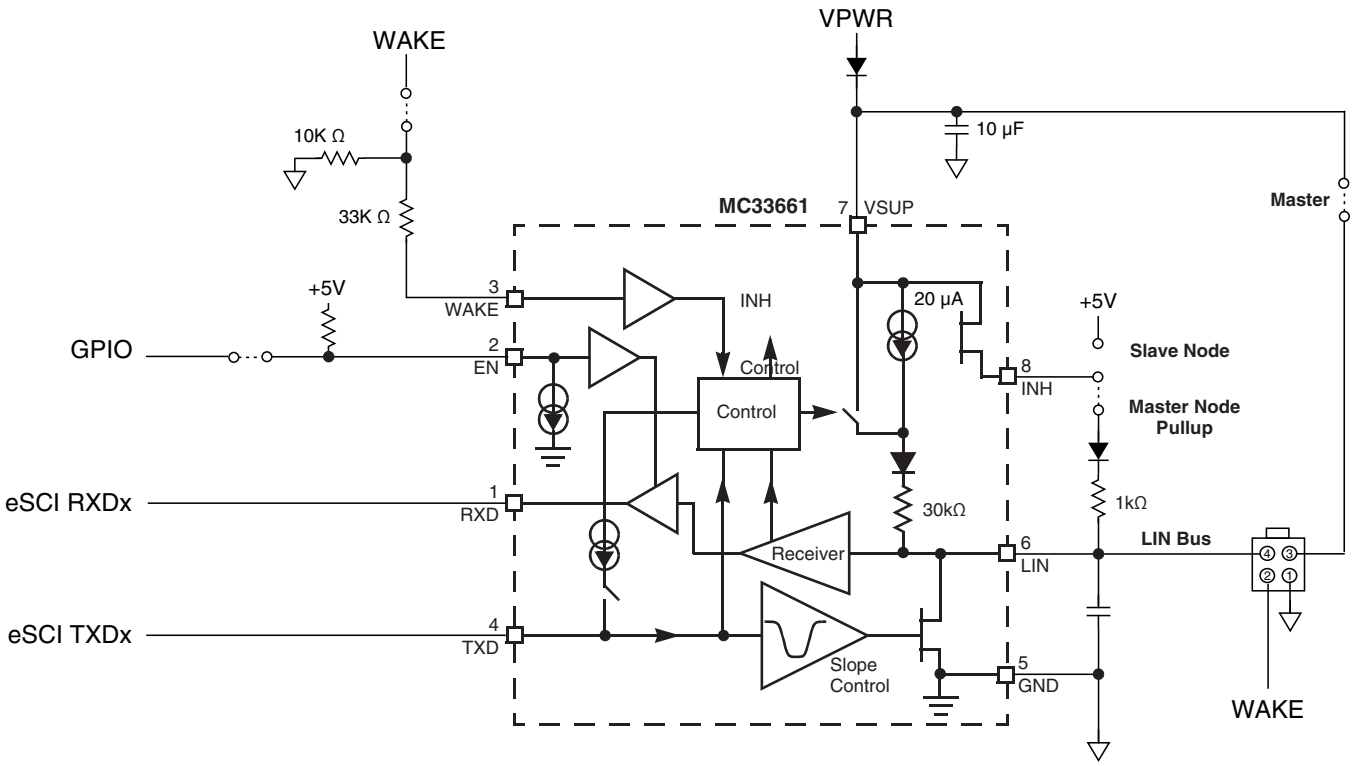


Figure 13. Typical LINFlex to LIN connections

Table 13 shows the pins of the MC33661 and their typical connections to an MCU.

Table 13. MC33661 pin definitions and example system connections

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
1	RXD	Output	Receive Data Output	MCU LIN RXD	LIN Receive Data Output to the MCU.
2	EN	Input	Enable Control	MCU GPIO	Enables operation of the device.
3	Wake	Input	Wake Input	LIN Bus Wake[1]	Wake enables the devices out of sleep mode.
4	TXD	Input	Transmit Data Input	MCU LIN TXD	LIN Transmit Data Input from the MCU.
5	GND	Input	Ground	System Ground Reference	Device ground reference.
6	LIN	Input/Output	LIN Bus	LIN Bus	Bidirectional pin that represents the single-wire transmit and receiver.

Table continues on the next page...

Table 13. MC33661 pin definitions and example system connections (continued)

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
7	VSUP	Input	Power Supply	Protected battery voltage	This is the power supply for the device and is typically connected to a nominal 12 V.
8	INH	Output	Inhibit Output	LIN Bus (if master)	The Inhibit pin controls either an external regulator to turn on a slave node or is connected through a resistor to the LIN bus on master nodes.

1. Wake is an optional signal on the LIN connector, but may come directly from a switch.

There no standard industry-defined LIN connector. Freescale uses a 4-pin Molex that allows for the the LIN bus pin, a power supply source (VPWR), a wakeup signal, and a ground reference. Slave nodes will often implement two connectors to allow the easy implementation of a daisy-chain of multiple nodes.

Table 14. LIN connector pinout recommendation

Function	Pin number	Pin number	Function
LIN Bus	4	3	VPWR
Wake	2	1	Ground

In a typical system, these pins would be used as follows:

- LIN Bus: This is the single-wire LIN bus that connects the master LIN node and the slave LIN nodes.
- VPWR: This connector input can be used as the power input to a slave node. Care should be taken that sufficient current is available for the total number of LIN slaves that are powered through this connection. In some systems, this may come from the master LIN node.
- Wake: The Wake signal is typically used for each individual slave node to enable the LIN physical interface of that node and consequently enable the power supply (using the INH output) to power up the MCU to perform some action. For example, when the handle on a car door is lifted, this signal would turn on the MCU that controls a function inside the vehicle, such as powering a smart dome light or enabling the controls of a smart seat.
- Ground: Ground reference for the module.

Part numbers for the 4-pin Molex Mini-Fit Jr.™ connector are shown in Table 15

Table 15. Recommended connector part numbers

Description	Manufacturer part number (Molex)
4-pin right-angle connector with flange for target system, tin contacts, with latch	39-29-1048
4-pin right-angle connector with pegs for target system, tin contacts, with latch	39-30-1040
4-pin vertical connector with pegs for target system, tin contacts, with latch	39-29-9042

Table continues on the next page...

Table 15. Recommended connector part numbers (continued)

Description	Manufacturer part number (Molex)
4-pin right-angle connector with flange for target system, gold contacts, latch	39-29-5043
Mating connector with latch for cable assemblies	39-01-2040
Female terminal for mating cable assembly	39-00-0077

9.2 Example RS-232 interface for LINFlex

The RS-232 (TIA/EIA-232-F) standard is a fairly common interface that was once available on nearly all computers. While this interface is disappearing, adapters are available to allow the use of RS-232 peripherals through other interfaces, such as USB. RS-232 was intended to be a very low-cost, low-performance interface. This interface was originally specified with signal voltages of +12 V and –12 V typically. However, this has been lowered to a typical minimum voltage of +5 V and –5 V in recent years.

Figure 14 shows the typical connections between the serial port of an MCU and the MAX3232-EP RS-232D transceiver from Texas Instruments (http://www.ti.com/). The transceiver operates from either a 3.3-V or a 5-V supply and includes two charge pumps to generate the required output voltages. This device contains two transmit drivers and two receivers. The charge pumps require four external capacitors.

NOTE

The commercial grade MAX3232 device is not rated for the full automotive temperature of -40 to +125° C and is not intended for automotive applications. This circuit should not be used or populated in a production module intended for automotive use. However, in many cases, the RS-232 interface is intended only as a development interface; therefore, the commercial device can be used for prototyping purposes. TI does offer a device option with an operating temperature range of –40 to +85° C. TI has an enhanced version of the device, MAX3232-EP, that is intended for aerospace, medical, and defense applications. This version is available with an operating temperature range of –55 to +125° C.

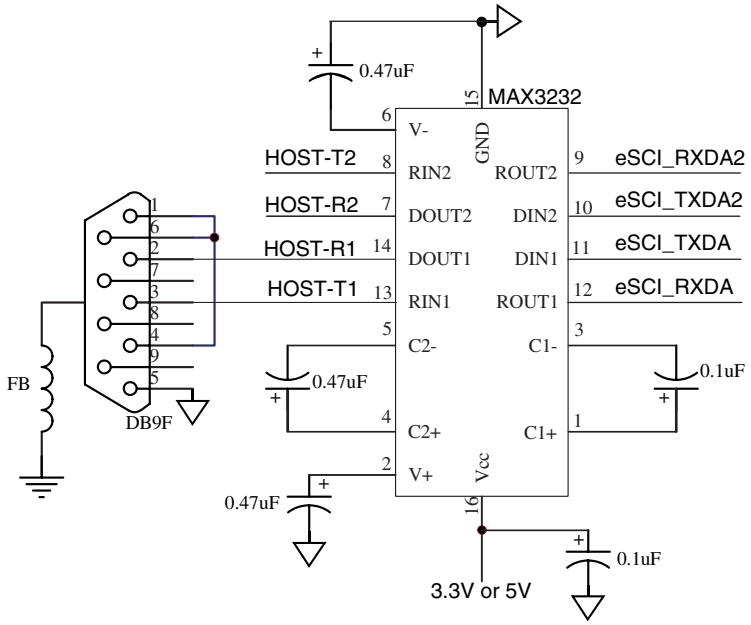


Figure 14. Typical LINFlex to RS-232D circuit

Table 16. Typical RS-232D connector definition

6 Connect to pin 1 and 4	**1** Connect to pin 4 and 6
7 N/C	**2** RS-232 TX (transmit)
8 N/C	**3** RS-232 RX (receive)
9 N/C	**4** Connect to pin 1 and 6
	5 GND

NOTE

N/C pins are not connected.

The connector's shell should be connected through a ferrite bead to ground.

9.3 CAN interface circuitry

A Controller Area Network (CAN) is commonly used in almost all automotive applications to allow communication between various microchips in the car.

The number of CAN modules on-chip vary from device to device. A separate CAN transceiver is required for each CAN module, although some CAN transceivers may have more than one on a single chip.

Freescale CAN modules conform to CAN protocol specification version 2.0B, and the transceivers shown in this application note comply with the ISO11898 physical layer standard.

Typically, CAN is used at either a low speed (5 kbit/s to 125 kbit/s) or a high speed (250 kbit/s to 1 Mbit/s). Powertrain applications typically use a high speed (HS) CAN interface to communicate between the engine control unit and the transmission control unit. Body and chassis applications typically use a low speed (LS) CAN interface. In the dashboard of a vehicle, there is typically a gateway device that interfaces between HS and LS CAN networks.

Freescale has a high-speed standalone CAN physical interface device, as well as CAN transceivers integrated with other functions[2]. Other popular CAN transceivers include the NXP devices in Table 17 below. Example TJA1050 HS and TJA1054 LS circuits are shown in this application note.

Table 17. NXP CAN transceiver comparison

	TJA1050	TJA1054	TJA1040	TJA1041
Bit rate (kbit/s)	1000	125	1000	1000
Modes of operation	Normal, Listen only	Normal, Standby, Sleep	Normal, Standby	Normal, Listen only, Standby, Sleep

9.3.1 High-speed CAN TJA1050 interface

Figure 15 shows the typical connections for the physical interface between the MCU and the CAN bus for HS applications using the NXP TJA1050 HS CAN transceiver.

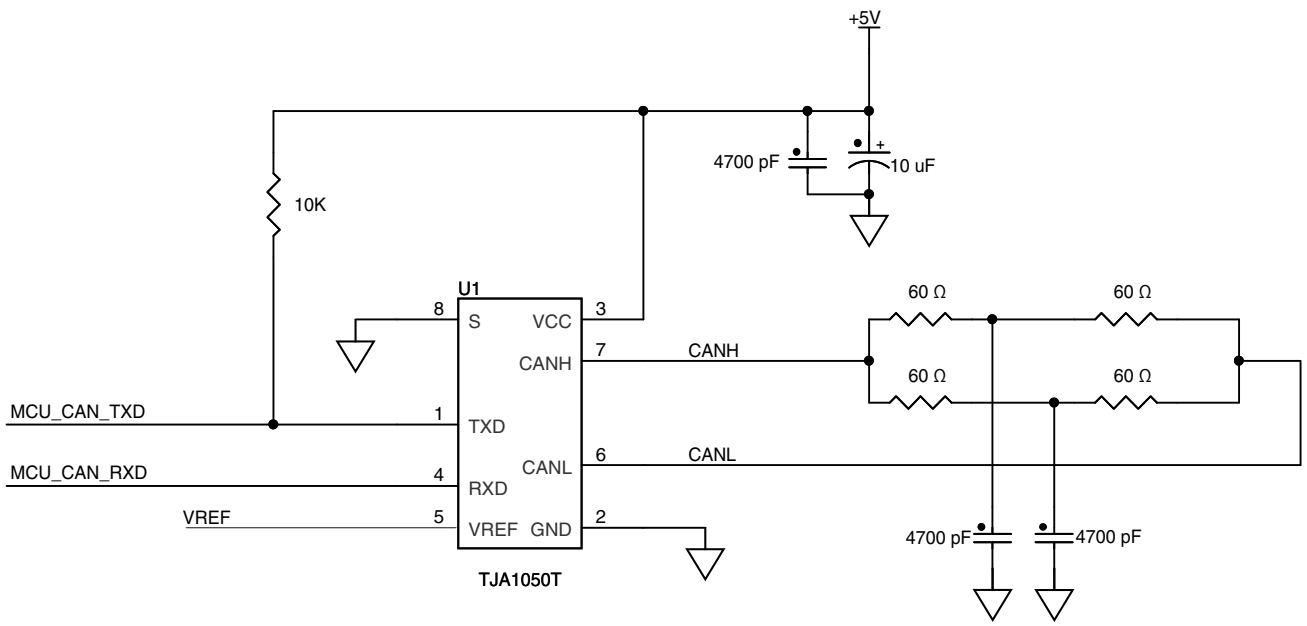


Figure 15. Typical high-speed CAN circuit using TJA1050

NOTE

Decoupling shown as an example only.

2. An example device is the MC33905 that includes a 5 V power supply controller, a CAN transceiver physical interface, and a LIN transceiver physical interface.

TXD/RXD pullup/pulldown may be required, depending on device implementation.

Table 18. TJA1050 pin definitions and example system connections

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
1	TXD	Input	Transmit Data	MCU CAN TXD	CAN transmit data input from the MCU.
2	GND	Output	Ground	Ground	Ground return termination.
3	VCC	Input		5 V	Voltage supply input (5 V).
4	RXD	Output	Receive Data	MCU CAN RXD	CAN receive data output to the MCU.
5	VREF	Output	Reference voltage Output	Not used	Mid-supply output voltage. This is typically not used in many systems, but can be used if voltage translation needs to be done between the CAN transceiver and the MCU.
6	CANL	Input/ Output	CAN Bus Low	CAN Bus Connector	CAN bus low pin.
7	CANH	Input/ Output	CAN Bus High	CAN Bus Connector	CAN bus high pin.
8	S	Input	Select	Grounded or MCU GPIO	Select for high-speed mode or silent mode. Silent mode disables the transmitter, but keeps the rest of the device active. This may be used in the case of an error condition.

9.3.2 Low-speed CAN TJA1054 interface

Figure 16 shows the typical connections for the physical interface between the MCU and the CAN bus for LS applications using the NXP TJA1054 LS CAN transceiver. Optionally, the standby and enable pins can be connected to MCU GPIO pins for additional control of the physical interface.

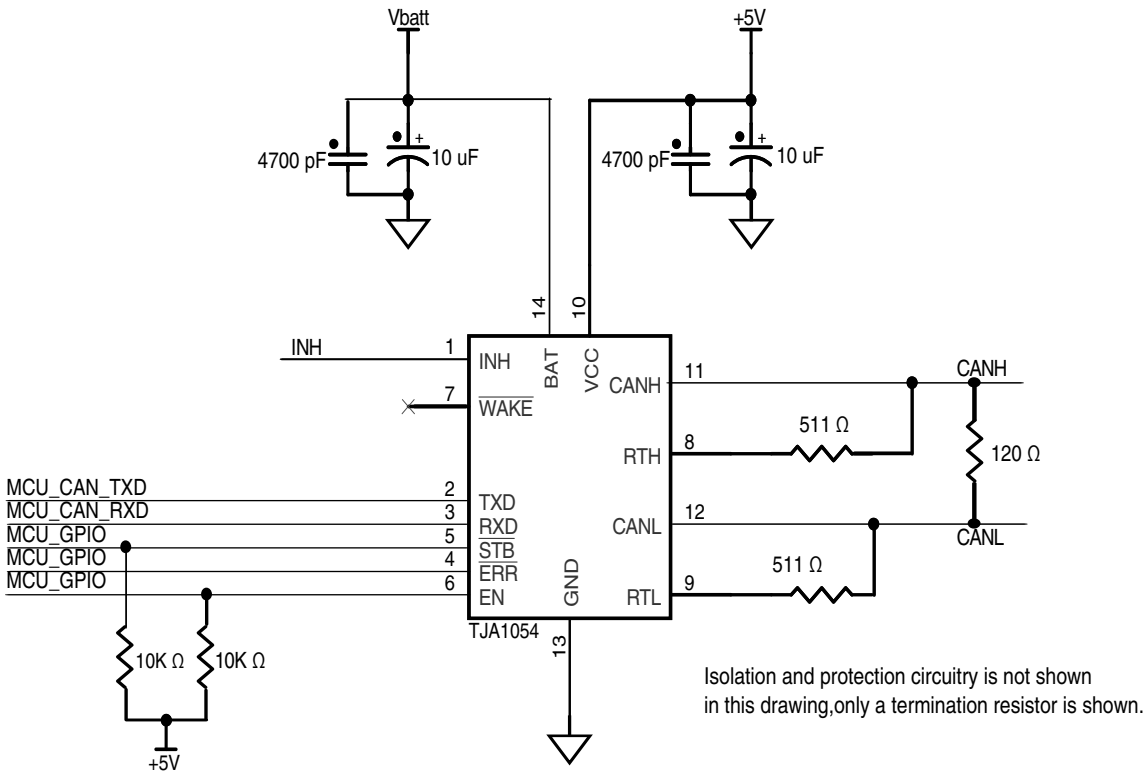


Figure 16. Typical low-speed CAN circuit using TJA1054

NOTE

Decoupling shown as an example only.

$\overline{\text{STB}}$ and EN should be pulled high for Normal mode. These signals can optionally be connected to MCU GPIO pins to allow MCU control of the the physical interface.

Table 19. TJA1054 pin definitions and example system connections

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
1	INH	Input	Inhibit	Typically not connected	Inhibit output for control of an external power supply regulator if a wake up occurs.
2	TXD	Input	Transmit Data	MCU CAN TXD	CAN transmit data input from the MCU.
3	RXD	Output	Receive Data	MCU CAN RXD	CAN receive data output to the MCU.
4	$\overline{\text{ERR}}$	Output	Error	MCU GPIO	The error signal indicates a bus failure in normal operating mode or a wake up is detected in standby or sleep modes.
5	$\overline{\text{STB}}$	Input	Voltage Supply for IO	MCU GPIO	Standby input for device. It is also used in conjunction with the EN pin to determine the mode of the transceiver.

Table continues on the next page...

Table 19. TJA1054 pin definitions and example system connections (continued)

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
6	EN	Input	Enable	MCU GPIO	Enable input for the device. It is also used in conjunction with the STB pin to determine the mode of the transceiver.
7	$\overline{\text{WAKE}}$	Input	Wake	Typically not connected	Wake input (active low), both falling and rising edges are detected.
8	RTH	Input	Termination Resistor High	Resistor to CANH	Termination resistor for the CAN bus high[1]
9	RTL	Input	Termination Resistor Low	Resistor to CANL	Termination resistor for the CAN bus low[1]
10	VCC	Input	Voltage Supply	5 volts	Digital IO supply voltage, 5 volts.
11	CANH	Output	CAN Bus High	CAN Bus Connector	CAN bus high pin.
12	CANL	Input/ Output	CAN Bus Low	CAN Bus Connector	CAN bus low pin.
13	Ground	Output	Ground	Ground	Ground return termination path.
14	BAT	Input	Standby	Battery voltage	Battery supply pin, nominally 12 V.

1. This allows the transceiver to control the CAN bus impedance under an error condition.

9.3.3 Recommended CAN connector

Generally, DB9 connectors are used for evaluation boards to connect CAN modules together, whereas there are various connectors used for production hardware. Figure 17 and Table 20 show a typical example of the connector pinout. A male type connector is used on the evaluation board and a female type cable connects with it.

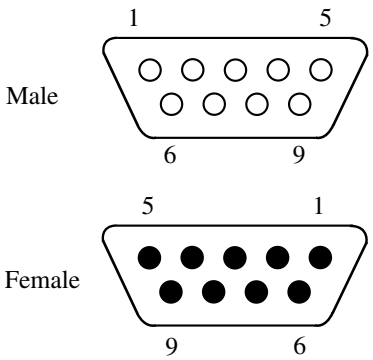


Figure 17. DB9 Connector Types

Table 20. DB9 connector mapping

Pin number	Signal name
1	N/C
2	CAN_L
3	GND
4	N/C
5	CAN_SHIELD (OPTIONAL)
6	GND
7	CAN_H
8	N/C
9	CAN_V+ (OPTIONAL)

NOTE

The metal shell of the connector should be connected through a ferrite bead to the chassis ground.

9.4 Fast Ethernet interface

The Fast Ethernet interface provides a standardized media independent interface (MII) that allows the connection of different Ethernet physical interfaces.

Ethernet is a commonly used high-speed network interface that supports both 10- and 100-Mbit/s Ethernet/IEEE 802.3 networks. An external transceiver interface and tranceiver function are required to complete the interface to the media.

The MPC5604E Ethernet interface supports three 10- and 100-Mbit/s IEEE Std. 802.3TM MII Ethernet physical interfaces. MII signals use CMOS signal levels compatible with devices operating at either 5.0 V or 3.3 V. Signals are not TTL compatible. They follow the CMOS electrical characteristics.

NOTE

The MPC5604E Ethernet interface uses the Ethernet AVB standard (IEEE 1722 Audio/ Video bridging) with hardware-supported Ethernet frame timestamping (IEEE 802.1as), which is required for the solution of the deterministic streaming service by precision time protocol (IEEE 1588).

The receiver functions correctly up to a RX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the system clock frequency must exceed four times the RX_CLK frequency.

Table 21. MII receive signal timing

No.	Parameter	Min	Max	Unit
1	Rx Clock Period	40	—	ns
2	RXD[3:0], RX_DV, RX_ER to RX_CLK setup	5	—	ns
3	RX_CLK to RXD[3:0], RX_DV, RX_ER hold	5	—	ns
4	Rx Clock Duty Cycle	40	60	%

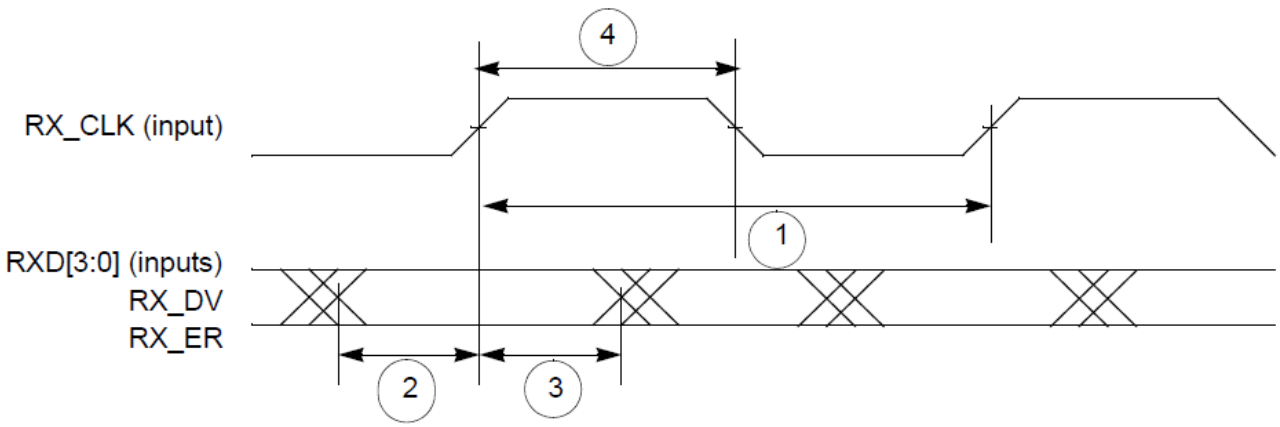


Figure 18. MII receive signal timing diagram

The transmitter functions correctly up to a TX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the system clock frequency must exceed four times the TX_CLK frequency. The transmit outputs (TXD[3:0], TX_EN, TX_ER) can be programmed to transition from either the rising or falling edge of TX_CLK; the timing is the same in either case. This options allows the use of non-compliant MII PHYs.

Table 22. MII transmit signal timing

No.[1]	Parameter	Min	Max	Unit
5	TX Clock Period	40	—	ns
6	TX_CLK to TXD[3:0], TX_EN, TX_ER invalid	5	—	ns
7	TX_CLK to TXD[3:0], TX_EN, TX_ER valid	—	25	ns
8	TX Clock Duty Cycle	40	60	%

1. Output pads configured with SRC = 0b11.

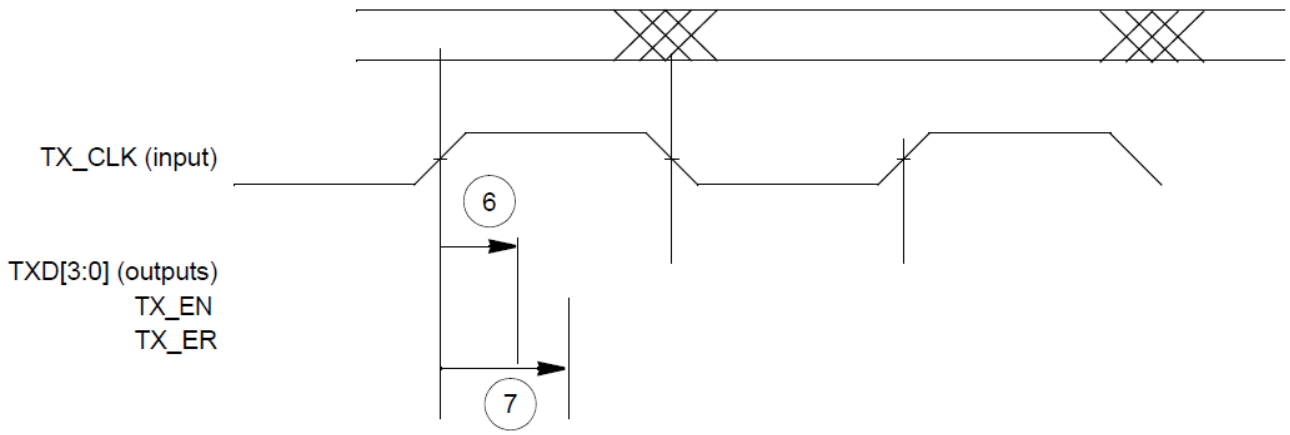


Figure 19. MII transmit signal timing diagram

Figure 20 shows the typical connections between the MII port of the MCU and the DP83848C Phyter® single-port 10/100 Mbit/s Ethernet physical layer transceiver from National Semiconductor (http://www.national.com/). The transceiver operates at a 3.3-V supply and support IEEE 802.3 MII.

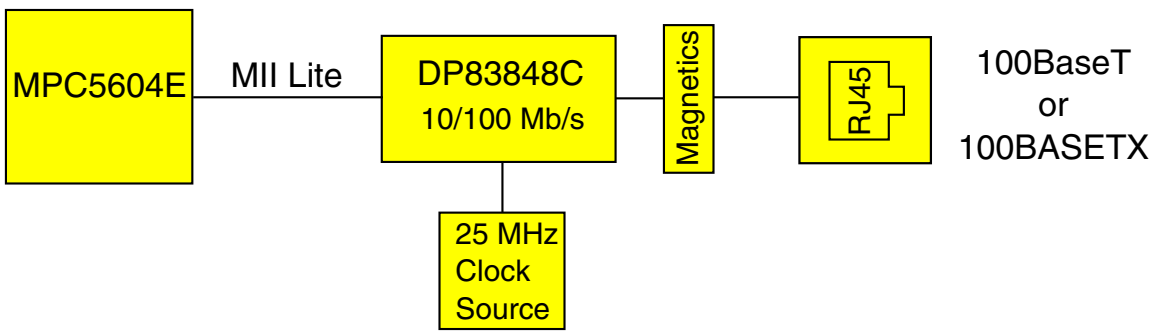


Figure 20. Typical FEC MII circuit using DP83848C

10 Pin Overview

Since there are many different requirements for the input and output signals of the MCU, several pin types are used. Table 23 summarizes the types of pins/pads available on the MCU. Information on the pad types and signal multiplexing is available in the *MPC5604E Microcontroller Reference Manual* and *MPC5604E Microcontroller Data Sheet*. This section helps interpret this information.

NOTE

This document uses the terms pins, balls, and pads interchangeably when referencing the external signals of the device.

Table 23. Pad types

Pad type	Abbreviation	Description
Slow Speed pads	Slow	Most of the peripheral signals are slow (or medium if available depending on the device definition) speed pads. The Slow speed pads have slew rate control and may implement digital input circuitry, digital output circuitry, or both.
Medium Speed pads	Medium	Most of the peripheral signals are medium (or medium if available depending on the device definition) speed pads. The Medium speed pads have slew rate control and may implement digital input circuitry, digital output circuitry, or both.
Fast pads	Fast	The fast pads are digital pads that allow high speed signals. Generally, these are used for the external bus interface.

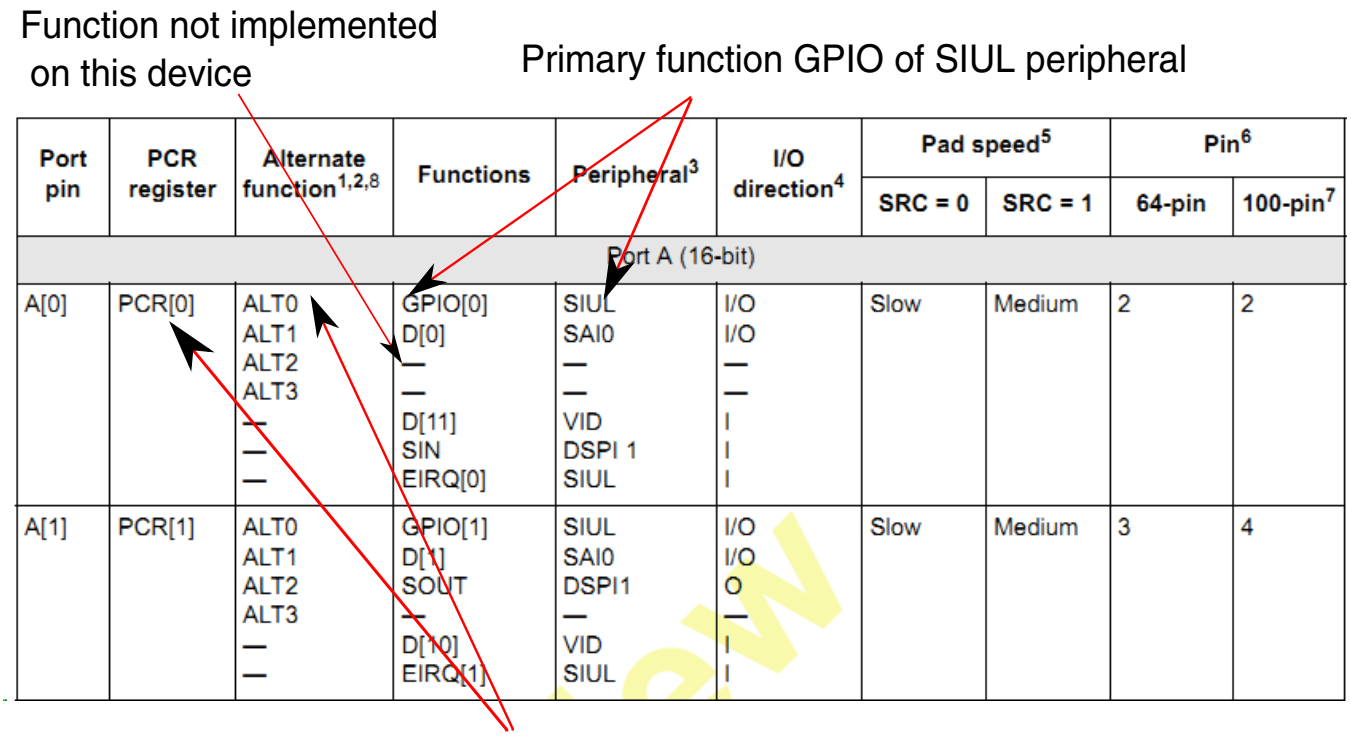
Each of these pad types have programmable features that are controlled in a pin or pad configuration register (PCR). All pins on the device, except single purpose pins without special properties that need to be controlled, have a PCR. In a few cases, some signals are grouped together and a PCR controls multiple pins. The PCR is identified by the GPIO number. The PCR controls the pin function, direction, and other capabilities of the pin.

10.1 Understanding pin multiplexing

Each pin (or pad[3]) of the MCU can be used for multiple functions. Software can select which function is available on the ball. The figure below shows a typical excerpt from the *MPC5604E Microcontroller Data Sheet* for the pin multiplexing of different functions. This table shows the different functions that are available on each pin.

Other information is also shown in this table that is important when designing a board. These other fields are shown in the following table.

3. Pins are used on packages that have pins for the signals. Pad refers to the bonding pad on the physical die that is contained inside the package. These terms are typically used interchangeably.



Port pin	PCR register	Alternate function[1,2,8]	Functions	Peripheral[3]	I/O direction[4]	Pad speed[5]		Pin[6]	
						SRC = 0	SRC = 1	64-pin	100-pin[7]
Port A (16-bit)									
A[0]	PCR[0]	ALT0 ALT1 ALT2 ALT3 — — —	GPIO[0] D[0] — — D[11] SIN EIRQ[0]	SIUL SAI0 — — VID DSPI 1 SIUL	I/O I/O — — I I I	Slow	Medium	2	2
A[1]	PCR[1]	ALT0 ALT1 ALT2 ALT3 — —	GPIO[1] D[1] SOUT — D[10] EIRQ[1]	SIUL SAI0 DSPI1 — VID SIUL	I/O I/O O — I I	Slow	Medium	3	4

- **Pad Speed**: These columns show available pad speed which is available for this pin. This speed is controlled by slew rate control bits in the PCRs of the SIUL module.
- **PIN:** These columns show the pin map location of the signal.

10.1.1 Pad slew rate

The slow-, medium-, and high-speed pads implement a slew rate control (SRC) selection in the Pad Configuration Register (PCR). Slew rate is used to slow down the time it takes for the signal to switch from a low to a high or from a high to a low.

Table 24 shows the different available slew rate settings.

Table 24. Slew rate settings

Pad type	Load drive (pF)	Frequency of Operation (MHz) (max)	Slope at rising/falling edge (ns) (min/max)
Slow Speed Pad	25	4	4/40
	50	2	6/50
	100	2	10/75
	200	2	14/100
Medium Speed Pad	25	40	2/12
	50	20	4/25
	100	13	8/40
	200	7	14/70

Table continues on the next page...

Table 24. Slew rate settings (continued)

Pad type	Load drive (pF)	Frequency of Operation (MHz) (max)	Slope at rising/falling edge (ns) (min/max)
Fast Speed Pad	25	72	1/4
	50	55	1.5/7
	100	40	3/12
	200	25	5/18

10.2 Injection current

All pins implement protection diodes that protect against electrostatic discharge (ESD). In many cases, both digital and analog pins need to be connected to voltages that are higher than the operating voltage of the device pin. In addition to providing protection from ESD, these diode structures will also clamp the voltage to a diode drop above the supply of that pin segment. This is permissible, as long as the current injection is limited as defined in the device specification. Current can be limited by adding a series resistor on the signal. The input protection diodes will keep the voltage at the pin to a safe level (per the absolute maximum ratings of the device) as long as it is less than the maximum injection current specification.

Additional circuits on the pins can be enabled only by fast ESD transients. In normal operation, these circuits have no effect on the pin characteristics and are triggered by fast high-voltage transients. To prevent turning on these circuits during normal power-up sequences, the ramp rate of the power supplies (all external supplies, 5 V, and if the internal regulators are not used, 3.3 V and 1.2 V) should not exceed 25 V/ms.

For absolute maximum ratings, refer to the current revision of the *MPC5604E Data Sheet* on www.freescale.com.

10.3 Handling unused pins

In some applications, not all pins of the device may be needed. Good CMOS handling practices state that all unused pins should be tied off and not left floating. On the MCU, unused digital pins can be left open in the target system. Almost all pins have internal pull devices (either pullup or pulldown devices[4]). For unused digital pins, it is recommended that software disable both the input buffers and the output buffers of the pads in the Pad Control Register for the ball. In addition, the weak pulldown device should be enabled. This keeps the pad in a safe state under all conditions.

For analog pins, it is recommended that they be pulled down to VSSA (the analog return path to the MCU).

4. Technically, these devices are not resistors. They are active weak transistors that pull the input either up or down.

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