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QorIQ T2080 Design Checklist

Also supports the T2081

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1 About this document

This document provides recommendations for new designs based on the T2080, which is an advanced, multicore processor that combines 4 dual-threaded e6500 processor cores built on Power Architecture®, with high-performance datapath acceleration logic and network and peripheral bus interfaces required for networking, telecom/datacom, wireless infrastructure, and mil/aerospace applications.

This document can also be used to debug newly-designed systems by highlighting those aspects of a design that merit special attention during initial system start-up.

NOTE

This document is also applicable to the T2081. For a list of functionality differences, see Appendix T2081 in the *T2080 Integrated Multicore Communications Processor Family Reference Manual* (T2080RM).

2 Before you begin

Ensure you are familiar with the following NXP collateral before proceeding:

- *T2080 QorIQ Integrated Multicore Data Sheet* (T2080)/ *T2081 QorIQ Integrated Multicore Data Sheet* (T2081)
- *QorIQ Integrated Multicore Communications Processor Family Reference Manual* (T2080RM)
- *T2080 and T2081 Chip Errata* (T2080CE)

3 Simplifying the first phase of design

Before designing a system with the chip, it is recommended that the designer be familiar with the available documentation, software, models, and tools.

This figure shows the major functional units of the T2080.

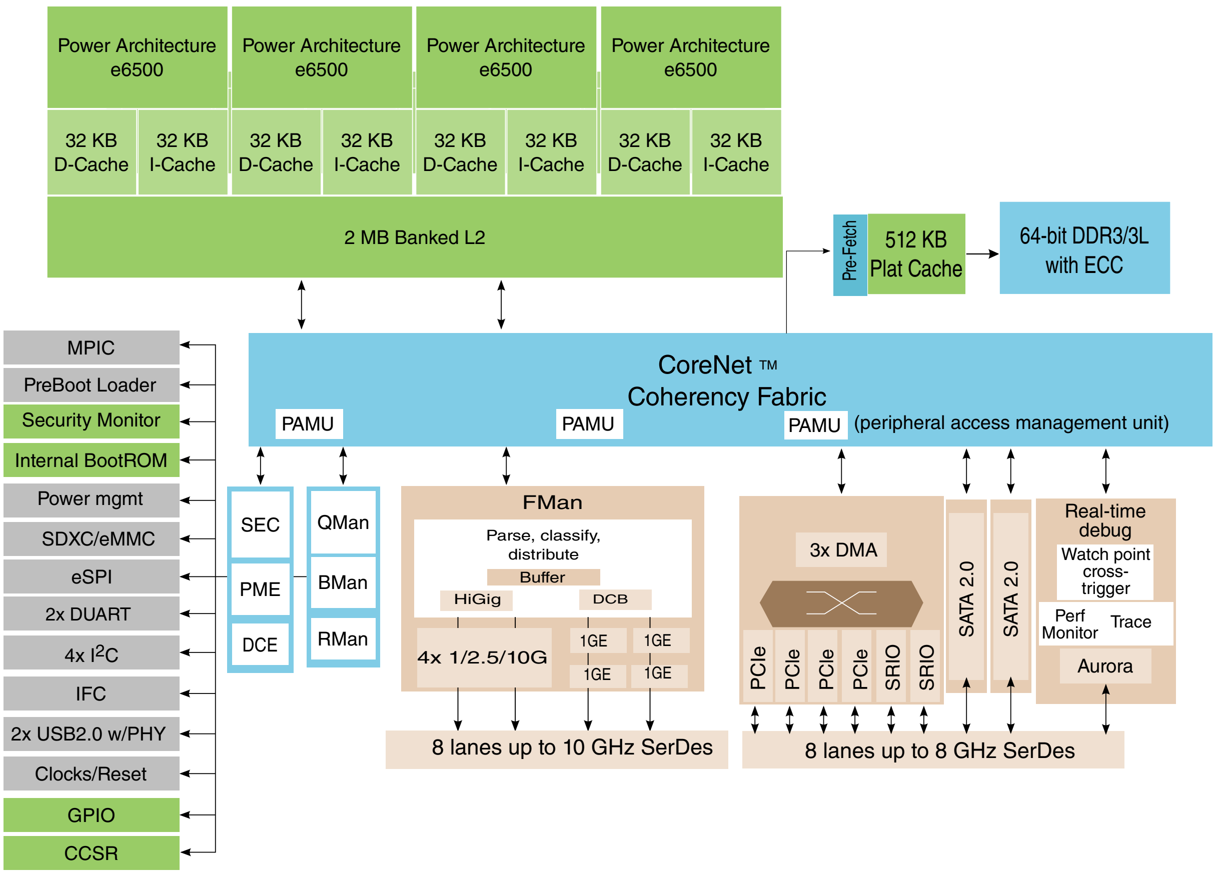


Figure 1. T2080 block diagram

This figure shows the major functional units of the T2081.

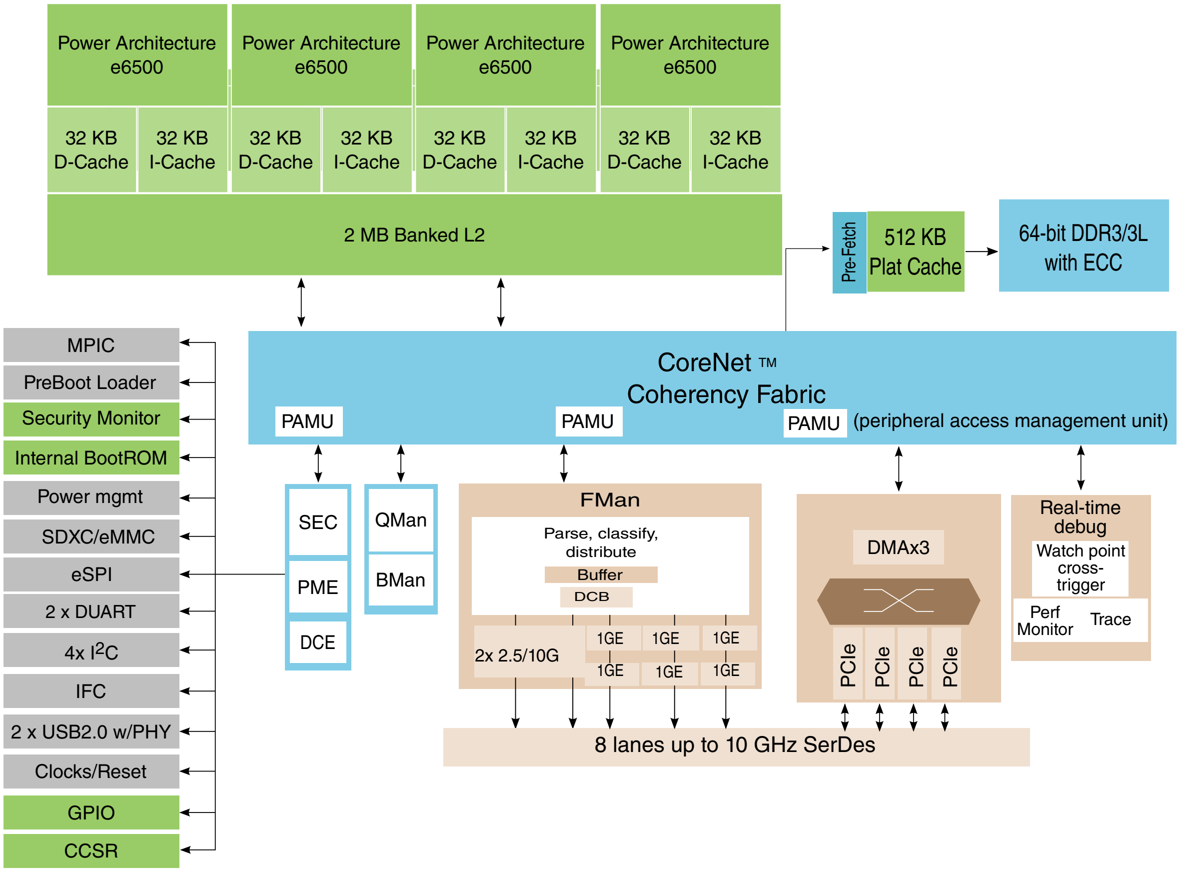


Figure 2. T2081 block diagram

3.1 Recommended resources

This table lists helpful tools, training resources, and documentation, some of which may be available only under a non-disclosure agreement (NDA). Contact your local field applications engineer or sales representative to obtain a copy.

Table 1. Helpful tools and references

ID	Name	Location
Related collateral		
T2080CE	*T2080 Chip Errata* **NOTE:** This document describes the latest fixes and workarounds for the chip. It is strongly recommended that this document be thoroughly researched prior to starting a design with the chip.	Contact your NXP representative
T2080/ T2081	*T2080 QorIQ Integrated Multicore Processor/ T2081 QorIQ Integrated Multicore Processor*	
T2080RM	*T2080 QorIQ Integrated Multicore Communications Processor Family Reference Manual*	www.nxp.com
e6500RM	*e6500 Core Reference Manual*	
ALTIVECPEM	*AltiVec Technology Programming Environments Manual*	

Table continues on the next page...

Table 1. Helpful tools and references (continued)

ID	Name	Location
ALTIVECPIM	*AltiVec Technology Programming Interface Manual*	
EREF_RM	*EREF 2.0: A Programmer's Reference Manual for Freescale Power Architecture® Processors*	
AN4326	*Verification of the IEEE 1588 Interface*	www.nxp.com
AN4311	*SerDes Reference Clock Interfacing and HSSI Measurements Recommendations*	
AN4290	*Configuring the Data Path Acceleration Architecture (DPAA)*	www.nxp.com
AN4039	*PowerQUICC and QorIQ DDR3/3L SDRAM Controller Register Setting Considerations*	
AN3940	*Hardware and Layout Design Considerations for DDR3 SDRAM Memory Interfaces*	www.nxp.com
AN3939	*DDR Interleaving for PowerQUICC and QorIQ Processors*	
AN2919	*Determining the I²C Frequency Divider Ratio for SCL*	
Models		
IBIS	To ensure first path success, NXP strongly recommends using the IBIS models for board level simulations, especially for SerDes and DDR characteristics.	www.nxp.com
BSDL	Use the BSDL files in board verification.	
Flotherm	Use the Flotherm model for thermal simulation. Especially without forced cooling or constant airflow, a thermal simulation should not be skipped.	
Available training		
-	Our third-party partners are part of an extensive alliance network. More information can be found at www.nxp.com/alliances.	www.nxp.com/alliances
-	Training materials from past Smart Network Developer's Forums and Freescale Technology Forums (FTF) are also available at our website. These training modules are a valuable resource for understanding the chip.	

3.2 Product revisions

This table lists the processor version register (PVR) and system version register (SVR) values for the various chip silicon derivatives.

Table 2. Revision level to part marking cross-reference

Part	Revision	e6500 core revision	Processor version register value	System version register value	Note
T2080E	1.0	2.0	8040_0020h	8538_0010h	—
T2080	1.0	2.0	8040_0020h	8530_0010h	—
T2081E	1.0	2.0	8040_0020h	8539_0010h	—
T2081	1.0	2.0	8040_0020h	8531_0010h	—
T2080E	1.1	2.0	8040_0120h	8538_0011h	—
T2080	1.1	2.0	8040_0120h	8530_0011h	—

Table continues on the next page...

Table 2. Revision level to part marking cross-reference (continued)

Part	Revision	e6500 core revision	Processor version register value	System version register value	Note
T2081E	1.1	2.0	8040_0120h	8539_0011h	—
T2081	1.1	2.0	8040_0120h	8531_0011h	—

4 Power design recommendations

4.1 Power pin recommendations

Table 3. Power and ground pin termination checklist

Signal name	Signal type	Used	Not used	Completed
AV_{DD}_CGA1	I	Power supply for cluster group A PLL 1 supply (1.8 V through a filter)	Must remain powered	
AV_{DD}_CGA2	I	Power supply for cluster group A PLL 2 supply (1.8 V through a filter)	Must remain powered	
AV_{DD}_D1	I	Power supply for DDR1 PLL (1.8 V through a filter)	Must remain powered	
AV_{DD}_PLAT	I	Power supply for Platform PLL (1.8 V through a filter)	Must remain powered	
AV_{DD}_SD1_PLL1	I	Power supply for SerDes1 PLL 1 (SerDes, filtered from X1VDD)	Must remain powered (no need to filter from X1VDD)	
AV_{DD}_SD1_PLL2	I	Power supply for SerDes1 PLL 2 (SerDes, filtered from X1VDD)	Must remain powered (no need to filter from X1VDD)	
AV_{DD}_SD2_PLL1	I	Power supply for SerDes2 PLL 1 (SerDes, filtered from X2VDD)	Must remain powered (no need to filter from X2VDD)	
AV_{DD}_SD2_PLL2	I	Power supply for SerDes2 PLL 2 (1SerDes, filtered from X2VDD)	Must remain powered (no need to filter from X2VDD)	
V_{DD}	I	Core and platform supply voltage		
S*n*V_{DD}	I	Core power supply for the SerDes logic transceiver (1.0 V)	Must remain powered	

Table continues on the next page...

Table 3. Power and ground pin termination checklist (continued)

Signal name	Signal type	Used	Not used	Completed
CV_{DD}	I	Power supply for the eSPI (1.8 V/2.5 V)	Must remain powered	
DV_{DD}	I	Power supply for the DUART, DMA, and I^2C (2.5 V/1.8 V)	Must remain powered	
$G1V_{DD}$	I	Power supply for the DDR3/3L (1.5 V/1.35 V)	Must remain powered	
LV_{DD}	I	Power supply for the Ethernet I/O, Ethernet management interface 1 (EMI1), 1588, GPIO (1.8 V/2.5 V)	Must remain powered	
OV_{DD}	I	Power supply for eSHDC, MPIC, GPIO, system control and power management, clocking, debug, IFC, DDRCLK supply, and JTAG I/O voltage (1.8 V)	Must remain powered	
V_{DD_LP}	I	Power supply for low power security monitor (1.0 V)	Must remain powered	
X*n*VDD	I	Pad power supply for the SerDes transceiver (1.35 V)	Must remain powered	
PROG_SFP	I	Should only be supplied 1.8 V during secure boot programming. For normal operation, this pin needs to be tied to GND.		
TH_V_{DD}	I	Thermal monitor unit supply (1.8 V)	Must remain powered	
USB_HV_{DD}	I	USB PHY Transceiver supply (3.3 V)	Tie to GND	
USB_OV_{DD}	I	USB PHY Transceiver supply (1.8 V)	Tie to GND	
USB_SV_{DD}	I	USB PHY Analog supply voltage (1.0 V)	Tie to GND	
SENSEVDD	O	V_{DD} sense pin	Connect to regulator feedback	
S*n*GND	I	SerDes core logic GND	Tie to GND	
X*n*GND	I	SerDes transceiver GND	Tie to GND	
GND	I	Ground	Tie to GND	
AGND_SD1_PLL1	I	SerDes 1 PLL 1 GND	Tie to GND	
AGND_SD1_PLL2	I	SerDes 1 PLL 2 GND	Tie to GND	
AGND_SD2_PLL1	I	SerDes 2 PLL 1 GND	Tie to GND	
AGND_SD2_PLL2	I	SerDes 2 PLL 2 GND	Tie to GND	
SENSEGND	O	GND sense pin	Connect to regulator feedback	
USB_AGND	I	USB PHY transceiver GND	Tie to GND	

4.2 Power system-level recommendations

Table 4. Power design system-level checklist

Item	Completed
General	

Table continues on the next page...

Table 4. Power design system-level checklist (continued)

Item	Completed
Ensure that the ramp rate for all voltage supplies (including CV_{DD}, DV_{DD}, OV_{DD}, GnV_{DD}, LV_{DD}, SnV_{DD}, and XnV_{DD}, all core and platform VDD supplies, D1_MVREF, and all AV_{DD} supplies) is less than 25 V/mS. Ramp rate is specified as a linear ramp from 10 to 90%. If non-linear (for example, exponential), the maximum rate of change from 200 to 500 mV is the most critical, because this range might falsely trigger the ESD circuitry. Required ramp rate for PROG_SFP should be less than 25 V/mS.	
Ensure that VDD nominal voltage supply is set for VID with voltage tolerance of +/- 30 mV from the nominal VDD value. Ensure that all other power supplies have a voltage tolerance no greater than 5% from the nominal value.[1]	
Ensure the power supply is selected based on MAXIMUM power dissipation.[1]	
Ensure the thermal design is based on THERMAL power dissipation.[1]	
Ensure the power-up sequence is within 400 ms.[1]	
Ensure the PLL filter circuit is applied to AV_{DD}_PLAT, AV_{DD}_CGA*n*, AV_{DD}_D1.	
If SerDes is enabled, ensure the PLL filter circuit is applied to the respective AV_{DD}_SD*n*_PLL*n* pins. Otherwise, a filter is not required. Even if an entire SerDes module is not used, the power is still needed to the AV_{DD} pins. However, instead of using a filter, it needs to be connected to the XV_{DD} rail through a zero Ω resistor.	
Ensure the PLL filter circuits are placed as close to the respective AV_{DD}_SD*n*_PLL*n* pins as possible.	
Power supply decoupling	
Provide sufficiently-sized power planes for the respective power rail. Use separate planes if possible; split (shared) planes if necessary. If split planes are used, ensure that signals on adjacent layers do not cross splits. Avoid splitting ground planes at all costs.	
Place at least one decoupling capacitor at each CV_{DD}, V_{DD}, DV_{DD}, OV_{DD}, $G1V_{DD}$, LV_{DD}, SnV_{DD}, and XnV_{DD} pin of this chip.	
It is recommended that the decoupling capacitors receive their power from separate CV_{DD}, V_{DD}, DV_{DD}, OV_{DD}, $G1V_{DD}$, LV_{DD}, SnV_{DD}, XnV_{DD}, and GND vias in the PCB, utilizing short traces to minimize inductance.	
Ensure the board has at least one 0.1 µF SMT ceramic chip capacitor as close as possible to each supply ball of the chip (CV_{DD}, V_{DD}, DV_{DD}, OV_{DD}, $G1V_{DD}$, LV_{DD}).	
Only use ceramic surface-mount technology (SMT) capacitors to minimize lead inductance, preferably 0402 or 0603.	
Distribute several bulk storage capacitors around the PCB, feeding the V_{DD} and other planes (for example, CV_{DD}, DV_{DD}, OV_{DD}, $G1V_{DD}$, LV_{DD}, SnV_{DD}, and XnV_{DD} planes to enable quick recharging of the smaller chip capacitors.	
Ensure the bulk capacitors have a low equivalent series-resistance (ESR) rating to ensure the quick response time necessary.	
Ensure the bulk capacitors are connected to the power and ground planes through two vias to minimize inductance.	
Ensure you work directly with your power regulator vendor for best values and types of bulk capacitors. The capacitors need to be selected to work well with the power supply to be able to handle the chip's power requirements. [2] Most regulators perform best with a mix of ceramic and very low ESR Tantalum type capacitors.	
SerDes power supply decoupling	
Use only SMT capacitors to minimize inductance.	
Connections from all capacitors to power and ground must be done with multiple vias to further reduce inductance.	

Table continues on the next page...

Table 4. Power design system-level checklist (continued)

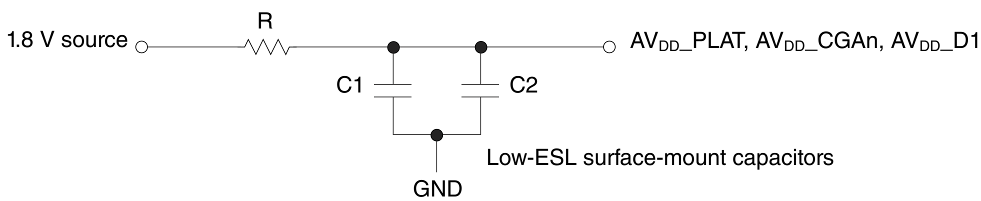
Item	Completed
Ensure the board has at least one 0.1 µF SMT ceramic chip-capacitor as close as possible to each supply ball of the chip (SnV_{DD}, XnV_{DD}).	
Where the board has blind vias, ensure these capacitors are placed directly below the chip supply and ground connections.	
Where the board does not have blind vias, ensure these capacitors are placed in a ring around the chip as close to the supply and ground connections as possible.	
For all SerDes supplies: Ensure there is a 1 µF ceramic chip capacitor on each side of the chip.	
For all SerDes supplies: Ensure there is a 10 µF, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100 µF, low ESR SMT tantalum chip capacitor between the device and any SerDes voltage regulator.	
PLL power supply filtering[3]	
Provide independent filter circuits per PLL power supply, as illustrated in this figure. Where: • R = 5 Ω ± 5% • C1 = 10 µF ± 10%, 0603, X5R, with ESL ≤ 0.5 nH • C2 = 1.0 µF ± 10%, 0402, X5R, with ESL ≤ 0.5 nH • Low-ESL surface-mount capacitors **NOTE:** A higher capacitance value for C2 may be used to improve the filter as long as the other C2 parameters do not change (0402 body, X5R, ESL ≤ 0.5 nH). **NOTE:** Voltage for AV_{DD} is defined at the input of the PLL supply filter and not the pin of AV_{DD}.  	
Ensure filter circuits use surface mount capacitors with minimum effective series inductance (ESL).	
Place each circuit as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. **NOTE:** If done properly, it is possible to route directly from the capacitors to the AV_{DD} pins, without the added inductance of vias. **NOTE:** It is recommended that an area fill or power plane split be provided to provide a low-impedance profile, which helps keep nearby crosstalk noise from inducing unwanted noise.	
Ensure each of the PLLs is provided with power through independent power supply pins (AV_{DD}_PLAT, AV_{DD}_CGA*n*, AV_{DD}_D1, and AV_{SDn_PLL}, respectively).	
For maximum effectiveness, ensure the filter circuit is placed as close as possible to the AV_{DD}_SD*n*_PLL*n* ball to ensure it filters out as much noise as possible.	
Ensure the ground connection is near the AV_{DD}_SD*n*_PLL*n* ball. The 0.003 µF capacitor is closest to the ball, followed by a 4.7 µF capacitor and 47 µf capacitors, and finally the 0.33 Ω resistor to the board supply plane.	
To ensure stability of the internal clock, ensure the power supplied to the PLL is filtered using a circuit similar to the one shown in this figure. Note the following: • AV_{DD}_SD*n*_PLL*n* should be a filtered version of XnV_{DD}. • Signals on the SerDes interface are fed from the XnV_{DD} power plane.	

Table continues on the next page...

Table 4. Power design system-level checklist (continued)

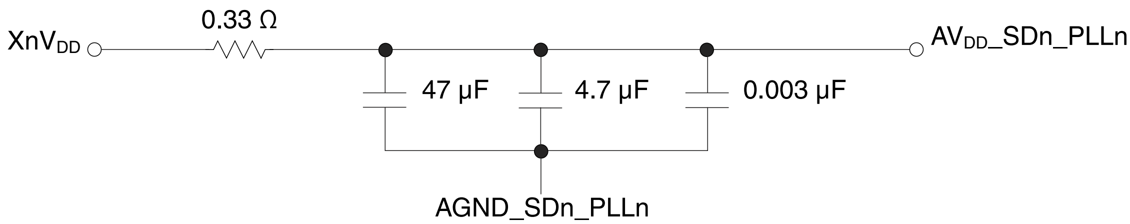
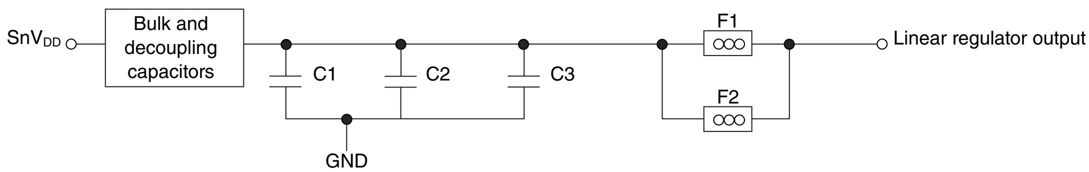
Item	Completed
• It is recommended that an area fill or power plane split be provided for both AV_{DD} and AGND to provide a low-impedance profile, which helps keep nearby crosstalk noise from inducing unwanted noise. • Voltage for AV_{DD}_SD*n*_PLL*n* is defined at the PLL supply filter and not the pin of AV_{DD}_SD*n*_PLL*n*. • A 47 µF 0805 XR5 or XR7, 4.7 µF 0603, and 0.003 µF 0402 capacitor are recommended. The size and material type are important. A 0.33 Ω ± 1% resistor is recommended. • **Caution**: These filters are a necessary extension of the PLL circuitry and are compliant with the device specifications. Any deviation from the recommended filters is done at the user's risk. 	
Ensure the capacitors are connected from AV_{DD}_SD*n*_PLL*n* to the ground plane.	
Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide, and direct.	
Ensure AV_{DD}_SD*n*_PLL*n* is a filtered version of X*n*V_{DD}.	
There must be dedicated analog ground AGND_SD*n*_PLL*n* for each AV_{DD}_SD*n*_PLL*n* pin up to the physical locale of the filters themselves.	
S*n*V_{DD} may be supplied by a linear regulator or sourced by a filtered V_{DD}. Systems may design-in both options to allow flexibility to address system noise dependencies. However, for initial system bring-up, the linear regulator option is highly recommended. An example solution for S*n*V_{DD} filtering, where S*n*V_{DD} is sourced from a linear regulator, is shown in the following figure. The component values in this example filter are system-dependent and are still under characterization, so component values may need adjustment based on the system or environment noise. Where: • C1 = 0.003 µF ± 10%, X5R, with ESL ≤ 0.5 nH • C2 and C3 = 2.2 µF ± 10%, X5R, with ESL ≤ 0.5 nH • F1 and F2 = 120 Ω at 100 MHz 2A 25% 0603 Ferrite (for example, Murata BLM18PG121SH1) • Bulk and decoupling capacitors are added, as needed, per power supply design.  **NOTE:** See section "Power-on ramp rate" in the applicable chip data sheet for maximum S*n*V_{DD} power-up ramp rate. **NOTE:** There must be enough output capacitance or a soft-start feature to assure the ramp-rate requirement is met. **NOTE:** Besides a linear regulator, a low-noise-dedicated switching regulator can be used. 10 mVp-p, 50 kHz to 500 MHz is the noise goal.	
X*n*V_{DD} may be supplied by a linear regulator or sourced by a filtered G1V_{DD}. Systems may design-in both options to allow flexibility to address system noise dependencies. However, for initial system bring-up, the linear regulator option is highly recommended. An example solution for X*n*V_{DD} filtering, where X*n*V_{DD} is	

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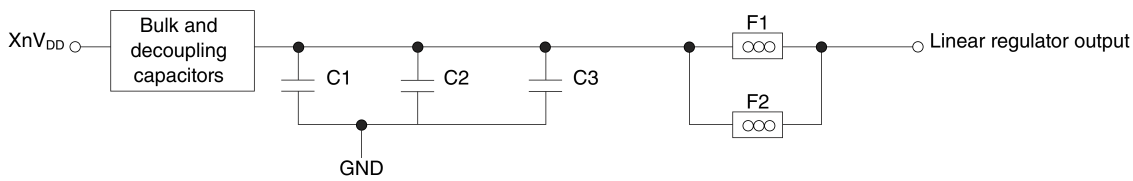
Table 4. Power design system-level checklist (continued)

<table>
<tr><th>Item</th><th>Completed</th></tr>
<tr><td>
sourced from a linear regulator, is shown in the following figure. The component values in this example filter are system-dependent and are still under characterization, so component values may need adjustment based on the system or environment noise.

Where:

C1 = 0.003 μF ± 10%, X5R, with ESL ≤ 0.5 nH
C2 and C3 = 2.2 μF ± 10%, X5R, with ESL ≤ 0.5 nH
F1 and F2 = 120 Ω at 100 MHz 2A 25% 0603 Ferrite (for example, Murata BLM18PG121SH1)
Bulk and decoupling capacitors are added, as needed, per power supply design.



NOTE: See section "Power-on ramp rate" in the applicable chip data sheet for maximum XnV$_{DD}$ power-up ramp rate.
NOTE: There must be enough output capacitance or a soft-start feature to assure the ramp-rate requirement is met.
NOTE: The ferrite beads should be placed in parallel to reduce voltage droop.
NOTE: Besides a linear regulator, a low-noise-dedicated switching regulator can be used. 10 mVp-p, 50 kHz to 500 MHz is the noise goal.
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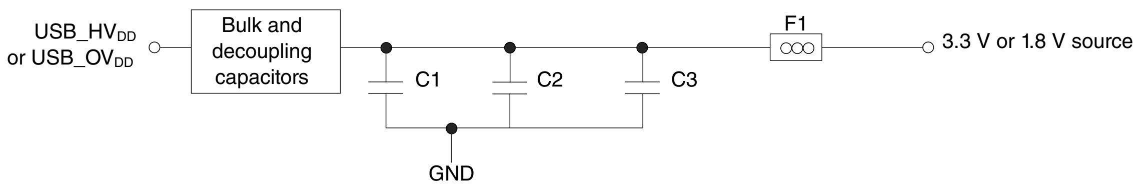
USB_HV$_{DD}$ and USB_OV$_{DD}$ must be sourced by a filtered 3.3 V and 1.8 V voltage source using a star connection. An example solution for USB_HV$_{DD}$ and USB_OV$_{DD}$ filtering, where USB_HV$_{DD}$ and USB_OV$_{DD}$ are sourced from a 3.3 V and 1.8 V voltage source, is illustrated in the following figure. The component values in this example filter is system-dependent and are still under characterization, so component values may need adjustment based on the system or environment noise.

Where:

C1 = 0.003 μF ± 10%, X5R, with ESL ≤ 0.5 nH
C2 and C3 = 2.2 μF ± 10%, X5R, with ESL ≤ 0.5 nH
F1 = 120 Ω at 100 MHz 2A 25% 0603 Ferrite (for example, Murata BLM18PG121SH1)
Bulk and decoupling capacitors are added, as needed, per power supply design.



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<tr><td>
USB_SV$_{DD}$ must be sourced by a filtered V$_{DD}$ using a star connection. An example solution for USB_SV$_{DD}$ filtering, where USB_SV$_{DD}$ is sourced from V$_{DD}$, is illustrated in the following figure. The component values in this example filter are system-dependent and are still under characterization, so component values may need adjustment based on the system or environment noise.

Where:

C1 = 2.2 μF ± 20%, X5R, with low ESL (for example, Panasonic ECJ0EB0J225M)
F1 = 120 Ω at 100-MHz 2A 25% Ferrite (for example, Murata BLM18PG121SH1)
Bulk and decoupling capacitors are added, as needed, per power supply design

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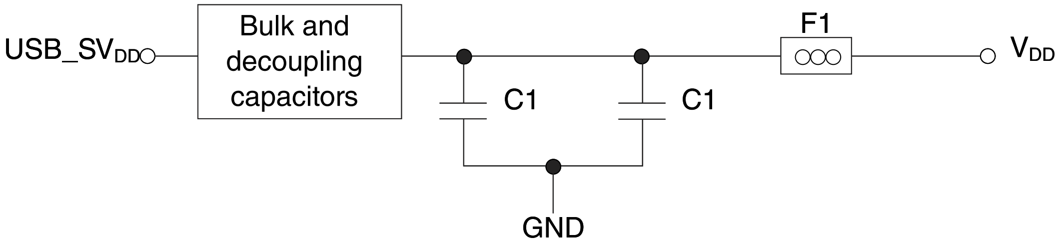
Table 4. Power design system-level checklist (continued)

Item	Completed
	
Use ceramic chip capacitors with the highest possible self-resonant frequency. All traces should be kept short, wide, and direct.	

1. See the applicable chip data sheet for more details.
2. Suggested bulk capacitors are 100-330 µF (AVX TPS tantalum or Sanyo OSCON).
3. The PLL power supply filter circuit filters noise in the PLLs' resonant frequency range from 500 kHz to 10 MHz.

4.3 Power-on reset recommendations

Various chip functions are initialized by sampling certain signals during the assertion of PORESET_B. These power-on reset (POR) inputs are pulled either high or low during this period. While these pins are generally output pins during normal operation, they are treated as inputs while PORESET_B is asserted. When PORESET_B de-asserts, the configuration pins are sampled and latched into registers, and the pins then take on their normal output circuit characteristics.

Table 5. Power-on reset system-level checklist

Item	Completed
Ensure PORESET_B is asserted for a minimum of 1 ms.	
Ensure HRESET_B is asserted for a minimum of 32 SYSCLK cycles.	
In cases where a configuration pin has no default, use a 4.7 kΩ pull-up or pull-down resistor for appropriate configuration of the pin.	
Optional: An alternative to using pull-up and pull-down resistors to configure the POR pins is to use a PLD or similar device that drives the configuration signals to the chip when HRESET_B is asserted. The PLD must begin to drive these signals at least four SYSCLK cycles prior to the de-assertion of PORESET_B (PLL configuration inputs must meet a 100 µs set-up time to HRESET_B), hold their values for at least two SYSCLK cycles after the de-assertion of PORESET_B, and then release the pins to high impedance afterward for normal device operation **NOTE:** See the applicable chip data sheet for details about reset initialization timing specifications.	
Configuration settings	
Ensure the settings in the "Configuration signals sampled at reset" section of the reference manual are selected properly. **NOTE:** See the applicable chip reference manual for a more detailed description of each configuration option.	

5 Interface recommendations

5.1 DDR SDRAM Memory Interface 1 pin termination recommendations

Table 6. DDR SDRAM Memory Interface 1 pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
D1_MAPAR_ERR_B	I	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan. Recommend that a weak pull-up resistor (4.7 kΩ) be placed on this pin to the respective power supply.	Pull up whether used or not used.	
D1_MAPAR_OUT	O	If the controller supports the optional MAPAR_OUT and MAPAR_ERR signals, ensure that they are hooked up as follows: • MAPAR_OUT (from the controller) => PAR_IN (at the RDIMM) • ERR_OUT (from the RDIMM) => MAPAR_ERR (at the controller).	May be left unconnected.	
D1_MA[0:15]	O	Must be properly terminated to VTT.	May be left unconnected.	
D1_MBA[0:2]	O	Must be properly terminated to VTT.	May be left unconnected.	
D1_MCAS_B	O	Must be properly terminated to VTT.	May be left unconnected.	
D1_MCKE[0:3]	O	Must be properly terminated to VTT. This output is actively driven during reset rather than being tri-stated during reset.	May be left unconnected.	
D1_MCK[0:3]	O	Ensure these pins are terminated correctly.	May be left unconnected.	
D1_MCS[0:3]_B	O	Must be properly terminated to VTT.	May be left unconnected.	
D1_MDIC[0:1]	I/O	MDIC[0] is grounded through an 187 Ω precision 1% resistor and MDIC[1] is connected to GV_{DD} through an 187 Ω precision 1% resistor. For either full or half driver strength calibration of DDR I/Os, use the same MDIC resistor value of 187 Ω. Memory controller register setting can be used to	May be left unconnected.	

Table continues on the next page...

Table 6. DDR SDRAM Memory Interface 1 pin termination checklist (continued)

Signal Name	I/O type	Used	Not Used	Completed
		determine automatic calibration is done to full or half drive strength. These pins are used for automatic calibration of the DDR3/DDR3L I/Os. The MDIC[0:1] pins must be connected to 187 Ω precision 1% resistors.		
D1_MDM[0:8]	O	—	May be left unconnected.	
D1_MDQS[0:8]_B	I/O	—	May be left unconnected.	
D1_MDQ[0:63]	I/O	—	May be left unconnected.	
D1_MECC[0:7]	I/O	—	May be left unconnected.	
D1_MODT[0:3]	O	Ensure the MODT signals are connected correctly. In general, for dual-ranked DIMMS, the following should all go to the same physical memory bank: • MODT(0), MCS(0), MCKE(0) • MODT(1), MCS(1), MCKE(1) • MODT(2), MCS(2), MCKE(2) • MODT(3), MCS(3), MCKE(3) For quad-ranked DIMMS, it is recommended to obtain a data sheet from the memory supplier to confirm required signals. But in general, each controller needs MCS(0:3), MODT(0:1), and MCKE(0:1) connected to the one quad-ranked DIMM.	May be left unconnected.	
D1_MRAS_B	O	Must be properly terminated to VTT.	May be left unconnected.	
D1_MWE_B	O	Must be properly terminated to VTT.	May be left unconnected.	

5.2 Integrated Flash Controller pin termination recommendations

Table 7. Integrated Flash Controller pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
IFC_AD[0:15]	I/O	This pin is a reset configuration pin. It has a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the device is in its reset state. This pull-up is designed to be overpowered by an external 4.7 kΩ resistor. If the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.		

Table continues on the next page...

Table 7. Integrated Flash Controller pin termination checklist (continued)

Signal Name	I/O type	Used	Not Used	Completed
IFC_AVD	O	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan. Pin must **NOT** be pulled down during power-on reset. This pin may be pulled up, driven high, or if there are any connected devices, left in tristate. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.		
IFC_A[16:20]	O	Pin must NOT be pulled down during power-on reset. This pin may be pulled up, driven high, or if there are any externally connected devices, left in tristate. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset. Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.		
IFC_A[21]	O	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan. This pin is a reset configuration pin. It has a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the device is in its reset state. This pull-up is designed to be overpowered by an external 4.7 kΩ resistor. If the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.		
IFC_A[22:31]	O	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.		
IFC_BCTL	O	This output is actively driven during reset rather than being tri-stated during reset.	May be left unconnected.	
IFC_CLE	O	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan. This pin is a reset configuration pin. It has a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the device is in its reset state. This pull-up is designed to be overpowered by an external 4.7 kΩ resistor. If the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.		
IFC_CLK[0:1]	O	This output is actively driven during reset rather than being tri-stated during reset.	May be left unconnected.	

Table continues on the next page...

Table 7. Integrated Flash Controller pin termination checklist (continued)

Signal Name	I/O type	Used	Not Used	Completed
IFC_CS[0:7]_B	O	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan. Recommend that a weak pull-up resistor (4.7 kΩ) be placed on this pin to the respective power supply.	May be left unconnected.	
IFC_NDDDR_CLK	O	This output is actively driven during reset rather than being tri-stated during reset.	May be left unconnected.	
IFC_NDDQS	I/O	Connect as needed.	May be left unconnected.	
IFC_OE_B	O	Pin must **NOT** be pulled down during power-on reset. This pin may be pulled up, driven high, or if there are any connected devices, left in tristate. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset. Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.		
IFC_PAR[0:1]	I/O	Connect as needed.	May be left unconnected.	
IFC_PERR_B	I	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.	Pull high through a 4-7 kΩ resistor to OV_{DD} or can be left floating if configured as outputs via the GPIO_GPDIR register.	
IFC_RB[0:4]_B	I	Recommend that a weak pull-up resistor (1 kΩ) be placed on this pin to the respective power supply.		
IFC_TE	O	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan. This pin is a reset configuration pin. It has a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the device is in its reset state. This pull-up is designed to be overpowered by an external 4.7 kΩ resistor. If the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.		
IFC_WE[0]_B	O	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.		

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Table 7. Integrated Flash Controller pin termination checklist (continued)

Signal Name	I/O type	Used	Not Used	Completed
		Pin must **NOT** be pulled down during power-on reset. This pin may be pulled up, driven high, or if there are any connected devices, left in tristate. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.		
IFC_WP[0]_B	O	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan. Pin must **NOT** be pulled down during power-on reset. This pin may be pulled up, driven high, or if there are any connected devices, left in tristate. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.		
IFC_WP[1:3]_B	O	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.		

5.3 DUART pin termination recommendations

Table 8. DUART pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
UART1_CTS_B	I	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.	Pull high through a 2-10 kΩ resistor to DV_{DD}.	
UART1_RTS_B	O	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.	May be left unconnected.	
UART1_SIN	I	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.	Pull low through a 2-10 kΩ resistor to GND.	

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Table 8. DUART pin termination checklist (continued)

Signal Name	I/O type	Used	Not Used	Completed
UART1_SOUT	O	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.	May be left unconnected.	
UART2_CTS_B	I	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.	Pull high through a 2-10 kΩ resistor to DV_{DD}.	
UART2_RTS_B	O	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.	May be left unconnected.	
UART2_SIN	I	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.	Pull low through a 2-10 kΩ resistor to GND.	
UART2_SOUT	O	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.	May be left unconnected.	

5.4 I2C pin termination recommendations

Table 9. I2C pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
IIC1_SCL	I/O	This pin is an open-drain signal.	Pull high through a 2-10 kΩ resistor to DV_{DD}.	

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Table 9. I2C pin termination checklist (continued)

Signal Name	I/O type	Used	Not Used	Completed
		Recommend that a weak pull-up resistor (1 kΩ) be placed on this pin to the respective power supply.		
IIC1_SDA	I/O	This pin is an open-drain signal. Recommend that a weak pull-up resistor (1 kΩ) be placed on this pin to the respective power supply.	Pull high through a 2-10 kΩ resistor to DV_{DD}.	
IIC2_SCL	I/O	This pin is an open-drain signal. Recommend that a weak pull-up resistor (1 kΩ) be placed on this pin to the respective power supply.	Pull high through a 2-10 kΩ resistor to DV_{DD}.	
IIC2_SDA	I/O	This pin is an open-drain signal. Recommend that a weak pull-up resistor (1 kΩ) be placed on this pin to the respective power supply.	Pull high through a 2-10 kΩ resistor to DV_{DD}.	
IIC3_SCL	I/O	This pin is an open-drain signal. Recommend that a weak pull-up resistor (1 kΩ) be placed on this pin to the respective power supply.	Pull high through a 2-10 kΩ resistor to DV_{DD}.	
IIC3_SDA	I/O	This pin is an open-drain signal. Recommend that a weak pull-up resistor (1 kΩ) be placed on this pin to the respective power supply.	Pull high through a 2-10 kΩ resistor to DV_{DD}.	
IIC4_SCL	I/O	This pin is an open-drain signal. Recommend that a weak pull-up resistor (1 kΩ) be placed on this pin to the respective power supply.	Pull high through a 2-10 kΩ resistor to DV_{DD}.	
IIC4_SDA	I/O	This pin is an open-drain signal. Recommend that a weak pull-up resistor (1 kΩ) be placed on this pin to the respective power supply.	Pull high through a 2-10 kΩ resistor to DV_{DD}.	

5.5 eSPI Interface pin termination recommendations

Table 10. eSPI Interface pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
SPI_CLK	O	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other	Pull low through a 2-10 kΩ resistor to GND.	

Table continues on the next page...

Table 10. eSPI Interface pin termination checklist (continued)

Signal Name	I/O type	Used	Not Used	Completed
		manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.		
SPI_CS[0:3]_B	O	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan. If used as an SDHC signal, pull up 10-100 kΩ to the respective I/O supply.	May be left unconnected.	
SPI_MISO	I	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.	Pull high through a 2-10 kΩ resistor to CV_{DD}.	
SPI_MOSI	I/O	—	Pull high through a 2-10 kΩ resistor to CV_{DD}.	

5.6 eSDHC pin termination recommendations

Table 11. eSDHC pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
SDHC_CD_B	I	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.	Pull high through a 10-50 kΩ resistor to OV_{DD}.	
SDHC_CLK	I/O	—	May be left unconnected.	
SDHC_CMD	I/O	If used as an SDHC signal, pull up 10-100 kΩ to the respective I/O supply.	Pull high through a 10-50 kΩ resistor to OV_{DD}.	
SDHC_DAT[0:7]	I/O	If used as an SDHC signal, pull up 10-100 kΩ to the respective I/O supply.	Pull high through a 10-50 kΩ resistor to OV_{DD}.	

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Table 11. eSDHC pin termination checklist (continued)

Signal Name	I/O type	Used	Not Used	Completed
SDHC_WP	I	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.	Pull high through a 10-50 kΩ resistor to OV_{DD}.	

5.7 Programmable Interrupt Controller pin termination recommendations

Table 12. Programmable Interrupt Controller pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
IRQ[0:11]	I	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.	Pull high through 2-10 kΩ resistors to the respective power supply.	
IRQ_OUT_B	O	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan. Recommend that a weak pull-up resistor (4.7 kΩ) be placed on this pin to the respective power supply. This pin is an open-drain signal.	Pull high through 2-10 kΩ resistors to OV_{DD}.	

5.8 LP Trust pin termination recommendations

Table 13. LP Trust pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
LP_TMP_DETECT_B	I	If a tamper sensor is used, it must maintain the signal at the specified voltage until a tamper is detected. A 1 kΩ pull-down resistor is strongly recommended.	Pull high through a 2-10 kΩ resistor to VDD_LP.	

5.9 Trust pin termination recommendations

Table 14. Trust pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
TMP_DETECT_B	I	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan. If a tamper sensor is used, it must maintain the signal at the specified voltage until a tamper is detected. A 1 kΩ pull-down resistor is strongly recommended.	Pull high through 2-10 kΩ resistors to OV_{DD}.	

5.10 System Control pin termination recommendations

Table 15. System Control pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
HRESET_B	I/O	This pin is an open-drain signal. Recommend that a weak pull-up resistor (4.7 kΩ) be placed on this pin to the respective power supply.		
PORESET_B	I	This pin is required to be asserted as per the applicable chip data sheet, in relation to minimum assertion time and during power up/ power down. It is an input-only pin and must be asserted to sample power-on configuration pins.		
RESET_REQ_B	O	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.		

Table 15. System Control pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
		Pin must **NOT** be pulled down during power-on reset. This pin may be pulled up, driven high, or if there are any connected devices, left in tristate. If this pin is connected to a device that pulls down during reset, an external pull-up is required to drive this pin to a safe state during reset.		

5.11 Power Management pin termination recommendations

Table 16. Power Management pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
ASLEEP	O	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan. This pin is a reset configuration pin. It has a weak (~20 kΩ) internal pull-up P-FET that is enabled only when the device is in its reset state. This pull-up is designed to be overpowered by an external 4.7 kΩ resistor. If the signal is intended to be high after reset, and if there is any device on the net that might pull down the value of the net at reset, a pull-up or active driver is needed.		

5.12 SYSCLK pin termination recommendations

Table 17. SYSCLK pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
SYSCLK	I	This pin must always be connected to a 66.7 to 133.3 MHz input clock.		

5.13 DDR Clocking pin termination recommendations

Table 18. DDR Clocking pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
DDRCLK	I	This pin must always be connected to a 66.7 to 133.3 MHz input clock.		

5.14 RTC pin termination recommendations

Table 19. RTC pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
RTC	I	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.	Pull low through a 2-10 kΩ resistor to GND.	

5.15 Debug pin termination recommendations

Table 20. Debug pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
CKSTP_OUT_B	O	This pin is an open-drain signal. Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan. Recommend that a weak pull-up resistor (4.7 kΩ) be placed on this pin to the respective power supply.		
CLK_OUT	O	This output is actively driven during reset rather than being tri-stated during reset.		
EVT[0:4]_B	I/O	EVT[0]_B has a weak (~20 kΩ) internal pull-up P-FET that is always enabled.	Pull high through 2-10 kΩ resistors to OV_{DD}.	
EVT[5:6]_B	I/O	—	Pull high through 2-10 kΩ resistors to OV_{DD}.	
EVT[7:8]_B	I/O	—	Pull high through 2-10 kΩ resistors to OV_{DD}.	
EVT[9]_B	I/O	—	Pull high through 2-10 kΩ resistors to OV_{DD}.	

5.16 DFT pin termination recommendations

Table 21. DFT pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
SCAN_MODE_B	I	These are test signals for factory use only and must be pulled up (100 Ω to 1 kΩ) to the respective power supply for normal operation.		

Table continues on the next page...

Table 21. DFT pin termination checklist (continued)

Signal Name	I/O type	Used	Not Used	Completed
TEST_SEL_B	I	These are test signals for factory use only and must be pulled up (100 Ω to 1 kΩ) to the respective power supply for normal operation.		

5.17 Analog Signals pin termination recommendations

Table 22. Analog Signals pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
D1_MVREF	I/O	DDR reference voltage: 0.49 x GV_{DD} to 0.51 x $GVOV_{DD}$. D1_MVREF can be generated using a divider from GV_{DD} as MVREF. Another option is to use supplies that generate GV_{DD}, VTT, and D1_MVREF voltage. These methods help reduce differences between GV_{DD} and MVREF. D1_MVREF generated from a separate regulator is not recommended, because D1_MVREF does not track GV_{DD} as closely.	Must be pulled to ground (GND).	
D1_TPA	I/O	Do not connect. These pins should be left floating.		
FA_ANALOG_G_V	I/O	Must be pulled to ground (GND).		
FA_ANALOG_PIN	I/O	Must be pulled to ground (GND).		
TD1_ANODE	I/O	These pins should be tied to ground if the diode is not utilized for temperature monitoring.		
TD1_CATHODE	I/O	These pins should be tied to ground if the diode is not utilized for temperature monitoring.		
TH_TPA	—	Do not connect. These pins should be left floating.		

5.18 SerDes 1 pin termination recommendations

Table 23. SerDes 1 pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
SD1_IMP_CAL_RX	I	This pin requires a 200 Ω pull up to the respective power supply.	If the SerDes interface is entirely unused, the unused pin must be left unconnected.	
SD1_IMP_CAL_TX	I	This pin requires a 698 Ω pull up to the respective power supply.	If the SerDes interface is entirely unused, the unused pin must be left unconnected.	

Table continues on the next page...

Table 23. SerDes 1 pin termination checklist (continued)

Signal Name	I/O type	Used	Not Used	Completed
SD1_PLL1_TPA	O	Do not connect. These pins should be left floating.		
SD1_PLL1_TPD	O	Do not connect. These pins should be left floating.		
SD1_PLL2_TPA	O	Do not connect. These pins should be left floating.		
SD1_PLL2_TPD	O	Do not connect. These pins should be left floating.		
SD1_REF_CLK[1:2]_P	I	Ensure clocks are driven correctly.	If the SerDes *n* lanes are not used in the system, connect to S*n*GND, where *n* corresponds to the unused SerDes lanes.	
SD1_REF_CLK[1:2]_N	I	Ensure clocks are driven correctly.	If the SerDes *n* lanes are not used in the system, connect to S*n*GND, where *n* corresponds to the unused SerDes lanes.	
SD1_RX[0:7]_P	I	Ensure these pins are terminated correctly.	If the SerDes interface is entirely or partly unused, the unused pins must be connected to S*n*GND.	
SD1_RX[0:7]_N	I	Ensure these pins are terminated correctly.	If the SerDes interface is entirely or partly unused, the unused pins must be connected to S*n*GND.	
SD1_TX[0:7]_P	O	Ensure these pins are terminated correctly.	If the SerDes interface is entirely or partly unused, the unused pins must be left unconnected.	
SD1_TX[0:7]_N	O	Ensure these pins are terminated correctly.	If the SerDes interface is entirely or partly unused, the unused pins must be left unconnected.	

5.19 SerDes 2 pin termination recommendations

NOTE

SerDes 2 does not apply to T2081.

Table 24. SerDes 2 pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
SD2_IMP_CAL_RX	I	This pin requires a 200 Ω pull up to the respective power supply.	If the SerDes interface is entirely unused, the unused pin must be left unconnected.	
SD2_IMP_CAL_TX	I	This pin requires a 698 Ω pull-up to the respective power-supply.	If the SerDes interface is entirely unused, the unused pin must be left unconnected.	
SD2_PLL1_TPA	O	Do not connect. These pins should be left floating.		
SD2_PLL1_TPD	O	Do not connect. These pins should be left floating.		
SD2_PLL2_TPA	O	Do not connect. These pins should be left floating.		
SD2_PLL2_TPD	O	Do not connect. These pins should be left floating.		

Table continues on the next page...

Table 24. SerDes 2 pin termination checklist (continued)

Signal Name	I/O type	Used	Not Used	Completed
SD2_REF_CLK[1:2]_P	I	Ensure clocks are driven correctly.	If the SerDes *n* lanes are not used in the system, connect to S*n*GND, where *n* corresponds to the unused SerDes lanes.	
SD2_REF_CLK[1:2]_N	I	Ensure clocks are driven correctly.	If the SerDes *n* lanes are not used in the system, connect to S*n*GND, where *n* corresponds to the unused SerDes lanes.	
SD2_RX[0:7]_P	I	Ensure these pins are terminated correctly.	If the SerDes interface is entirely or partly unused, the unused pins must be connected to S*n*GND.	
SD2_RX[0:7]_N	I	Ensure these pins are terminated correctly.	If the SerDes interface is entirely or partly unused, the unused pins must be connected to S*n*GND.	
SD2_TX[0:7]_P	O	Ensure these pins are terminated correctly.	If the SerDes interface is entirely or partly unused, the unused pins must be left unconnected.	
SD2_TX[0:7]_N	O	Ensure these pins are terminated correctly.	If the SerDes interface is entirely or partly unused, the unused pins must be left unconnected.	

5.20 USB PHY 1 & 2 pin termination recommendations

Table 25. USB PHY 1 & 2 pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
USB1_DRVVBUS	O	—	May be left unconnected.	
USB1_PWRFAULT	I	—	Pull low through a 1 kΩ resistor to GND.	
USB1_UDM	I/O	—	May be left unconnected.	
USB1_UDP	I/O	—	May be left unconnected.	
USB1_UID	I	—	Pull low through a 1 kΩ resistor to GND.	
USB1_VBUSCLMP	I	—	Pull low through a 1 kΩ resistor to GND.	
USB2_DRVVBUS	O	—	May be left unconnected.	
USB2_PWRFAULT	I	—	Pull low through a 1 kΩ resistor to GND.	
USB2_UDM	I/O	—	May be left unconnected.	
USB2_UDP	I/O	—	May be left unconnected.	
USB2_UID	I	—	Pull low through a 1 kΩ resistor to GND.	
USB2_VBUSCLMP	I	—	Pull low through a 1 kΩ resistor to GND.	

Table continues on the next page...

Table 25. USB PHY 1 & 2 pin termination checklist (continued)

Signal Name	I/O type	Used	Not Used	Completed
USBCLK	I	—	Pull low through a 1 kΩ resistor to GND.	
USB_IBIAS_REXT	I/O	New board designs should leave a placeholder for a parallel series resistor and capacitor filter to be used in very close proximity to the USB_IBAIS_REXT pin of NXP QorIQ chips. When needed, this allows for flexibility in populating them, which helps avoid board-coupled noise to this pin. A 100 nF low-ESL SMD ceramic chip capacitor in series with a 100 Ω SMD resistor performs the needed filtration with slight variations that suit each board case.	May be left unconnected.	

5.21 IEEE1588 pin termination recommendations

Table 26. IEEE1588 pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
TSEC_1588_ALARM_OUT[1:2]	O	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.	May be left unconnected.	
TSEC_1588_CLK_IN	I	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan. Connect to external high-precision timer reference input.	Pull low through a 2-10 kΩ resistor to GND.	
TSEC_1588_CLK_OUT	O	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.	May be left unconnected.	

Table continues on the next page...

Table 26. IEEE1588 pin termination checklist (continued)

Signal Name	I/O type	Used	Not Used	Completed
TSEC_1588_PULSE_OUT[1:2]	O	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.	May be left unconnected.	
TSEC_1588_TRIG_IN[1:2]	I	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.	Pull low through a 2-10 kΩ resistor to GND.	

5.22 Ethernet Management Interface 1 pin termination recommendations

Table 27. Ethernet Management Interface 1 pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
EMI1_MDC	O	—	May be left unconnected.	
EMI1_MDIO	I/O	Tie high through a 2-10 kΩ resistor to LV_{DD}.	Pull low through a 2-10 kΩ resistor to GND.	

5.23 Ethernet Management Interface 2 pin termination recommendations

Table 28. Ethernet Management Interface 2 pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
EMI2_MDC	O	This pin is an open-drain signal. These pins must be pulled up to 1.2 V through a 180 Ω ± 1% resistor for MDC and a 330 Ω ± 1% resistor for MDIO.	May be left unconnected.	
EMI2_MDIO	I/O	This pin is an open-drain signal.	Pull low through a 2-10 kΩ resistor to GND.	

Table 28. Ethernet Management Interface 2 pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
		These pins must be pulled up to 1.2 V through a 180 Ω ± 1% resistor for MDC and a 330 Ω ± 1% resistor for MDIO.		

5.24 Ethernet Controller (RGMII) 1 pin termination recommendations

Table 29. Ethernet Controller (RGMII) 1 pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
EC1_GTX_CLK	O	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.	May be left unconnected.	
EC1_GTX_CLK125	I	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.	Pull low through a 2-10 kΩ resistor to GND.	
EC1_RXD[0:3]	I	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.	Pull low through a 2-10 kΩ resistor to GND.	
EC1_RX_CLK	I	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.	Pull low through a 2-10 kΩ resistor to GND.	
EC1_RX_CTL	I	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other	Pull low through a 2-10 kΩ resistor to GND.	

Table continues on the next page...

Table 29. Ethernet Controller (RGMII) 1 pin termination checklist (continued)

Signal Name	I/O type	Used	Not Used	Completed
		manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.		
EC1_TXD[0:3]	O	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.	May be left unconnected.	
EC1_TX_CTL	O	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan. This pin requires an external 1-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.	May be left unconnected.	

5.25 Ethernet Controller (RGMII) 2 pin termination recommendations

Table 30. Ethernet Controller (RGMII) 2 pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
EC2_GTX_CLK	O	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.	May be left unconnected.	
EC2_GTX_CLK125	I	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.	Pull low through a 2-10 kΩ resistor to GND.	

Table continues on the next page...

Table 30. Ethernet Controller (RGMII) 2 pin termination checklist (continued)

Signal Name	I/O type	Used	Not Used	Completed
EC2_RXD[0:3]	I	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.	Pull low through a 2-10 kΩ resistor to GND.	
EC2_RX_CLK	I	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.	Pull low through a 2-10 kΩ resistor to GND.	
EC2_RX_CTL	I	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.	Pull low through a 2-10 kΩ resistor to GND.	
EC2_TXD[0:3]	O	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.	May be left unconnected.	
EC2_TX_CTL	O	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan. This pin requires an external 1-kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven.	May be left unconnected.	

5.26 DMA pin termination recommendations

Table 31. DMA pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
DMA1_DACK[0]_B	O	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.	May be left unconnected.	
DMA1_DDONE[0]_B	O	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.	May be left unconnected.	
DMA1_DREQ[0]_B	I	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.	Pull high through a 2-10 kΩ resistor to DV_{DD}.	
DMA2_DACK[0]_B	O	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.	May be left unconnected.	
DMA2_DDONE[0]_B	O	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.	May be left unconnected.	
DMA2_DREQ[0]_B	I	Functionally, this pin is an output or an input, but structurally it is an I/O because it either samples configuration input during reset, is a muxed pin, or has other manufacturing test functions. This pin will therefore be described as an I/O for boundary scan.	Pull high through a 2-10 kΩ resistor to DV_{DD}.	

5.27 JTAG pin termination recommendations

Table 32. JTAG pin termination checklist

Signal Name	I/O type	Used	Not Used	Completed
TCK	I	If COP is used, connect as needed and strap to OV_{DD} via a 10kΩ pull up.	Pull high through 2-10 kΩ resistors to OV_{DD}.	
TDI	I	This pin has a weak (~20 kΩ) internal pull-up P-FET that is always enabled.	May be left unconnected.	
TDO	O	This output is actively driven during reset rather than being tri-stated during reset.	May be left unconnected.	
TMS	I	This pin has a weak (~20 kΩ) internal pull-up P-FET that is always enabled.	May be left unconnected.	
TRST_B	I	This pin has a weak (~20 kΩ) internal pull-up P-FET that is always enabled. Connect as shown in the JTAG interface connection figure below.	Tie TRST_B to HRESET_B through a 0 kΩ resistor.	

5.27.1 JTAG system-level recommendations

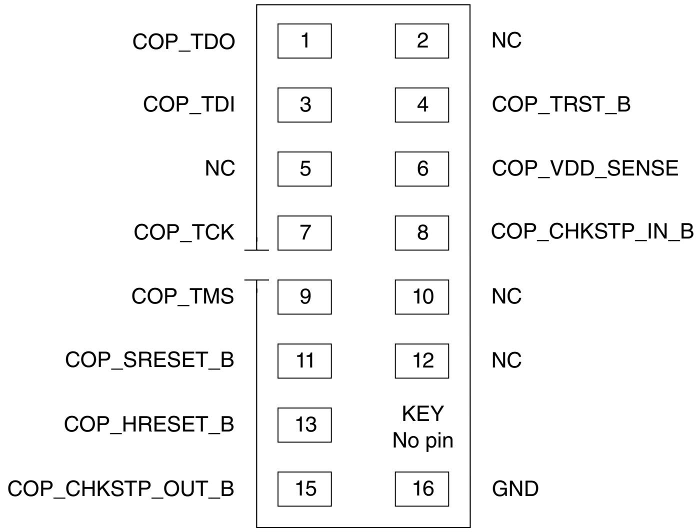
Table 33. JTAG system-level checklist

Item	Completed
COP signal interface to JTAG port	
Configure the group of system control pins as shown in Figure 3. **NOTE:** These pins must be maintained at a valid deasserted state under normal operating conditions, because most have asynchronous behavior and spurious assertion gives unpredictable results.	
The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert PORESET_B or TRST_B in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.	
Boundary-scan testing	
Ensure that TRST_B is asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. **NOTE:** While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert TRST_B during the power-on reset flow. Simply tying TRST_B to PORESET_B is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.	

Table continues on the next page...

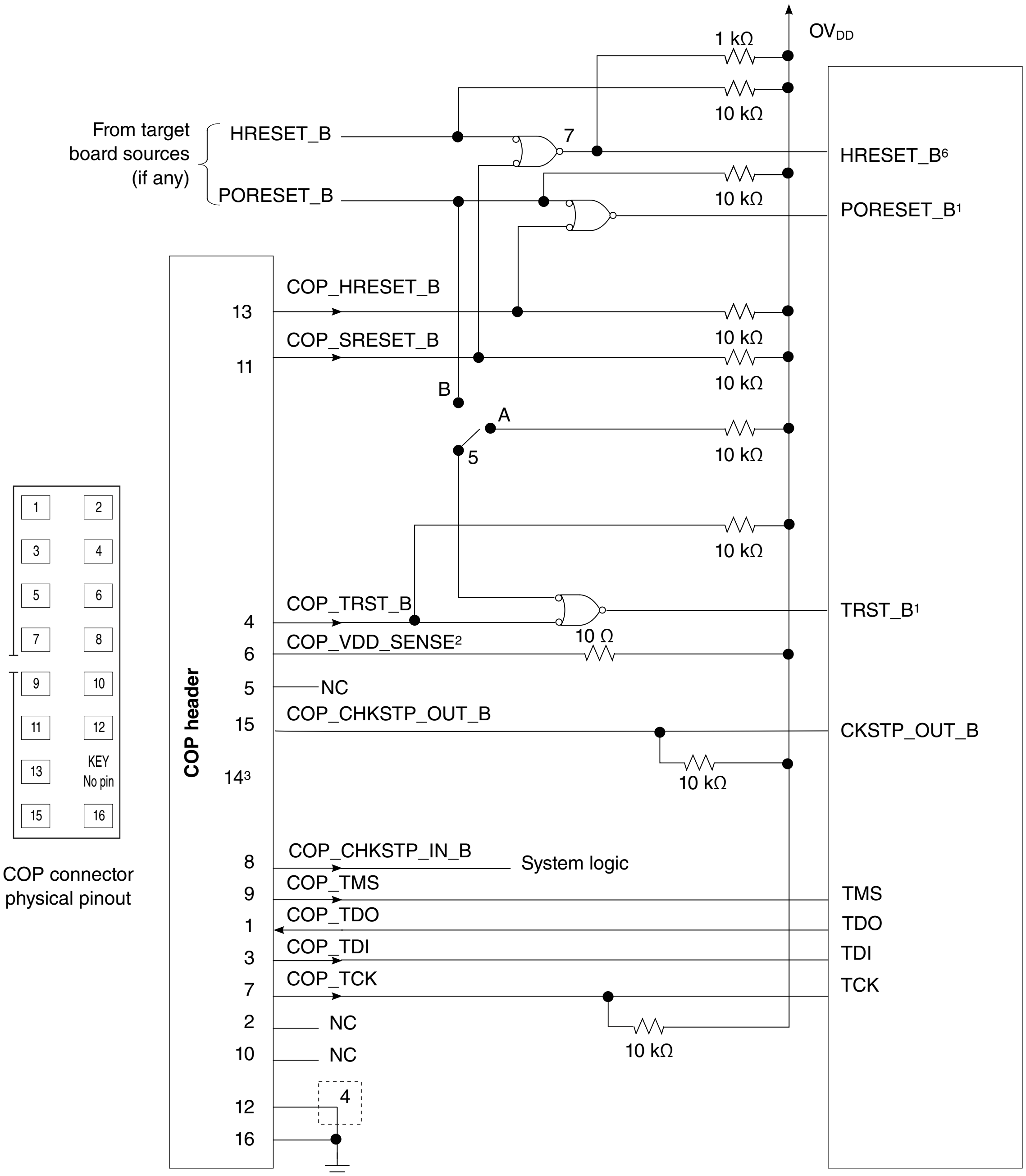
Table 33. JTAG system-level checklist (continued)

<table>
<tr><th>Item</th><th>Completed</th></tr>
<tr><td>Follow the arrangement shown in Figure 3 to allow the COP port to assert PORESET_B or TRST_B independently while ensuring that the target can drive PORESET_B as well.</td><td></td></tr>
<tr><td>The COP interface has a standard header, shown in the following figure, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key. There is no standardized way to number the COP header, so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in this figure is common to all known emulators.



NOTE: The COP header adds many benefits such as breakpoints, watch points, register and memory examination/modification, and other standard debugger features. An inexpensive option is to leave the COP header unpopulated until needed.</td><td></td></tr>
</table>

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 3. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions, as most have asynchronous behavior and spurious assertion gives unpredictable results.



Notes:

1. The COP port and target board should be able to independently assert PORESET_B and TRST_B to the processor in order to fully control the processor as shown here.

2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.

3. The KEY location (pin 14) is not physically present on the COP header.

4. Although pin 12 is defined as a no-connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.

5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the TRST_B line. If BSDL testing is not being performed, this switch should be closed to position B.

6. Asserting HRESET_B causes a hard reset on the device

7. This is an open-drain output gate.

Figure 3. JTAG interface connection

5.28 Aurora configuration signals

Correct operation of the Aurora interface requires configuration of a group of system control pins as demonstrated in the figures below. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion will give unpredictable results.

NXP recommends that the Aurora 34 pin duplex connector be designed into the system as shown in Figure 6 or the 70 pin duplex connector be designed into the system as shown in Figure 7.

If the Aurora interface will not be used, NXP recommends the legacy COP header be designed into the system as described in "Termination of unused signals" in the chip reference manual.

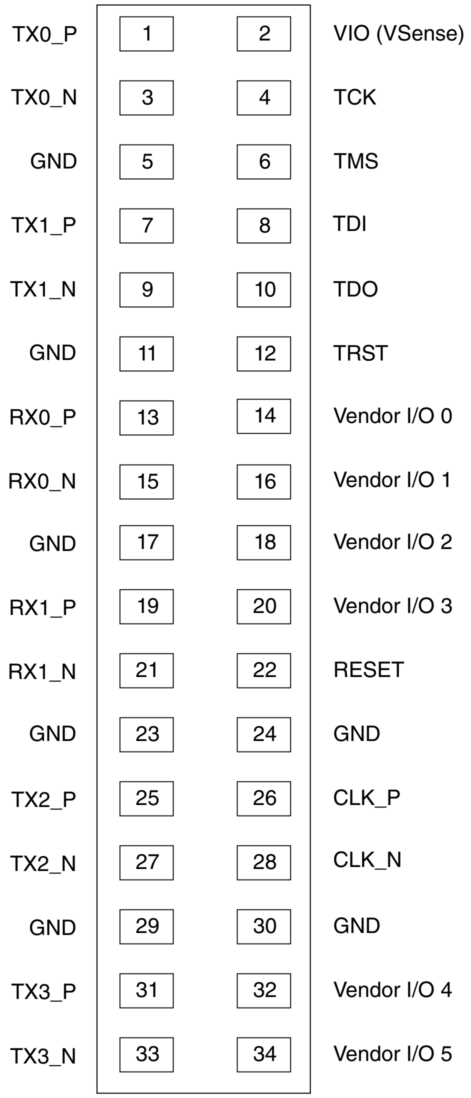
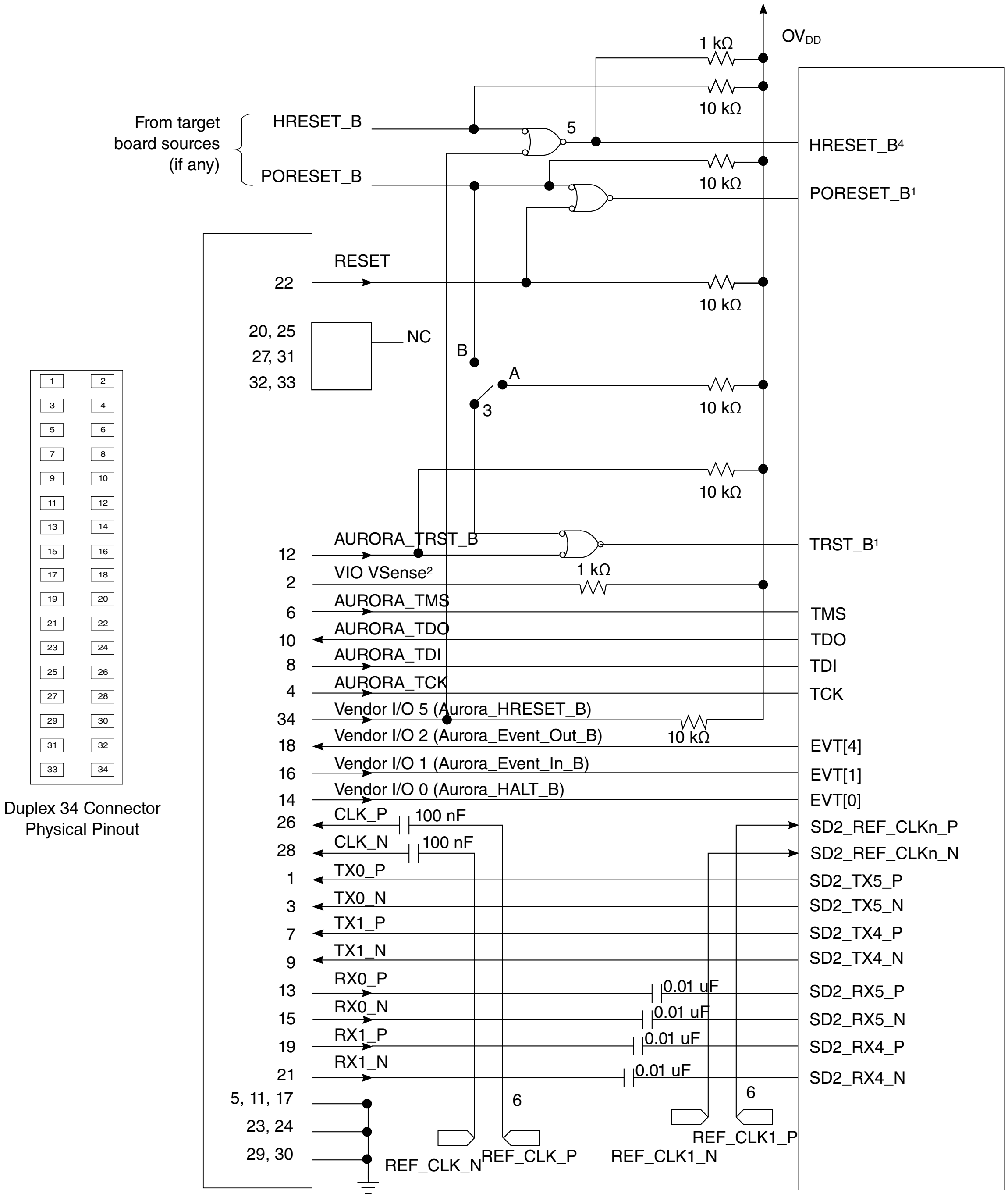


Figure 4. Aurora 34 pin connector duplex pinout

TX0_P	1	2	VIO (VSense)
TX0_N	3	4	TCK
GND	5	6	TMS
TX1_P	7	8	TDI
TX1_N	9	10	TDO
GND	11	12	TRST
RX0_P	13	14	Vendor I/O 0
RX0_N	15	16	Vendor I/O 1
GND	17	18	Vendor I/O 2
RX1_P	19	20	Vendor I/O 3
RX1_N	21	22	RESET
GND	23	24	GND
TX2_P	25	26	CLK_P
TX2_N	27	28	CLK_N
GND	29	30	GND
TX3_P	31	32	Vendor I/O 4
TX3_N	33	34	Vendor I/O 5
GND	35	36	GND
RX2_P	37	38	N/C
RX2_N	39	40	N/C
GND	41	42	GND
RX3_P	43	44	N/C
RX3_N	45	46	N/C
GND	47	48	GND
TX4_P	49	50	N/C
TX4_N	51	52	N/C
GND	53	54	GND
TX5_P	55	56	N/C
TX5_N	57	58	N/C
GND	59	60	GND
TX6_P	61	62	N/C
TX6_N	63	64	N/C
GND	65	66	GND
TX7_P	67	68	N/C
TX7_N	69	70	N/C

Figure 5. Aurora 70 pin connector duplex pinout



Notes:

1. The Aurora port and target board should be able to independently assert PORESET_B and TRST_B to the processor in order to fully control the processor as shown here.

2. Populate this with a 1 kΩ resistor for short-circuit/current-limiting protection.

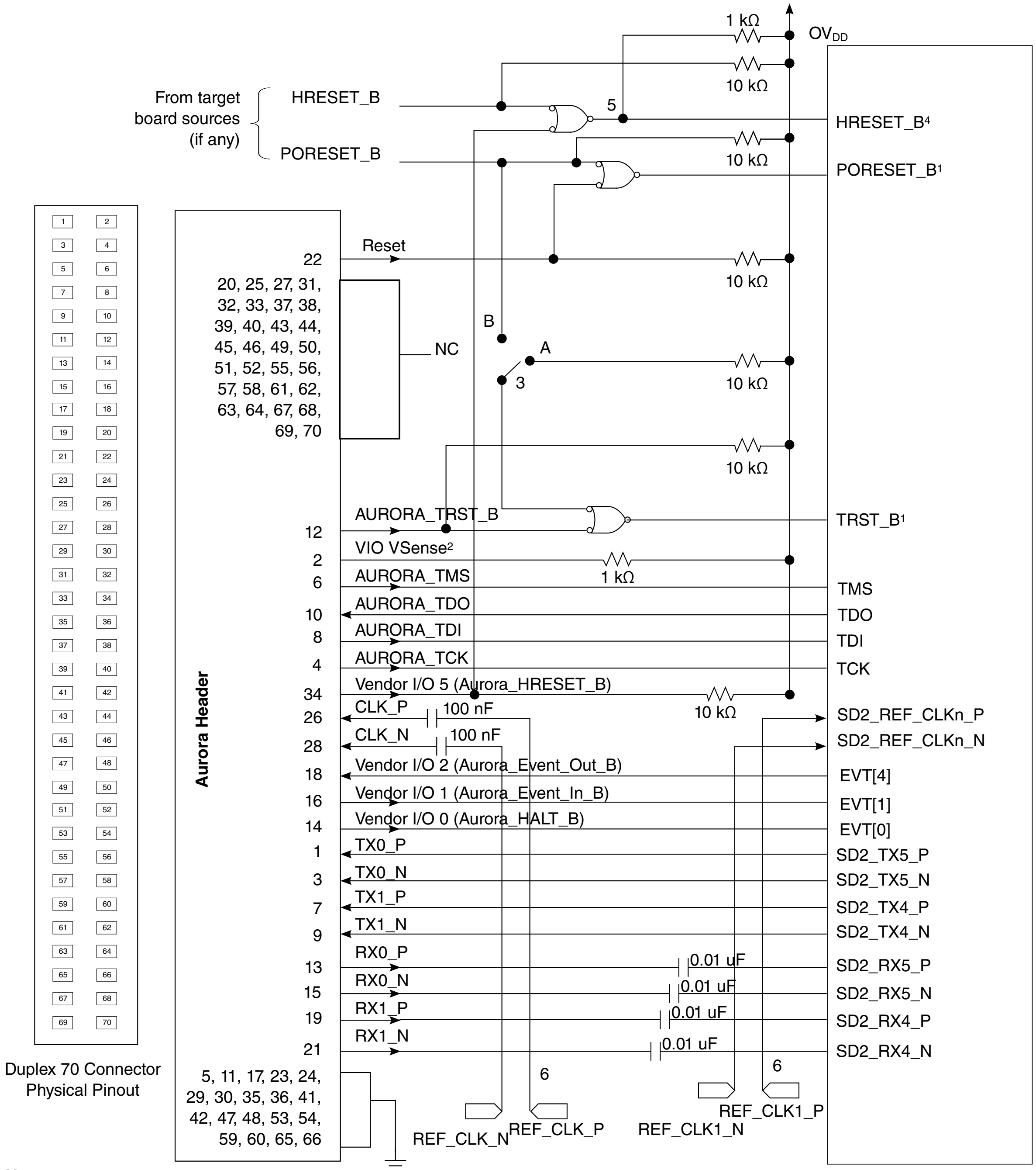
3. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the TRST_B line. If BSDL testing is not being performed, this switch should be closed to position B.

4. Asserting HREST_B causes a hard reset on the device

5. This is an open-drain output gate.

6. REF_CLK_P/REF_CLK_N and REF_CLK1_P/REFCLK1_N are buffered clocks from the same common source.

Figure 6. Aurora 34 pin connector duplex interface connection



Notes:

1. The Aurora port and target board should be able to independently assert PORESET_B and TRST_B to the processor in order to fully control the processor as shown here.

2. Populate this with a 1 kΩ resistor for short-circuit/current-limiting protection.

3. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the TRST_B line. If BSDL testing is not being performed, this switch should be closed to position B.

4. Asserting HREST_B causes a hard reset on the device

5. This is an open-drain output gate.

6. REF_CLK_P/REF_CLK_N and REF_CLK1_P/REFCLK1_N are buffered clocks from the same common source.

Figure 7. Aurora 70 pin connector duplex interface connection

6 Revision history

This table summarizes changes to this document.

Table 34. Revision history

Revision	Date	Change
3	01/2018	• In Power system-level recommendations, changed power-up sequence from 75 ms to 400 ms • Updated company name from "Freescale" to "NXP" within document content
2	09/2015	• In Table 7, added the IFC_WP[0]_B signal.
1	09/2015	• In Table 3, added 1.8 V for LV_{DD} GPIO and removed the EMI2 supply. • In Table 4, removed "F2" from the USB_HV_{DD} and USB_OV_{DD} row. • In Table 7, changed the IFC_WP[0:3]_B signal name to IFC_WP[1:3]_B and removed the note about not pulling the pin down during power on reset. • In Table 12, updated the "Not Used" column for IRQ[0:11]. • In Table 23, added "Used" descriptions for the SD1_TX[0:7]_P and SD1_TX[0:7]_N signals.
0	04/2015	Initial public release

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Document Number AN4804
Revision 3, 01/2018

BUILT ON Power