Freescale Semiconductor
Application Note

Document Number:AN4865
Rev. 0, 01/2014

TFT Panel Support in the MPC5645S Microcontroller Family

How to Choose a Suitable Panel and Configure MPC5645S

by: Marie-Anne Le Menn and Steve McAslan

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1 Introduction

Each Display Control Unit (DCU) module on the MPC5645S MCU family is capable of driving a TFT LCD panel of different sizes. The upper limit on the size of each panel depends on a range of factors including DCU clock speed, platform clock speed, memory interface speed, graphic data encoding, and number of graphic layers active. This application note explains how each of these factors contributes to the limit and provides guidelines for the maximum panel size for various MCU configurations.

2 The DCU modules

The DCU performs two primary tasks on the MPC5645S architecture. First, it fetches composites and blends graphics dynamically from on- or off-chip memory. Second, it provides the final graphic content to a TFT LCD panel connected to the MPC5645S GPIO pads.

The DCU itself provides fundamental and practical upper limits to the panel size. There are no practical lower limits because the DCU supports all known available small panel sizes.

Since the DCU does not rely on a frame buffer, its performance is dependent on the availability and speed of the memory in or attached to the MPC5645S. A graphic is fetched

from memory when it is associated with a DCU layer. The DCU3 module allows any combination of up to 16 layers to be displayed at a time and up to four of these layers to be blended together at each individual output pixel value. The DCULite module allows any combination of up to four layers to be displayed at a time and up to two of these layers to be blended together at each individual output pixel value. Therefore, the peak demand from the DCU3 is four graphics at the highest quality encoding of 32 bits-per-pixel (BPP). Each of those source graphics can come from any memory location; so the peak demand on a specific memory interface would also be 4 x 32 BPP. In the case of DCULite the peak demand would be 2 x 32 BPP.

2.1 Hardware upper limits to panel size

Configuration of the DCU panel interface is described in detail in *AN4444: Configuring and Using the DCU3 and DCULite on the MPC5645S*, available on **freescale.com**. This configuration allows a number of upper values that define the specification limits on panel size. However, in practice, most panels will be smaller than the size that the specification allows.

The absolute maximum size of a panel that can be connected to the MPC5645S is 1024x1024 pixels as defined by the DCU DISP_SIZE register, but this is not a practical size because for a normal 60 Hz refresh rate, the panel would require a pixel clock value of greater than 300 MHz which is higher than the clock architecture can supply.

The pixel clock in the DCU is derived from among the FMPLL0, the FMPLL1, the 16MHz internal RC oscillator, or the 4-16 MHz external oscillator clock sources on the MCU, which gives a usual upper limit of 125 MHz. It gives a theoretical panel size limit of approximately 1024x768 pixels (corresponding to a pixel clock of 47 MHz).

2.2 Pixel clock rates and content of panel

This pixel output clock rate is limited in usability by the challenge of high speed circuit design (especially EMC). It is also limited by the rate at which pixels can be fetched since the DCU must fetch and blend each of the pixels before outputting them to the panel.

All incoming pixels must pass across the internal crossbar (XBAR) which typically operates at 125 MHz and allows 64-bit transfers. Therefore the DCU can fetch each 32 BPP layer at a peak rate of 250 Mpixels/s (two pixels per clock cycle). This data rate must be shared among all layers that are visible on the panel so the peak rate is actually 250 Mpixels per second per layer.

This means that the rate at which layers can be fetched is reduced by the number of overlapping layers in the design. For example a frame which uses 4 x 32 BPP overlapping layers means that each of the layers can have one pixel fetched at an average incoming rate of 62.5 Mpixels/s. Since all incoming pixels must be fetched before a single output pixel can be displayed this in turn means that the maximum rate of the output pixel clock is also 62.5 MHz.

In practice, a pixel clock rate closer to 60 MHz is more reasonable because it is more straightforward to create from the source clock frequency. This pixel clock value would support a panel of 1024 x 768 but although this may be a practical hardware limit, it is likely that memory and display specifications will reduce this further.

2.3 Impact of memory bandwidth

The MPC5645S MCU supports various memory types of which the highest bandwidth performance is found on SDRAM, on-chip RAM (OCRAM), and serial flash (QuadSPI). Other memory sources are also available but do not have the speed or the memory-mapping required by the DCU.

It is necessary to understand the effect of memory bandwidth on the DCU configuration to see how it affects usable panel sizes.

2.3.1 Impact of memory availability

Some members of the MPC5645S family include an DRAM interface which allows up to 2 GB to be connected to the system while others have a limit of 1.5 MB of on-chip RAM (OCRAM). It is likely that the size of available RAM will be an upper limit on the graphic content available and indirectly on the size of the panel that can be connected. This is because the DCU fetches graphics stored in memory to display on the panel and the less memory there is, the less sophisticated or (more likely) the smaller the panel may be.

For this reason, a MPC5645S application with no external DRAM limits the maximum panel size because there is simply not enough memory to store the graphics required for the application and the external memory available is too slow.

2.3.2 Influence of memory speed

As previously discussed in Pixel clock rates and content of panel, the DCU can fetch pixels at a peak rate of 250 Mpixels/s for a 32 BPP graphic. This is equivalent to a raw transfer rate of just under 1 GB/s. This means that the memory system must also be able to provide a combined operating rate as fast to allow the DCU to operate at its maximum performance and so support the largest panel possible.

- SDRAM: The maximum SDRAM data rate is 500 MB/s which is based on a 125 MHz bus, DDR2 memory, and a 32-bit interface. At this rate, it would be possible to supply approximately 4 x 32 BPP layers each frame to the DCU3 for a 60 MHz pixel clock where only graphics are stored in the SDRAM and layer access is at its most efficient level. The peak SDRAM rate allows a reasonable assumption that the 1 GB/s peak bandwidth could be comfortably achieved while allowing for random data access into the memory. Alternatively, the memory could supply graphic content to the DCU3 and the DCULite simultaneously.
- OCRAM: The OCRAM also operates at the platform clock of 125 MHz and provides a 64-bit interface. Therefore its bandwidth is also approximately 1 GB/s or 4 x 32 BPP layers each frame (at 60 MHz). The limitation with this memory is that it cannot be increased in size.
- Serial flash: The slowest and most cost-effective of these memories is the serial flash attached to the QuadSPI module. This interface is available, allowing 4-bit single data rate operation, but also two serial flashes to operate in parallel giving an effective 8-bit transfer at single data rate. A typical operating specification for the fastest option is 80 MHz which yields a peak memory bandwidth of 80 MB/s. In practice, the effective bandwidth is less because of the command overhead of each memory read but a sustained rate of more than 60 MB/s is considered a realistic expectation. This supports around 1 x 16 BPP layer each frame for a 40 MHz pixel clock. Reducing the pixel clock speed obviously increases the number of layers that can be fetched.

Given the above calculations, it is apparent that even with a fast DDR2 SDRAM, the largest panel supported with full color encoding is WVGA (800 x 480, c. 33 MHz). The use of external flash will further reduce this capacity if direct fetch from memory is required.

However, there are many techniques that can be employed to minimize the memory bandwidth and capacity required and thereby allow more layers to be blended on a larger panel.

2.4 Memory optimization techniques

There are three benefits of optimizing the requirements for graphic memory:

- Graphics which use fewer BPP for each pixel can make more efficient use of bandwidth.
- Graphics which take less space in memory save cost by reducing the overall memory footprint.
- Buffering graphics from slower and cheaper memory into RAM allows better performance.

It is possible to reduce the footprint of the graphics by using more advanced features of the MPC5645S. The memory space saving that is achievable depends heavily on the specific graphics and may come at the expense of time to display the image.

The MPC5645S includes a number of features that make it possible to reduce the memory footprint required for a given application. These include:

- Optimizing the original graphic encoding and using tile mode of the DCU

- Compressing the graphic data using Run Length Encoding (RLE) and using either the DCU (available only for the two first layers) or independent RLE module to unpack the image when required
- Generate graphics as required using the OpenVG Graphics Processing Unit (GPU)
- Using the DMA module to rotate and mirror graphics instead of storing multiple images

Each of these features is explained in the following subsections.

2.4.1 Optimizing graphic encoding

The DCU can display graphics in 13 different encodings without loss of quality in the blend.

NOTE

The quality of the image is always determined by the source graphic format.

In most cases, the use of 32 BPP ARGB images is excessive. There are various factors which make this the case:

- Most MPC5645S applications will be on relatively small panels with limited resolution and limited brightness.
- The range of colors and gradients in most images can be easily represented by a smaller color gamut.
- Many applications only require a 16- or 18-bit panel and so, full 24-bit RGB color is wasteful unless the temporal dithering function is enabled.

Given these factors, it is normal for many applications to use 16-bit formats as a standard. This immediately doubles the effective number of layers which can be stored in memory and fetched with a given bandwidth. For some images, a look-up-table format is suitable; available formats include 8 BPP which gives a 256 color palette. More likely is that applications can use the 8 BPP Transparency format which gives full-quality alpha anti-aliasing for a given image color. Either of these two latter options give 4x bandwidth and footprint benefits. All of these options can be used in combination, so it is possible to use a single high-quality 32 BPP image along with 8 BPP or 16 BPP formats on a single frame.

When analyzing panel options, a combination of format usages is assumed.

2.4.2 Compressing the graphics

The memory footprint may be reduced by compressing the source graphic using RLE. There are two options to decompress the image.

- Standalone module: The standalone module does not allow any net saving of memory bandwidth since the decompressed image must ultimately be stored into memory although the decoding can be done during frame refresh porches.
- DCU module: This module decompresses the RLE data internally (for the two first layers) and so it does save some bandwidth as well as memory space; however, there are more restrictions on this approach (limited format support, partial extraction not possible and limited to one layer at a time)

The usefulness of RLE compression is entirely dependent on the source image but since it is lossless, it is a simple exercise to examine the benefit of the approach by compressing the image.

2.4.3 Using the OpenVG GPU

The OpenVG GPU allows the creation and manipulation of images and so removes the need to store them in external flash and subsequently copy them to RAM. There is no direct saving of memory bandwidth since the images must always be stored in RAM before use; however, only the images required for the current or upcoming frames need to be stored in RAM.

The OpenVG engine can draw and translate images using vector data or source raster images and in both cases, significant memory savings can be made by manipulating the images as they are needed for the display.

2.4.4 Manipulate images using the DMA

The MPC5645S includes an advanced Direct Memory Access module called the eDMA which allows manipulation of data ordering while a copy is taking place. This DMA uses independent inner and outer loops to calculate how to choose the next source and destination address and this allows operations such as rotations and mirroring and integer re-sizing. As a result, this module is commonly used to provide memory saving for objects that rotate or have a consistent pattern around a centre. In these cases, it is possible to store only a small portion of the image or pattern— typically 45°—and reconstruct the remainder of the graphic by using the eDMA translations.

3 Suggested panel sizes for different use cases

In this section, a number of different application use cases are considered and the MPC5645S configuration for each is suggested.

NOTE

Since the recommendations rely on typical requirements, it is possible that the experienced designer or expert software engineer may be able to extract a higher performance from the system than shown here.

3.1 How to interpret the calculations

All calculations are made using graphics that are of the same size as the panel. Although this is not a typical use case, it gives an insight into the capability of the system and the users can use this as a reference point for their own graphics. For example, if the calculation shows that a single 16 BPP graphic may be stored in OCRAM, then it will be possible to store the sum of the same surface area in multiple smaller graphics and graphics with smaller encoding size.

Consider the case where 2.5 16 BPP graphics can be fetched from SRAM. In this case, it would be possible to fetch 5 full-sized 8 BPP graphics or 5 16 BPP graphics where each is one half of the panel size.

Note that in all cases, the DCU3 can never use more than four layers simultaneously and therefore any calculation which supports more than this at 32 BPP indicates that any combination of graphics is possible for that panel size.

The tables shown in the following subsections contain a bandwidth calculation and a memory size calculation. For QuadSPI serial flash, the main limitation will be the memory bandwidth when for internal OCRAM, the lack of storage can be a greater limit than the memory bandwidth.

Each of the tables contains up to nine entries from the values described below:

- Width—the width of the panel chosen
- Height—the height of the panel chosen
- Nominal clock—the typical pixel clock frequency of a panel of this size
- 32 BPP OCRAM capacity—the maximum number of panel-sized 32 BPP layers that can be stored using 1 MB of OCRAM
- 32 BPP OCRAM % load—the fraction of memory bandwidth used if the maximum number of 32 BPP graphics are fetched from OCRAM to blend a single output pixel. In other words, the memory bandwidth that the DCU modules consume when fetching four layers from OCCRAM for one panel application (DCU3) and six layers for two panels applications (DCU3 + DCULite)
- 32 BPP QuadSPI load capacity – the maximum number of panel-sized 32 BPP layers that can be fetched from an external serial flash using the entire memory bandwidth
- 32 BPP SDRAM % load – the fraction of memory bandwidth used if the maximum number of 32 BPP graphics are fetched from SDRAM to blend a single output pixel. In other words, the memory bandwidth that the DCU modules consume when fetching four layers from OCCRAM for one panel application (DCU3) and six layers for two panels applications (DCU3 + DCULite)

- 16 BPP OCRAM capacity—the maximum number of panel-sized 32 BPP layers that can be stored using 1 MB of OCRAM
- 16 BPP OCRAM % load—the fraction of memory bandwidth used if the maximum number of 16 BPP graphics are fetched from OCRAM to blend a single output pixel. In other words, the memory bandwidth that the DCU modules consume when fetching four layers from OCCRAM for one panel application (DCU3) and six layers for two panels applications (DCU3 + DCULite)
- 16 BPP QuadSPI capacity— the maximum number of panel-sized 16 BPP layers that can be fetched from an external serial flash using the entire memory bandwidth
- 16 BPP SDRAM % load—the fraction of memory bandwidth used if the maximum number of 16 BPP graphics are fetched from SDRAM to blend a single output pixel. In other words, the memory bandwidth that the DCU modules consume when fetching four layers from OCCRAM for one panel application (DCU3) and six layers for two panels applications (DCU3 + DCULite)

An entry of "-" in any table means that the value is unobtainable by the MPC5645S. Recommended screen sizes are highlighted.

Note that in all cases, the peak bandwidth of the memory is considered as 100% usage. In practice, the average memory bandwidth is lower than this; however the panel does not consume data at a constant rate due to the horizontal and vertical porches. In addition, there are several buffers in the system, panel-sized graphics are rarely used, and the DCU performs a pre-emptive fetch; so in practical applications, the true usable bandwidth is very hard to predict. For these reasons, the usable bandwidth is always stated against peak performance. A user should note that it is unlikely that bandwidth above c. 90% should be considered achievable in most applications.

3.2 QuadSPI applications

The different packages provide support for one QuadSPI interface. For this use case assume that the two QuadSPI serial flash are used and run at 66 MHz at a single data rate access.

Width	Height	Nominal clock (MHz)	QuadSPI load capacity	
			32 BPP	16 BPP
320	240	5	3.3	6.6
480	272	9	1.8	3.7
640	480	25	-	1.3
800	480	33	-	1
800	600	40	-	-
1024	768	65	-	-

QuadSPI applications

From the table given above, it is clear that using only the QuadSPI interface for graphic load would be really restrictive. However it can be used to complement other memories for a panel size of 320 x 240 (QVGA) or above 480 x 272 using 16BPP graphics.

3.3 Single panel applications

The MPC5645S has the ability to use the DCU3 or the DCULite module in a single panel application, but in most cases, DCU3 is the obvious choice. This is because it is designed to support a total of 16 layers and can fetch up to four graphics when DCULite supports only a total of four layers and can fetch up to two graphics. These examples assume the use of DCU3.

3.3.1 LQFP applications (176 and 208 pins)

The LQFP packages do not provide support for SDRAM, so memory for application and graphics is limited to the OCRAM and a dual QuadSPI interface. For this use case, assume a platform clock of 125 MHz.

Width	Height	Nominal clock (MHz)	32 BPP		16 BPP	
			OCRAM max	OCRAM % load	OCRAM max	OCRAM % load
320	240	5	3.26	8	6.51	4
480	272	9	1.91	14.4	3.83	7.2
640	480	25	0.81	40	1.63	20
800	480	33	0.65	52.8	1.3	26.4
800	600	40	0.52	64	1.04	32
1024	768	65	0.32	-	0.64	52

LQFP applications

From the table given above, it is clear that panels above 480 x 272 (WQVGA) place an unreasonable demand on the storage capability of OCRAM (c. 1 layer) and the bandwidth capability of the serial flash (max 1 16 BPP graphic). A WQVGA panel can be considered to be supported well by this system since it allows storage of large 32 BPP graphics and multiple 16 BPP graphics in both OCRAM and serial flash.

3.3.2 BGA applications

The BGA package supports SDRAM for application and graphics and a dual QuadSPI interface. A large external DDR2 RAM can be used to store graphics and so in this case the capacity of storage is not a limitation. The load performance of the SDRAM is identical to the OCRAM.

Width	Height	Nominal clock (MHz)	SDRAM % load	
			32 BPP	16 BPP
320	240	5	8	4
480	272	9	14.4	7.2
640	480	25	40	20
800	480	33	52.8	26.4
800	600	40	64	32
1024	768	65	-	52

416-pin BGA applications

From the table given above, it is clear that panels up to 800 x 600 (SVGA) are supported in this system. In practice, the WVGA (800 x 480) is a more common form factor. A WVGA panel can be considered to be supported well by this system since the bandwidth of the SDRAM allows several graphics.

3.4 Dual panel applications

In these examples, assume that two identical panels are used. One is linked to the DCU3, and the other one to the DCULite. The maximum of graphics which can be fetched in the same time is six, with four for the DCU3 and two for the DCULite.These examples give an insight into the overall performance limits of the systems. It is important to notice that the DCULite module is not available for the LQFP 176-pin package.

NOTE

The memory bandwidth of each panel is independent. This means that each panel can consume up to 1 GB/s independently from the memory sources.

3.4.1 LQFP (208-pin) applications

The LQFP (208-pin) package does not provide support for SDRAM, so memory for application and graphics is limited to the OCRAM and the dual QuadSPI interface. For this use case, assume a platform clock of 125 MHz.

Width	Height	Nominal clock (MHz)	32 BPP		16 BPP	
			OCRAM max	OCRAM % load	OCRAM max	OCRAM % load
320	240	5	3.26	12	6.51	6
480	272	9	1.91	21.6	3.83	10.8
640	480	25	0.81	60	1.63	30
800	480	33	0.65	79.2	1.3	39.6
800	600	40	0.52	96	1.04	48
1024	768	65	0.32	-	0.64	78

208-pin LQFP applications:

From the table given above, it is clear that panels above 480 x 272 (WQVGA) place an unreasonable demand on the storage capability of OCRAM (c. 1 layer) and the bandwidth capability of the serial flash (max 1 16 BPP graphic). A WQVGA panel can be considered to be supported well by this system since it allows storage of large 32 BPP graphics and multiple 16 BPP graphics in both OCRAM and serial flash. However only two QVGA (320 x240) allow to use fully the capacity of the DCU and the DCULite by loading six graphics of 32 BPP in once.

3.4.2 BGA applications

The BGA package supports SDRAM for application and graphics and a dual QuadSPI interface. A large external DDR2 RAM can be used to store graphics and so in this case the capacity of storage is not a limitation. The load performances of the SDRAM are identical to the OCRAM.

Width	Height	Nominal clock (MHz)	SDRAM % load	
			32 BPP	16 BPP
320	240	5	12	6
480	272	9	21.6	10.2
640	480	52	60	30
800	480	33	79.2	39.6
800	600	40	96	48
1024	768	65	-	78

416-pin BGA applications

From the table given above, it is clear that panels up to 800 x 600 (SVGA) are supported in this system. A WVGA panel can be considered to be supported well by this system since the bandwidth of the SDRAM allows up to six 32 BPP graphics on each panel. Larger panels may be supported depending on the acceptable maximum loading of the external memory.

NOTE

The usability of the serial flash in this case is likely very restricted.

4 Conclusion

The MPC5645S platform comfortably supports panels of various sizes; however the memory capacity and bandwidth of the system impose upper limits on the practical size of these panels. Notice that the number presented in this document have been calculated for the worst cases, assuming the load of four or six 32BPP graphics with the size of the panel.

For the LQFP package, panels of no larger than WQVGA (480 x 272) are comfortably supported. For the BGA package, up to two SVGA (800 x 600) panels can be connected assuming a suitable SDRAM memory is also connected.

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USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or +1-480-768-2130
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Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
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www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
No. 118 Jianguo Road
Chaoyang District
Beijing 100022
China
+86 10 5879 8000
support.asia@freescale.com

Document Number: AN4865
Rev. 0, 01/2014