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Application Note

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MPC5775K Hardware Design Guide

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Contents

1 Introduction

The MPC5775K is a 32-bit heterogeneous multi-core microcontroller primarily intended for use in computationally intensive automotive safety and chassis applications. The device incorporates three Power Architecture® cores arranged as two independent e200z7260 for general computation and an e200z420 core with an e200z419 checker core running in delayed lockstep configuration for safety-critical and housekeeping tasks. The MPC5775K also integrates high-performance analog and signal processing features designed to support sophisticated automotive RADAR applications.

This application note illustrates the MPC5775K power supply options and details the external circuitry required for power supplies, oscillator connections, and supply decoupling pins. It also discusses configuration options for clock, reset, ADC modules and the RADAR analog front-end, as well as recommended debug and peripheral communication connections and other major external hardware required for the device.

The MPC5775K requires multiple external power supplies to operate. The main core internal logic requires a 1.25 V power supply. This can be supplied from an external source or alternatively provided by an internal DC-DC regulator that requires a dedicated supply. 3.3 V is required for the general purpose I/O, flash memory, analog front-end, external communications interfaces, and on-chip SAR analog to digital converter.

2 MPC5775K Package Options Overview

The MPC5775K is available in a single package type: A 356-ball MAPBGA package that is suited to development, debug and commercial production.

Table 1. MPC5775K package description

Package	Description
356 Map ball grid array (MAPBGA)	Full support for all device modules and features including JTAG and Nexus High Speed Aurora Trace debug interfaces.

The following table shows the physical dimensions of the packages. See the device data sheet for complete package dimensions and ball placement. Drawings are also available on the freescale.com, search for the case outline number shown in Table 2.

Table 2. Package sizes

Package	Physical Size	Case Outline Number	Pitch
356 MAPBGA	17 x 17 mm	98ASA00478D	0.8 mm

3 Power Supply

The MPC5775K microcontroller unit has a robust power management infrastructure that enables applications to select among various user modes and to monitor internal voltages for high- and low-voltage conditions. The monitoring capability is also used to ensure supply voltages and internal voltages are within the required operating ranges before the microcontroller can exit the reset state and enter operation.

The microcontroller offers a DC-DC voltage regulator function as part of the power management controller (PMC) module. This regulator can be used to supply the digital low voltage required for the internal logic and other low voltage supplies. The device can be configured to use either this internal regulation mode or an external 1.25 V regulated power supply to provide the core voltage. The standard configuration utilizes the internal DC-DC voltage regulator, with the following external supply voltages:

- 3.3 V for main general purpose I/O, SAR ADC supply and reference, PDI I/O, JTAG debug interface, flash memory supply voltage and external communication interfaces (Ethernet, FlexRay, etc.)
- 3.0 - 5.5 V (required) for the internal DC-DC voltage regulator which supplies 1.25 V for the internal logic, PLL circuits and low voltage/Nexus Aurora I/O.

Detailed information on the power management configurations can be found in the Power Management Controller section.

3.1 Power Supply Signals and Decoupling

Table 3 lists all MCU power domains with corresponding pin names. Depending on the power management configuration, some of the supplies below may not require an external power source. The power management configuration is detailed in Power Management Controller.

Table 3. MCU power supply pins

Domain name	Supply Voltage	Description
VDD_LV_CORE	1.25 V	Low-voltage supply for core logic
VDD_HV_IOx	3.3 V	High-voltage supply for general purpose I/O
VDD_HV_RAW	3.3 V	High-voltage, high fidelity supply for analog front-end block
VDD_HV_DAC	3.3 V	High-voltage supply for DAC module in analog front-end
VDD_HV_ADC	3.3 V	Voltage supply for SAR ADC module
VDD_HV_ADCREF0/2	3.3 V	Voltage reference for SAR ADC 0/2
VDD_HV_ADCREF1/3	3.3 V	Voltage reference for SAR ADC 1/3
VDD_HV_FLA	3.3 V	Voltage supply for flash memory
VDD_HV_IO_PDI	3.3 V or 1.8 V	PDI I/O voltage supply
VDD_HV_PMU	3.3 V	Voltage supply for power management unit
VDD_HV_REG3V8	3.0 V - 5.5 V[1]	Voltage supply for internal DC-DC voltage regulator
VDD_LV_LFASTPLL[2]	1.25 V	Voltage supply for DigiRF (SIPI/LFAST) PLL
VDD_LV_IO_AURORA[3]	1.25 V	Voltage supply for Nexus Aurora I/O
VDD_LV_PLL0	1.25 V	Voltage supply for system PLL
VDD_LV_IO	1.25 V	Low voltage supply for general purpose I/O

1. Internal regulation mode. When using external regulation mode, this domain can be tied to VDD_HV_PMU
2. The naming convention VDD_LV_LFASTPLL is equal to VDD_LV_DRFPLL
3. VDD_LV_IO_AURORA must be connected to the same voltage supply as VDD_LV_CORE. The supplies must be brought up simultaneously.

Some of the supplies can be powered with different supply voltages. The parallel digital interface (PDI) communications interface can operate at 3.3 V or alternatively at 1.8 V for input only mode. The internal voltage regulator supply, VDD_HV_PMU, can be supplied with a voltage between 3.0 V and 5.5 V. See the device data sheet for specific information and to learn what voltage ranges can be safely connected to the power pins.

Table 4 shows all power domains and the suggested decoupling and/or filter capacitors for their corresponding pins. These values are provided as a guideline and will vary depending on the application and capability of the power supplies used.

The decoupling capacitors must be placed as close as possible to the MCU supply pins, with priority given to those with the smallest capacitance value..

Table 4. Supply pin decoupling capacitors

Domain name	Supply Voltage	Minimum Decoupling Capacitors
VDD _LV_CORE	1.25 V	0.1 µF x 16, 4.7 µF x 4, 10 µF x 2 (40 µF total)[1]
VDD_HV_IOx	3.3 V	2 x 0.1 µF for each VDD_HV_IO supply[2]
VDD_HV_RAW	3.3 V	0.1 µF, 1 µF
VDD_HV_DAC	3.3 V	1000 pF, 0.1 µF, 1 µF

Table continues on the next page...

Table 4. Supply pin decoupling capacitors (continued)

Domain name	Supply Voltage	Minimum Decoupling Capacitors
VDD_HV_ADC	3.3 V	0.1 µF, 1 µF
VDD_HV_ADCREF0/2	3.3 V	0.01 µF, 1 µF
VDD_HV_ADCREF1/3	3.3 V	0.01 µF, 1 µF
VDD_HV_FLA	3.3 V	0.1 µF, 1000 pF
VDD_HV_IO_PDI	1.8 V or 3.3 V	3 x 0.1 µF for each VDD_HV_IO_PDI supply
VDD_HV_PMU	3.3 V	100 nF, 4.7 µF
VDD_HV_REG3V8	3.0 V - 5.5 V	1 µF Ceramic[3]
VDD_LV_DRFPLL	1.25 V	1000 pF, 0.1 µF, 1 µF, 0.01 µF
VDD_LV_IO_AURORA	1.25 V	0.1 µF, 1 µF
VDD_LV_PLL0	1.25 V	1000 pF, 0.1 µF, 1µF, 0.01 µF
VDD_LV_IO	1.25 V	0.1 µF x 2

1. When using internal regulation mode, assure that the total capacitance (accounting for temperature variations) never falls below 40 µF
2. External capacitors for the IO pins are dependent on the application.
3. 100 nF connected in parallel in case of non-ceramic capacitor

The device has several pins for the connection of external decoupling capacitors for the analog front-end. Details of these can be found in RADAR Analog Front End

3.2 Decoupling Capacitors Layout Priority

When trade-offs must be made in the schematic layout, it is important to ensure that the highest priority supplies have decoupling capacitors placed as closely as possible to the MCU. The list below outlines the recommended order of the supplies from highest to lowest priority in terms of their importance for decoupling.

1. VDD_HV_RAW & VDD_HV_DAC
2. VDD_HV_ADCREF0/2 & VDD_HV_ADCREF1/3
3. VDD_HV_ADC
4. VDD_LV_PLL0
5. VDD_LV_CORE
6. VDD_LV_AURORA
7. VDD_HV_PMU
8. VDD_HV_FLA
9. VDD_LV_LFASTPLL
10. VDD_LV_IO
11. VDD_HV_IO
12. VDD_HV_IO_PDI

Highest priority is given to the high-fidelity analog front end supplies VDD_HV_RAW and VDD_HV_DAC, as their decoupling must be prioritized to maintain analog signal integrity. VDD_HV_ADRREF0, VDD_HV_ADREF1, and VDD_HV_ADC is the SAR analog-to-digital converters reference and power supply decoupling. Clean supplies are vital to ensure that the highest accuracy is achieved with the ADCs. The supply for the system PLL is prioritized as this helps to ensure reliable and stable operation from the internal PLL circuit.

Medium priority is given to VDD_LV_CORE, VDD_LV_DRFPLL, VDD_LV_AURORA, VDD_HV_PMU, and VDD_HV_FLA. VDD_LV_CORE is the main supply for the on-chip digital logic and this is prioritized as it affects the largest amount of logic on the device. VDD_LV_AURORA powers the high speed Nexus Aurora pins and noise on this domain would affect the quality of the output. VDD_HV_PMU is the power management unit supply and VDD_HV_FLA is the input supply for the flash memory. A good supply to the flash memory ensures reliable flash programming and erasing.

VDD_LV_DRFPLL powers the PLL for the LFAST/SIPI communication interface. VDD_HV_IO, VDD_LV_IO, VDD_IO_PDI drive GPIO and other external communication interfaces. Although it is still important that these supplies have a clean power signal, the hardware they power is less affected by noise and they are considered of lower priority.

3.3 Power Management Controller

The MPC5775K has a dedicated module for configuration and monitoring of power supplies, enable signals, internal component trimming, and power-on reset generation. The Power Management Controller (PMC) consists of an analog block and a supporting digital interface that provides control over the analog components. The Power Management Controller chapter in the device reference manual explores the digital block in some depth.

NOTE

This document will focus on the external hardware and connections concerned with the PMC analog block.

3.3.1 Core Supply Options

The MPC5775K offers two options for supplying the 1.25 V used by the core and other low-voltage digital power domains.

- Internal voltage regulation mode, using the integrated DC-DC voltage regulator (VREG)
- External voltage regulation mode using an externally regulated 1.25 V supply

The input pin VREG_SEL allows selection between internal and external regulation modes, the function of this input is described in the table below.

Table 5. VREG_SEL input signal

Input Level	Core Supply Mode
High (3.3V)	Internal regulation mode
Low (GND)	External regulation mode

The Power Management Controller (PMC) has an internal voltage regulator function that uses a switched-mode power supply (SMPS) circuit to supply the 1.25 V required by the internal core logic, (VDD_LV_CORE) and the other low-voltage digital supplies (VDD_LV_AURORA, VDD_LV_PLL0 and VDD_LV_IO). The regulator requires the support of external circuitry detailed in SMPS External Component Configuration. This configuration is an asynchronous buck regulator with nominal switching frequency of 1 MHz. The switching frequency is modulated to improve the EMI performance of the device, further information on this feature can be found in the PMC chapter in the device reference manual.

VREG_SEL is part of a collection of I/O signals that relate to the VREG operation mode. The other pins are mentioned in the table below.

Table 6. PMC Voltage regulator signals

Signal Name	Direction	VREG Enabled (Internal Mode)	VREG Disabled (External Mode)
VREG_POR_B	Input	External power-on reset. If not required, can be left floating or connected to 3.3 V supply. Pulled up internally to 3.3 V	Power-on reset(POR) input. Used by external circuitry to trigger a POR or hold device in reset state
VREG_ISENS	Input	Current sense input to internal regulator	Not used. Connect to VDD_LV_CORE
VREG_SWP	Output	Output from internal VREG. Controls the gate of the external switching PMOS transistor [1]	Not used, can be left floating

1. If the connection between VREG_SWP and the PMOS gate is broken, the switch may fully turn on. For added protection against this risk, a 100 Kilo Ohm resistor can be connected between VDD_HV_REG3V8 and the PMOS gate.

3.3.2 Internal Voltage Regulator Supply Mode

The standard device configuration uses the internal DC-DC voltage regulator to supply the core voltage and other low-voltage digital supplies. Figure 1 shows all the power supply connections required when operating in internal voltage regulation mode and provides guidelines on how to structure the power nets. Values for the decoupling capacitors shown in the diagram is found in Table 4.

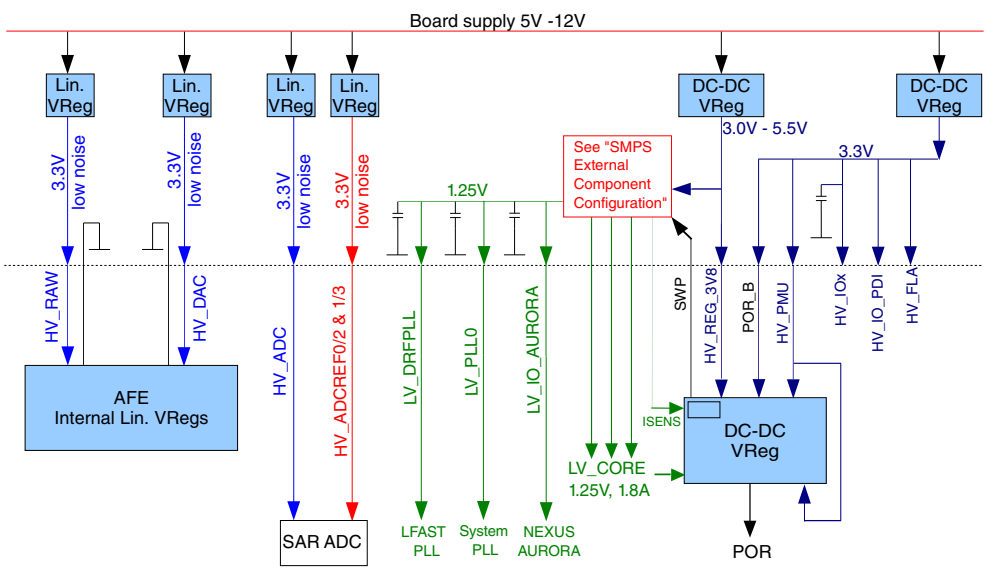

Figure 1. Supply connections

The internal regulator requires a dedicated 3.0 V - 5.5 V supply alongside the 3.3 V PMC supply to generate the 1.25 V digital low voltage. The support of an external PMOS switch circuit is also required, details are given in SMPS External Component Configuration. The analog front-end (AFE) requires high-fidelity supplies and careful decoupling to support its sensitive analog functionality, covered in RADAR Analog Front End.

Internal regulation mode is enabled by driving the VREG_SEL input high and has the following attributes.

- The PMC internal power-on-reset (POR) and low-voltage/high-voltage detect (LVD/HVD) circuits are enabled by default.

- The internal POR will keep the device in reset until all the monitored supplies have reached their minimum operation threshold.
- The internal POR function means that the external POR pin VREG_POR_B is not needed. As such, it is internally pulled up to the PMC supply voltage. It can be left floating or alternatively connected to 3.3 V.
- VREG_POR_B remains active in internal regulation mode, even though POR is managed internally. If pulled low it will cause a power-on reset regardless of voltage regulation mode.[1]
- The internal LVD/HVD circuits are enabled by default to ensure the expected boot-up sequence occurs. More information on the LVDs/HVDs is available in Low-Voltage (LVD) and High-Voltage Detection (HVD).

3.3.3 SMPS External Component Configuration

When operating in internal voltage regulation mode, an SMPS circuit is required along with the support of external components in order to minimize noise and maintain a stable supply to guarantee device performance. Special care must be taken so that the switched regulator does not introduce noise into high-fidelity analog components. The external component layout is shown in Figure 2.

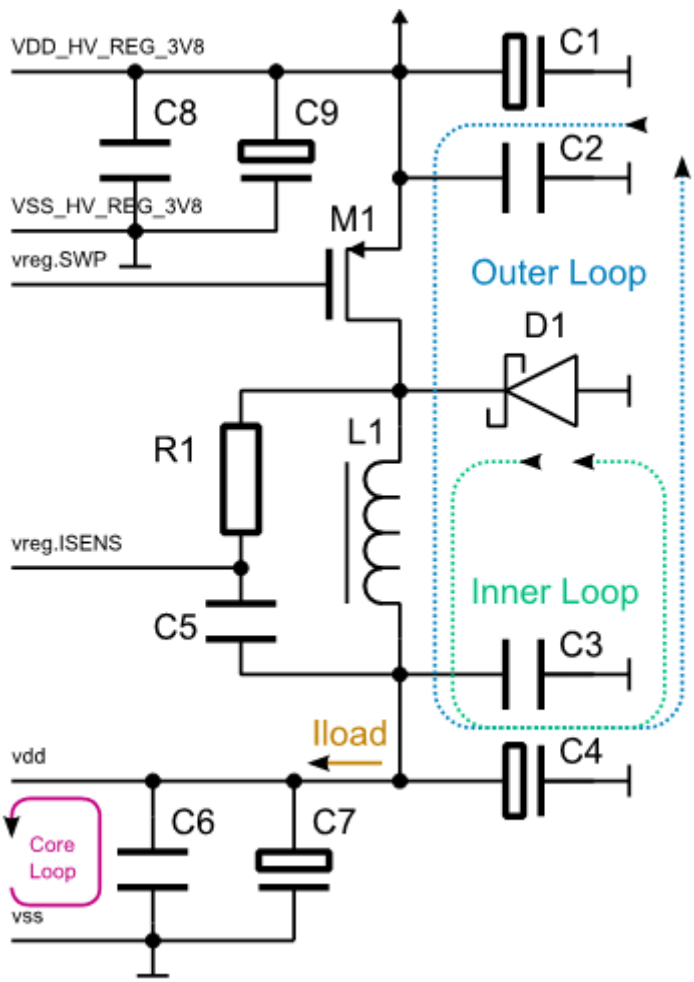

Figure 2. SMPS external components layout

1. VREG_POR_B can be used in internal regulation mode to ensure that the POR sequence is only started when main power supply reaches a stable regulation point. This can assist in cases where the power supply reaches the minimum LVD threshold but then drops below the threshold again when loaded, before reaching a stable regulation point.

Table 7 provides recommended values for the external components.

Table 7. External component values

Component Label	Recommended Value
M1	SI3443, 2SQ2315
L1	2.2 µH 3A <100 mΩ series resistance (E.g. Bourns SRU8043-2R2Y)
D1	SS8P3L 8A Schottcky diode
R1	240 kΩ
C1	10 µF ceramic
C2	100 nF ceramic
C3	100 nF ceramic (place close to inductor)
C4	10 µF ceramic (place close to inductor)
C5	100 pF ceramic
C6	4x 100 nF + 4x 10 nF ceramic (place close to MCU supply pins)
C7	4x 10 µF ceramic (place close to MCU supply pins)[1]
C8	100 nF ceramic (place close to MCU supply pins)
C9	1 µF ceramic (place close to MCU supply pins)

1. These are the same capacitors as those listed for VDD_LV_CORE in Table 2

For optimum electro-magnetic interference(EMI) performance, it is critical that the inner and outer loops shown in Figure 2 overlap on the PCB and are made as short as possible. It is highly recommended to have a section of the PCB ground plane dedicated to making a good connection between the grounds of C1/C2 and C3/C4. This measure will help to ensure that the loops are made as short as possible.

The role of C1/C2 is to guarantee a low input impedance to the buck converter. In a similar manner, C3/C4 make the impedance low at the buck converter output. This measure helps reduce the high frequency content of the current passing through the highlighted branch 'Iload', making it less critical that the buck converter components be placed close to the VDD/VSS pins of the MCU. However, it is important that capacitors C6 and C7 are placed as closely as possible to the VDD/VSS pins of the MCU, as they guarantee the low impedance of the core MCU supply and also help to reduce the high frequency content of the 'Iload' path.

The gate-driver circuitry also forms important current loops that must be minimized (not shown in Figure 2). For that purpose, C8/C9 must be placed as close as possible to the gate-driver supply pins. The ground connections for C8/C9 must be made as short as possible to C1/C2. When the PMOS switch is turned on, the high-frequency current that charges the gate comes from C1/C2, passing through the PMOS gate into the gate-driver pin. That current is carried to the gate-driver VSS pin returning to C1/C2. This current loop must be made as small as possible.

Conversely, when the PMOS switch is turned off, high-frequency currents enter in the PMOS gate coming from the gate-driver pin and flow into C1/C2, returning through the ground into C8/C9 and then into the gate-driver supply pin. Minimizing this second loop area is as critical as the first.

To shield nearby nets from the gate-driver generated noise, it is also recommended that the gate-driver supply pins are used to shield the VREG_SWP net until it reaches the PMOS switch. Nets on other PCB layer should avoid running parallel to this net.

The figure below is a circuit schematic showing an example SMPS circuit derived from the guidelines. For best performance, use the component values recommended in Table 7.

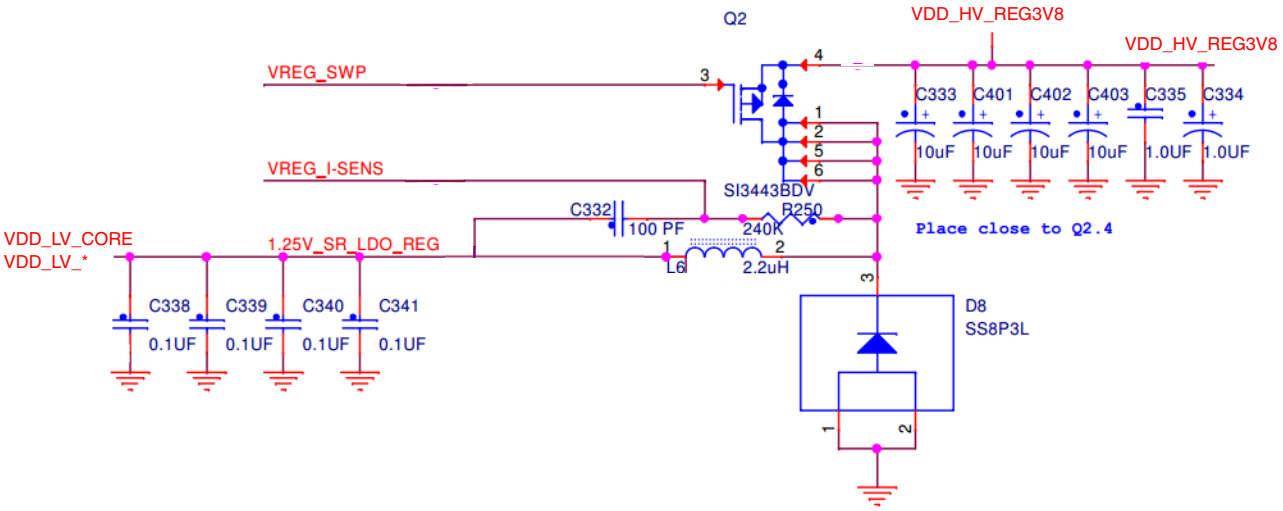

Figure 3. Example schematic of SMPS external components

3.3.4 External Supply Mode

If there is a stable 1.25 V regulated supply available to provide the digital low voltage, the internal voltage regulator can be disabled. This also negates the need for the external SMPS circuit. An overview of the power connections required for such a configuration is shown in Figure 4

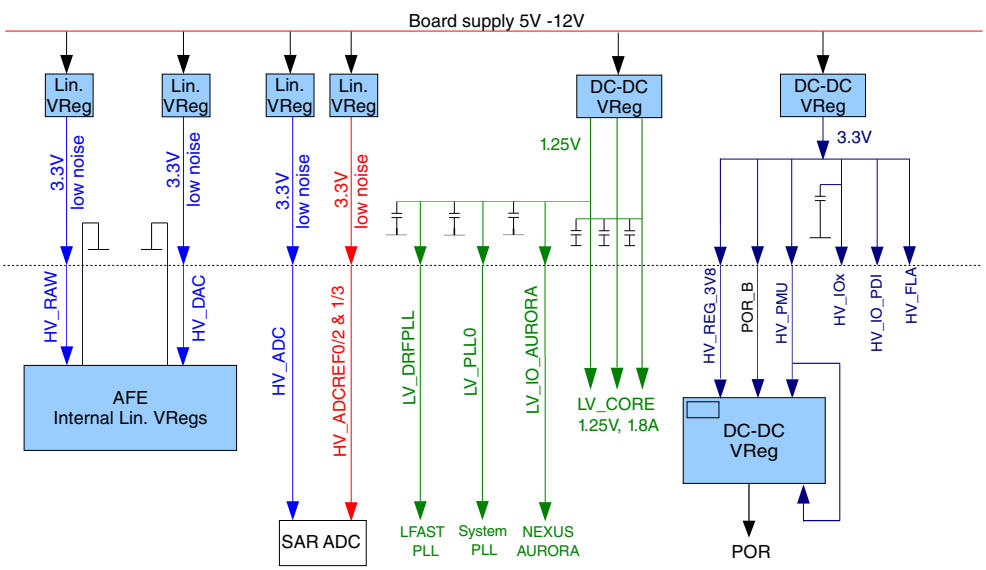

Figure 4. Supply connections

This mode of operation can be selected by driving the VREG_SEL pin low. This disables the internal:

- Voltage regulator (VREG)

- VDD_LV POR function (can be enabled by software)
- VDD_LV LVD/HVD circuits (can be enabled by software)

When internal regulation is disabled, the signals VREG_ISENS and VREG_SWP are not needed as they are for feedback and control of the SMPS circuitry. VREG_ISENS should be connected to VDD_LV_CORE and VREG_SWP connected to VDD_HV_PMU.

In external regulation mode, the supply for the internal voltage regulator, VDD_HV_REG3V8, can be connected to the same supply voltage as VDD_HV_PMU.

VDD_LV POR and LVD/HVD is the responsibility of the external regulation circuit. The device must be kept in reset ($\overline{\text{VREG\_POR\_B}}$ driven low) during power-up until all supplies have reached their minimum operating threshold and also during operation if any of the supplies move outside the specified range, as defined in the device data sheet. To achieve this, external LVD/HVD circuits are needed to monitor the supplies. After power-up, the internal LVDs/HVDs can be enabled by software to act as a second tier of detection and provide power supply information to the software.

3.4 Supply Monitoring

The MPC5775K has the capability to monitor selected supply voltages internally. This section concerns only the internal monitoring functions for POR and LVD/HVD, external POR and LVD/HVD circuit behavior will vary and should be designed using the device data sheet as reference. From this point, it is assumed that internal regulation mode is being used unless where explicitly stated. In external regulation mode, the internal POR and LVD/HVD are disabled by default but can be enabled by software after power-up.

The function of the power-on reset (POR) and low-voltage detect (LVD) circuits is to hold the device in reset as long as the supply voltages to the LVD circuits are below the minimum operating voltage. The device is held in reset until the point at which the supplies cross the lower threshold and the POR and LVDs are released.

3.4.1 Behavior of LVD / HVD

The internal LVD and HVD circuits monitor when the voltage on the corresponding supply is below or above defined values and either assert a reset or an interrupt. The LVDs/HVDs also support hysteresis for the falling and rising trip points.

Although there is an option to disable the LVDs and HVDs following reset, they are capable of being used in a ‘monitor’ only mode and also capable of generating a safe/interrupt event. The LVDs/HVDs can also be configured after device initialization to prevent reset when a supply crosses the LVD threshold, providing a higher voltage range. An application must then verify that the device remains in the functional range.

NOTE

The LVDs that form the power-on reset functionality, monitoring VDD_LV_CORE and VDD_HV_PMU, cannot be disabled. These modules are used during power-up phase and must ensure that an absolute lowest threshold of operation is never crossed. This is not a guarantee that the device will function down to this level. It is rather a guarantee that the device will recover if this level is crossed.

3.4.2 Low-Voltage (LVD) and High-Voltage Detection (HVD)

The internal LVD circuits monitor when the voltage on the corresponding supply is below defined values and either assert a reset or an interrupt, while the HVD circuits monitor to ensure a supply does not exceed an upper voltage limit. The LVDs/HVDs also support hysteresis in the falling and rising trip points.

- All LVDs and HVDs are capable of generating either a reset or an interrupt based on configuration, with the exception of two POR threshold monitors[2] :

    - LVD monitoring the internal core voltage (VDD_LV_CORE) always generates a reset when triggered.
    - LVD monitoring the PMC voltage supply input (VDD_HV_PMU) always generates a reset when triggered.
- All LVDs and HVDs configured for reset generation cause functional or destructive reset. Reset is not exited until all destructive reset conditions are cleared.
- The appropriate bits in the PMC status registers are set by LVD and HVD events.
- LVD and HVD control is protected by the SoC-wide register protection scheme. Therefore, it is configurable as long as the scheme is followed.
- There are user option bits available to allow degrading of “configurable” LVDs/HVDs from destructive down to functional reset. This is a write once mechanism managed by SSCM during device initialization.
- When the LVD or the HVD is enabled for destructive reset generation, then when a trigger event is detected, the external RESET_B pin is driven low.

Please refer to the device data sheet for LVD and HVD characteristics.

3.4.3 Power-on Reset

The power management controller (PMC) controls the internal power-on reset (POR) signal for the MCU. POR is the combination of all internal POR signals from the analog PMC block. When the critical power supplies are below minimum levels(internal regulation mode) or the VREG_POR_B pin is driven low, the MCU is held in the POWERUP phase of the reset state machine, POR asserted, until the power supplies have reached their specified levels. When the required voltage levels have been reached, POR is deasserted and is input to the reset generation module (MC_RGM) which propagates the device through the next steps of the boot process.

The PMC has internal POR low voltage detect(LVD) circuits to detect the minimum critical power supply voltages required to operate the internal voltage regulator, including hysteresis. It monitors:

- The voltage on the 1.25 V supply input, VDD_LV_CORE
- The 3.3 V signal used internally by the PMC, VDD_HV_PMU

Once both these supply voltages are above the threshold the internal POR signal will deassert. See Device Reset Configuration and the Reset chapter in the reference manual for VREG_POR_B and RESET_B pin functionality.

3.5 Power Sequence

The device is considered to be in a power sequence (POWER-UP state) when the device is either not supplied or is partially supplied. An internal power-on reset (POR) signal is used to identify POWER-UP state. This signal is released on exit of the power sequence. The power-on reset signal is a combination of LVD monitoring of the VDD_LV_CORE and VDD_HV_PMU supplies. Exit from the next phase, PHASE0, depends on the release of the secondary LVD/HVD circuits, which monitor:

- VDD_LV_PLL0
- VDD_HV_IO
- VDD_HV_FLA
- VDD_HV_ADC

Once they have reached the minimum operating threshold the device will exit reset. For more information on phases of the reset process, please refer to the Reset chapter in the device reference manual.

The actual threshold use for each internal LVD depends on the configuration of the device. This is configurable by hardware (flash option bits content) or by software (LVD event configuration through PMC register interface). Once the power-on signal has been asserted, the device configuration is reset to default power-up configuration. During the initialization phase,

2. As mentioned previously, the internal POR management is disabled by default when external regulation mode is selected. They cannot be disabled when operating in internal VREG mode.

the device defaults to a pre-determined state for each of the LVDs, HVDs, and the internal regulators. As the flash memory becomes available, the differential read process allows the trimmed data to be available for trimming the internal LVDs, HVDs, and regulators.

3.5.1 Power-up Sequence

In this section, the assumption is made that all supplies are low when entering the power-up sequence. Brown-out and power down sequences are specified in following sections.

There are simple power sequencing rules to follow in order to correctly power-up the device:

- The system PLL supply (VDD_LV_PLL0) and the core supply (VDD_LV_CORE) must be powered simultaneously. It is recommended to connect them to the same voltage supply.
- The high-voltage I/O supply (VDD_HV_IO) and the Power Management Unit supply (VDD_HV_PMU) must be powered simultaneously or VDD_HV_IO ramped before VDD_HV_PMU such that the two supplies always maintain less than 100 mV difference during the power ramp. They can be connected to the same voltage supply.
- The SD ADCs must be powered before a signal is applied to their inputs, to ensure protection of the input channels from overdrive signal levels. To do this, ramp VDD_HV_RAW supply before applying input to the SD ADCs.

All power supplies should ramp at slew rates within the ranges recommended in the device data sheet.

3.5.2 Power-down Sequence

If the threshold of the configurable monitor LVDs is crossed and they are configured to generate a destructive reset, the device re-enters the PHASE0 phase. The power-down sequence is started and the device enters the POWER-UP state as soon as the threshold of one of the POR LVDs (monitoring VDD_LV_CORE and VDD_HV_PMU) is crossed. The device supplies may then proceed to drop down to ground either through device leakage or external pull-down.

3.5.3 Brown-out Management

During brown-out, the device re-enters the POWER-UP phase as soon as the threshold of either POR VDD 1.2 V or APOR is crossed.

4 Clock Configuration

The MPC5775K system reference clock can be sourced in two ways: using the internal RC oscillator (IRCOSC) or connecting an external oscillator (XOSC). To use XOSC, an external 40 MHz crystal or oscillator must be connected through the XTAL and EXTAL pins. Information on how to do this can be found in Connecting External Clock Sources. IRCOSC or XOSC is used as the clock source for the internal phase-locked loops (PLL) to generate the high frequency clocks for the cores and peripherals.

This structure provides five different clock domains that are available as the source for system and peripheral clocks:

- IRCOSC - 16 MHz internal reliable RC oscillator
- XOSC - 40 MHz oscillator (using external crystal (XTAL) or external oscillator in bypass (EXTAL))
- PLL0 - up to 266 MHz PLL
- PLL1 - up to 266 MHz frequency-modulated (FM) PLL
- SDPLL- 320 MHz[3] PLL for the Sigma-Delta ADC

3. Divided by 2 (160 MHz) if used for system and peripheral clocks

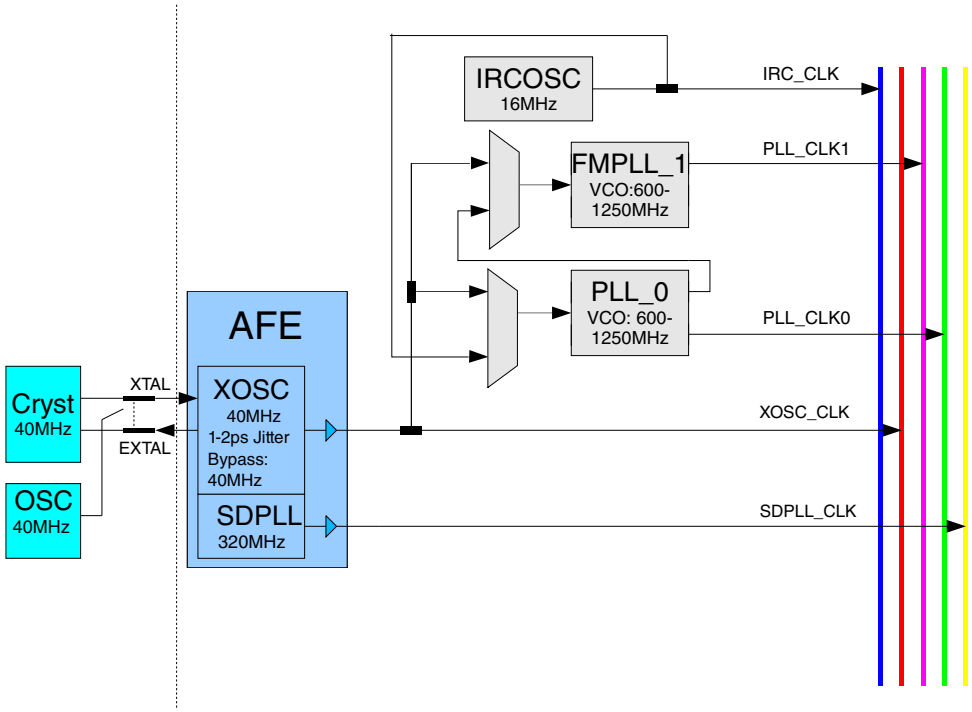

Figure 5. MPC5775K clock sources

During power up, the IRCOSC is the default clock for the system. In normal operation, software can then configure each of the system components to use one of the clock domains as the clock source. The dual PLL must be enabled by software and can provide separate system and peripheral clocks. PLL0 is the primary PLL driven by the reference clock and used to provide a clock to the device modules. PLL1 is a frequency-modulated PLL (FMPLL) driven by PLL0 and is used to provide the system clock. Alternatively, XOSC can be used to drive PLL1.

The most important aspects of an accurate clock source require that some care be taken in the layout and design of the circuitry around the crystal and PLL power supplies. Any noise in these circuits can affect the accuracy of the clock source to the PLL. The power supply for the PLL is taken from VDD_LV_PLL0. Noise on this supply can affect the accuracy and jitter performance of the PLLs. In order to minimize any potential noise, it is recommended that the additional capacitors recommended in Table 4 are fitted to the VDD_LV_PLL0 supply.

4.1 Connecting External Clock Sources

The MPC5775K features internal load capacitance on the XTAL and EXTAL pins for connecting external clock sources. This feature is intended to simplify the design and reduce the overall system cost by eliminating external components and reducing the PCB footprint. See the device data sheet for details on the internal capacitance values. PCB designers must take into account the parasitic capacitance levels on the signal lines connecting an external oscillator to the XTAL and EXTAL pins in order to avoid frequency deviation. Generally, for a crystal with load capacitance of 8 pF, a capacitance figure of 5-6 pF on the signal lines connected to both XTAL and EXTAL will result in good oscillator performance.

A diagram for the connection of an external 40 MHz crystal oscillator is shown in the figure below.

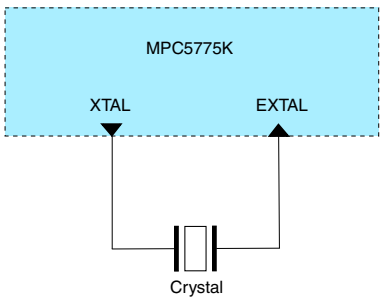

Figure 6. External oscillator connection

The oscillator should be placed as close as possible to the MCU. In order to minimize signal degradation, the circuitry should be placed entirely on only one PCB layer, avoiding unnecessary vias where possible. Do not allow any signals to cross the crystal connections to the device. Absolutely no high current or high speed signals should be run near any of the crystal components.

Other than the connections shown in the above schematics, no other connections should be made to the crystal or EXTAL and XTAL device pins. Do not use XTAL to drive any other circuitry than shown.

If an external clock is being used as clock reference to the MCU, then the XTAL pin should be left floating and the clock should be provided to EXTAL as shown in the figure below.

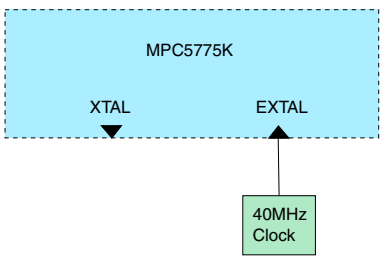

Figure 7. External clock connection (Bypass Mode)

Using either of these methods to connect an external clock makes it available as the XOSC internal clock source.

5 Device Reset Configuration

The MPC5775K MCU requires only very basic external reset circuitry. External circuitry for device configuration is not required. The device is configured during reset based on data in stored flash memory.

5.1 External Reset Signals

The MPC5775K device features two active-low external reset signals:

- Functional reset ($\overline{\text{RESET\_B}}$)
- Power-on reset ($\overline{\text{VREG\_POR\_B}}$)

$\overline{\text{RESET\_B}}$ is a bidirectional reset input/output that indicates if the device is active (high signal) or in reset. It is thus weak pull-up after the reset sequence has completed. A falling edge on this pin will trigger a functional reset to the Reset Generation Module(RGM). Forcing this pin low will keep the device in the last phase of the reset sequence (Phase3[Functional]).

In external voltage regulation mode, $\overline{\text{VREG\_POR\_B}}$ allows external supply circuits to signal to the MCU when power is available so the power-up sequence can begin. It should be forced high when the critical power supplies cross the LVD threshold.

In internal regulation mode, $\overline{\text{VREG\_POR\_B}}$ is not needed as the POR is managed within the PMC. It is internally pulled up to the PMC voltage, so it can be left floating. Alternatively, it can be connected to VDD_HV_PMU through a 4.7 Kilo Ohm pull-up resistor. Note that $\overline{\text{VREG\_POR\_B}}$ remains active in internal regulation mode. As such, if it is pulled low it will cause a power-on reset in the device.

Both of these pins operate on the 3.3 V power domain.

6 Recommended Debug Connectors And Connector Pin-out Definitions

The MPC5775K microcontroller implements the newly added (in the IEEE-ISTO 5001™-2011 version of the standard) high speed serial Nexus trace Auxiliary Port that uses the Xilinx™ Aurora physical interface. The Aurora interface allows the Nexus protocol information to be transmitted serially at a high date rate over one or more Aurora lanes. The Aurora protocol handles the encoding of the data and stripes the information across the number of lanes available on the device.

Table 8 shows the recommended connectors for different applications for the MPC57xxx Family.

Table 8. Recommended connectors

Connector style	Target system part number	Connector type
14-pin BERG JTAG only	3M 2514-6002UB	JTAG-only configuration
17-position (2 × 17, 34-pin) Samtec	Samtec ASP-137973-01	Serial Nexus configuration (supports up to 8 simplex lanes, less lanes are available if duplex support or High Speed Calibration LFAST interface support is required)

NOTE

Whichever connector is chosen, "keep-out" areas may be required by some tools. Consult the preferred tool vendor to determine any area that must remain clear around the debug connector. Some tool vendors may include an extension cable to minimize "keep-out" areas, but use of an extension will degrade the signal. In many cases, this degradation will be insignificant, but it depends on many factors including clock frequency and target board layout.

6.1 MPC5775K JTAG Connector

Table 9 shows the pinout of the recommended JTAG connector to support the MPC5775K device.

The recommended connector for the target system is Tyco part number 2514-6002UB.

Table 9. Recommended JTAG connector pinout

Description	Pin	Pin	Description
TDI	1	2	GND/VSS
TDO	3	4	GND/VSS
TCK	5[1]	6	GND/VSS
$\overline{\text{EVTI0}}$	7	8	$\overline{\text{VREG\_POR\_B}}$
$\overline{\text{RESET\_B}}$	9	10	TMS
VREF/VDD	11	12	GND/VSS
$\overline{\text{EVTO0}}$	13	14	JCOMP

1. If LBIST is enabled, an external pull resistor between 1 Kilo and 100 Kilo Ohm must be connected between TCK and either VDD/VSS to avoid LBIST failures

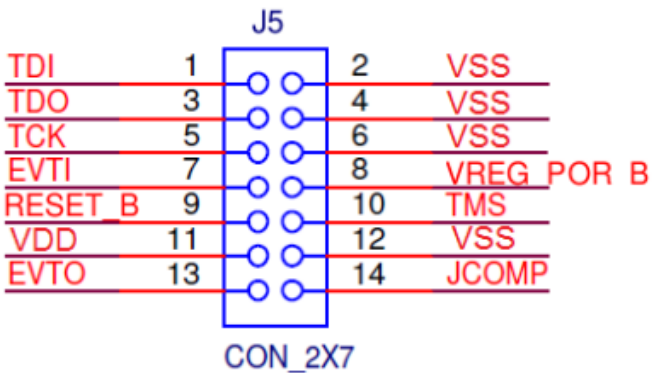

Figure 8. Diagram of the JTAG connector pinout

6.2 MPC5775K High-Speed Nexus Serial Trace Connector

For high speed Nexus Aurora trace applications, the Samtec™ ERF8 Series connector is recommended in the IEEE-ISTO 5001™-2011 standard. For the MPC57xx family, the 17 position (34 pins) connector is recommended. The part number of the Samtec connectors are shown in Table 10.

Table 10. Recommended high-speed serial trace connector part numbers

Connector	Part number (Samtec)	Style	Description
HS34	ASP-137973-01	Samtec ERF8 Series, 17 position by 2 row	Vertical mount for MCU module
HS34	ASP-177706-02	Samtec ERF8 Series, 17 position by 2 row	Right Angle mount for MCU module

The Samtec ERF8 series of connectors is intended for high speed applications requiring a minimum footprint size with a reliable, latching connection. The recommended connector has two rows of seventeen contacts each with a spacing of 0.8 mm. The connector provides isolation between the high-speed trace signals and the low-speed JTAG and control signals. It also provides ample ground connections to ensure signal integrity. If at all possible, the connector should be placed onto the target system with the even numbered pins nearest the edge of the printed circuit board.

Figure 9 is courtesy of Samtec U.S.A.

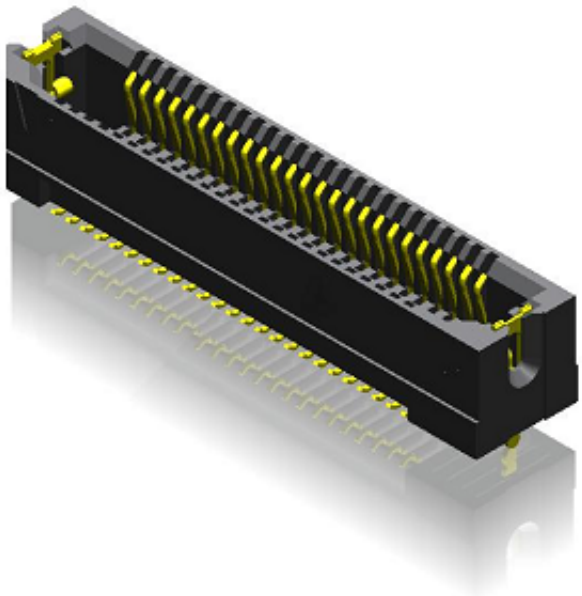

Figure 9. Recommended Nexus connector

Table 11 shows the recommended pinout for the Samtec connector.

Table 11. MPC5775K high-speed serial trace connector

Function	Pin No	Pin No	Function
TX0+	1	2	VREF
TX0-	3	4	TCK/TCKC/DRCLK
VSS	5	6	TMS/TMSC/TxDataP
TX1+	7	8	TDI/TxDataN
TX1-	9	10	TDO/RxDataP
VSS	11	12	JCOMP/RxDataN
TX2+	13	14	$\overline{\text{EVTI1}}$
TX2-	15	16	$\overline{\text{EVTI0}}$
VSS	17	18	$\overline{\text{EVTO0}}$
TX3+	19	20	VREG_POR_B
TX3-	21	22	RESET_B
VSS	23	24	VSS
(TX4+)[1]	25	26	CLK+
(TX4-)[1]	27	28	CLK-
VSS	29	30	VSS
(TX5+)[1]	31	32	$\overline{\text{EVTO1}}$/$\overline{\text{RDY}}$
(TX5-)[1]	33	34	N/C
VSS	GND	GND	VSS

1. Reserved for TXn signals, not currently used.

It is recommended that the "even" side of the connector be mounted closer to the edge of the printed circuit board to facilitate a direct connection to the tool.

6.3 Nexus Aurora Target System Requirements

The Nexus Aurora interface requires termination and AC coupling of the signals between the target system and the tool. The termination resistor for the Aurora clock is located inside the MCU. An external termination resistor is required. The transmit termination resistor must be implemented in the target system; however, it may be implemented internal to the FPGA of the tool.

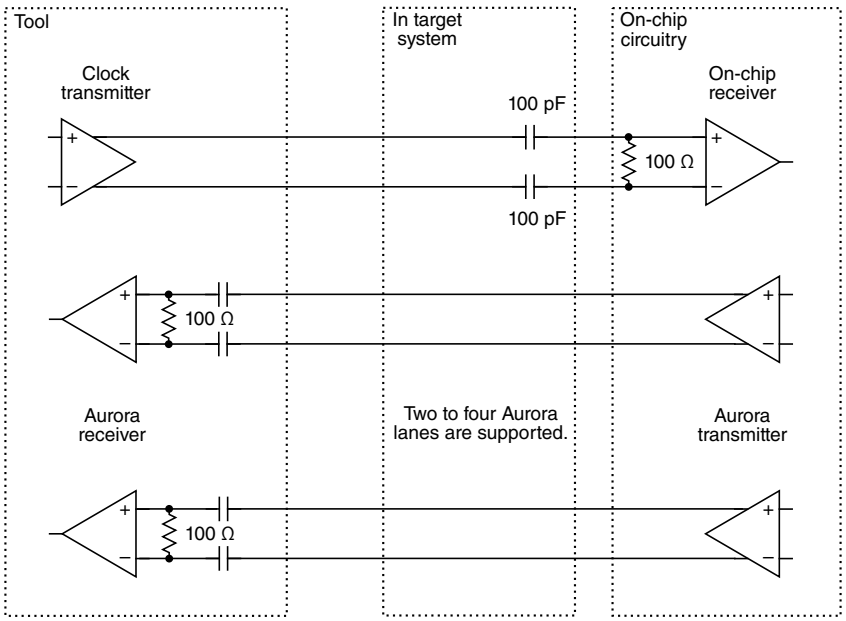

Figure 10. Nexus Aurora termination and coupling circuits

6.4 Minimum External Circuitry

Next to the connector, additional circuitry is required for the Nexus/JTAG debug circuitry. The MPC57xx devices include internal pull devices that ensure the pins remain in a safe state. However, if there is additional circuitry connected to the Nexus/JTAG pins, or long traces that could be affected by other signals (due to crosstalk from high-current or high-speed signals), a minimum number of external pull resistors can be added to ensure proper operation under all conditions.

Table 12. Optional external pullups/downs

Nexus/JTAG signal	Resistor/capacitor direction and value	Description
JCOMP	10 kΩ pulldown	Holds debug port in reset and prevents any debug commands from interfering with the normal operation of the MCU
$\overline{\text{VREG\_POR\_B}}$	4.7 kΩ pullup	The $\overline{\text{VREG\_POR\_B}}$ input should be driven from an open collector output; therefore, it requires a pull-up resistor for the MCU

Table continues on the next page...

Table 12. Optional external pullups/downs (continued)

Nexus/JTAG signal	Resistor/capacitor direction and value	Description
RESET_B	4.7 kΩ pullup	The RESET_B input should be driven from an open collector output; therefore, it requires a pull-up resistor for the MCU
Nexus CLKP & CLKN	100 pF on the signal lines	The LVDS Nexus clock signals require a capacitor for high speed functionality
EVTI	10 kΩ pullup	A pullup resistor prevents debug mode from being forced after reset if debug mode is enabled (JCOMP = high). It also prevents breakpoints from being forced if debug mode is enabled. **NOTE:** In almost all situations, a resistor is not required on this signal.

In addition to the pullup and pulldown resistors, some systems may want to use buffers between the JTAG connector inputs (JCOMP, TDI, TDO, TMS, EVTI, EVTO, VREG_POR_B, and RESET_B) and the MCU. This will prevent over-voltage conditions from causing damage to the MCU signals. Normal systems should not require this circuitry, but it is helpful in systems that can be exposed to improper connections that provide voltages that are outside the operating conditions of the MCU. A common circuit to use is the Texas Instruments™ SN74CBTLV38615. This device is a bus switch that implements a bidirectional interface between two terminals with less than 5 Ω of resistance. It should be powered by the same supply that powers the debug port. The device enable should be connected to ground for the interface to be enabled whenever the debug port on the MCU is powered. This circuit provides a high impedance to the tool when the debug port is powered off.

7 ADC Overview

The MPC5775K has two types of analog-to-digital converters (ADCs) that are designed for different applications:

- Four 12-bit Successive-Approximation-Register (SAR) ADCs with a configurable number of channels (up to 16 each) for voltage and temperature monitoring among other general applications
- Eight 12-bit Sigma-Delta (SD) ADC instances for rapid RADAR signal conversions

The SDADC is part of the RADAR analog front-end and is detailed in Sigma-Delta ADC. This chapter will focus on the SAR ADCs.

The SAR ADCs receive input from 25 multiplexed pins. Please refer to the Power Supply section for information on how to connect the ADC power and reference pins.

Each ADC instance receives input from a number of pins(channels), some of which are multiplexed to share with other ADC instances. This multiplexing, along with many other attributes of the ADCs, is controlled by configuration registers. Each ADC instance has an interface to the DMA controller for retrieval of converted data, the FCCU for error handling and the interrupt controller. Conversions can be triggered by hardware, software or externally:

- A Cross triggering unit (CTU) connected to each ADC allows automatic generation of ADC conversion requests on user selected conditions without CPU involvement.
- eTimer module provides the capability for external trigger injection to request a conversion.
- The CPU can request a conversion through software

7.1 SAR Analog Input Pin Multiplexing

There are 25 external analog pins that act as input channels for the SAR ADCs. They are multiplexed in order to facilitate sharing of the pins among the ADC instances.

There is an analog bypass bit "APC" in the Multiplexed Signal Configuration Register (MCSR) registers of the System Integration Unit (SIUL2) for the pins to disable the digital circuitry from the analog pins.

Table 13 gives the analog input pin assignment for the MPC5775K 356MBGA package.

Table 13. ADC pin muxing

ADC		Internal/ External	Signal source		Package Availability
ADC Instance	Channel No		Source	External Pin	
Shared external channels - ADC0/1					
ADC0	11	External	ADC0_AN[11]_ADC1_AN[11]	PAD[25]	All
ADC1	11				
ADC0	12	External	ADC0_AN[12]_ADC1_AN[12]	PAD[26]	All
ADC1	12				
ADC0	13	External	ADC0_AN[13]_ADC1_AN[13]	PAD[27]	All
ADC1	13				
ADC0	14	External	ADC0_AN[14]_ADC1_AN[14]	PAD[28]	All
ADC1	14				
ADC0 external channels					
ADC0	0	External	ADC0_AN[0]	PAD[23]	All
ADC0	1	External	ADC0_AN[1]	PAD[24]	All
ADC0	2	External	ADC0_AN[2]	PAD[33]	All
ADC0	3	External	ADC0_AN[3]	PAD[34]	All
ADC0	4	External	ADC0_AN[4]	PAD[70]	All
ADC0	5	External	ADC0_AN[5]	PAD[66]	All
ADC0	6	External	ADC0_AN[6]	PAD[71]	All
ADC0	7	External	ADC0_AN[7]	PAD[68]	All
ADC0	8	External	ADC0_AN[8]	PAD[69]	All
ADC0	9	—	not assigned	—	—
ADC0	10	Internal	Bandgap Reference PMC	—	—
ADC0	15	Internal	TSENS0	—	—
ADC1 Channels					
ADC1	0	External	ADC1_AN[0]	PAD[29]	All
ADC1	1	External	ADC1_AN[1]	PAD[30]	All
ADC1	2	External	ADC1_AN[2]	PAD[31]	All
ADC1	3	External	ADC1_AN[3]	PAD[32]	All
ADC1	9	—	not assigned	—	—
ADC1	10	Internal	Bandgap Reference PMC	—	—
ADC1	15	Internal	TSENS1	—	—
Shared external channels - ADC1/3					

Table continues on the next page...

Table 13. ADC pin muxing (continued)

ADC		Internal/ External	Signal source		Package Availability
ADC Instance	Channel No		Source	External Pin	
ADC1	4	External	ADC1_AN[4]_ADC3_AN[3]	PAD[75]	All
ADC3	3				
ADC1	5	External	ADC1_AN[5]_ADC3_AN[4]	PAD[64]	All
ADC3	4				
ADC1	6	External	ADC1_AN[6]_ADC3_AN[5]	PAD[76]	All
ADC3	5				
ADC1	7	External	ADC1_AN[7]_ADC3_AN[6]	PAD[73]	All
ADC3	6				
ADC1	8	External	ADC1_AN[8]_ADC3_AN[7]	PAD[74]	All
ADC3	7				
Shared external channels - ADC2/3					
ADC2	0	External	ADC2_AN[0]_ADC3_AN[0]	PAD[149]	All
ADC3	0				
ADC2	1	External	ADC2_AN[1]_ADC3_AN[1]	PAD[150]	All
ADC3	1				
ADC2	2	External	ADC2_AN2[]_ADC3_AN[2]	PAD[151]	All
ADC3	2				
ADC2 channels					
ADC2	5	Internal	Reserved for factory test only--SWG (for test only)	—	—
ADC2	10	Internal	Bandgap reference PMC	—	—
ADC3 channels					
ADC3	10	Internal	Bandgap Reference PMC	—	—
ADC3	11	Internal	Reserved for factory test only--Reserved for ATX	—	—
ADC3	12	Internal	Reserved for factory test only--Reserved for ATX	—	—
ADC3	13	Internal	Reserved for factory test only--Reserved for ATX	—	—
ADC3	14	Internal	Reserved for factory test only--Reserved for ATX	—	—
ADC0 and ADC1 Presampling					
ADC0	PRESx	Internal	VREFP_ADC0	—	—
ADC0	PRESx	Internal	VREFN_ADC0	—	—
ADC1	PRESx	Internal	VREFP_ADC1	—	—
ADC1	PRESx	Internal	VREFN_ADC1	—	—
ADC2 and ADC3 Presampling					
ADC2	PRESx	Internal	VREFP_ADC2	—	—
ADC2	PRESx	Internal	VREFN_ADC2	—	—
ADC3	PRESx	Internal	VREFP_ADC3	—	—
ADC3	PRESx	Internal	VREFN_ADC3	—	—

8 RADAR Analog Front End

The MPC5775K microcontroller integrates a number of high-performance digital and analog subsystems to support the implementation of next-generation RADAR-based advanced driver assistance systems. The analog front-end (AFE) module acts as an interface to the control registers for use with the integrated analog hard block, which includes:

- Eight continuous time sigma-delta ADCs (SDADC)
- Sigma-delta PLL (SDPLL) producing 320 MHz/160 MHz/80 MHz clocks for AFE components
- 12-bit high accuracy digital-to-analog converter (DAC)
- Low phase noise, low (1-2ps) jitter 40 MHz oscillator (XOSC)

A diagram of the AFE structure is shown in Figure 11. To support the high accuracy, high dynamic range analog functionality of the above features, careful configuration of power supplies and external circuitry is required to preserve signal integrity.

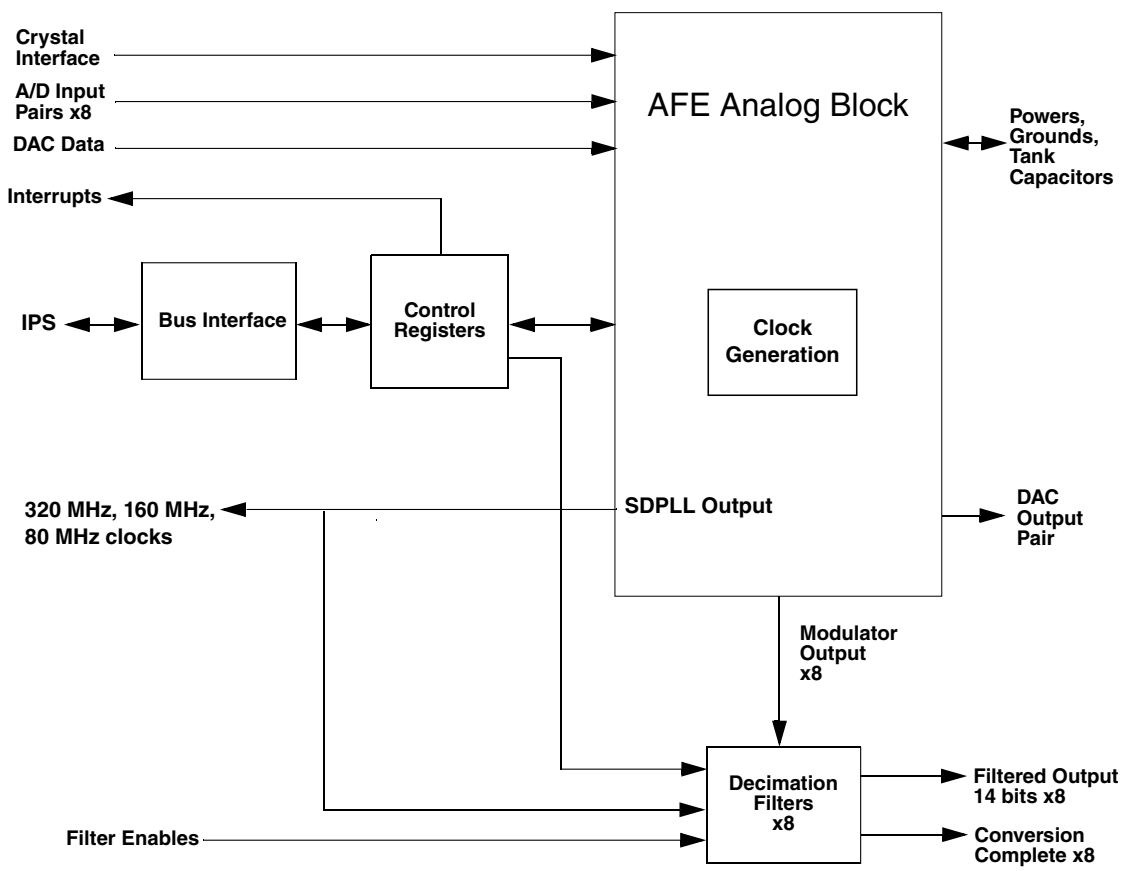

Figure 11. AFE Wrapper block diagram

8.1 AFE Power Supplies and External Connections

The AFE module requires multiple external connections. These are a mixture of high-fidelity analog power supplies, digital power supplies, ground connections, external capacitor connections and output signals for the various functions.

Table 14. AFE power supply connections

Name	Voltage Range	Domain	Function
VDD_HV_RAW	3.0 V - 3.6 V	3.3 V	Connects to 1.4 V regulators for: XOSC, SD PLL and SD ADC analog and digital.
VDD_HV_DAC	3.0 V - 3.6 V	3.3 V	Connects to DAC regulator

The table below shows the pins that the AFE exposes for the connection of external components. The components should be connected between the pin and ground.

Table 15. AFE external component connections

Pin Name	Function	Recommended
SD_R	External 0.1% trimming resistor for tuning the ADC resistor array.	40.2 Kilo Ohm +/-0.1%
VDD_LV_SDCLK	External bypass capacitor for LVDS analog 1.4 V VREG.	1.0 µF & 0.1 µF grounded to VSS_LV_SDCLK
VDD_LV_OSC	External bypass capacitor for XOSC analog 1.4 V VREG	1.0 µF & 0.1 µF grounded to VSS_LV_OSC
VDD_LV_SDPLL	External bypass capacitor for SD PLL analog 1.4 V VREG.	1.0 µF & 0.1 µF grounded to VSS_LV_SDPLL
VDD_LV_RADARREF	External bypass capacitor for 1.2 V from the VREF.	1.0 µF grounded to VSS_LV_SDADC
DAC_C	DAC connection to external cap for noise filtering.	10 µF connected to VDD_HV_DAC
SD_CM	ADC common mode external bypass capacitor	1.0 µF & 0.1 µF grounded to VSS_LV_SDADC
VDD_LV_SDADC	External bypass capacitor for ADC analog 1.4 V Vreg.	0.47 µF & 0.1 µF grounded to VSS_LV_SDADC
VDD_LV_RADARDIG	External bypass capacitor for ADC digital 1.4 V Vreg.	1.0 µF & 0.1 µF grounded to VSS_LV_RADARDIG
AFE_FILTER	Bypass capacitor for filtered analog supply	1.0 µF & 0.1 µF grounded to VSS_LV_SDADC
VDD_LV_DAC2V5	Bypass capacitor rampDAC 2.5 V VREG	1.0 µF & 0.1 µF grounded to VSS_HV_REGDAC

8.2 Sigma-Delta ADC

The eight time-continuous SD ADCs receive input as a differential pair. Each instance has two dedicated input pins.

Table 16. Sigma-Delta ADC external connections

Name	Pin (356MBGA)	Direction	Function
SD_0_ADCN	A2	I	ADC0 negative input
SD_1_ADCN	A3	I	ADC1 negative input
SD_2_ADCN	A4	I	ADC2 negative input
SD_3_ADCN	A5	I	ADC3 negative input
SD_4_ADCN	A6	I	ADC4 negative input
SD_5_ADCN	A7	I	ADC5 negative input
SD_6_ADCN	A8	I	ADC6 negative input
SD_7_ADCN	A9	I	ADC7 negative input
SD_0_ADCP	B2	I	ADC0 positive input
SD_1_ADCP	B3	I	ADC1 positive input
SD_2_ADCP	B4	I	ADC2 positive input
SD_3_ADCP	B5	I	ADC3 positive input
SD_4_ADCP	B6	I	ADC4 positive input
SD_5_ADCP	B7	I	ADC5 positive input
SD_6_ADCP	B8	I	ADC6 positive input
SD_7_ADCP	B9	I	ADC7 positive input

8.3 Digital-to-Analog Converter

The DAC is used to produce analog ramp signals for generation of RADAR waveforms.

Table 17. DAC signal description

Name	Pin (356MBGA)	Direction	Function
DAC_AN	D8	O	DAC negative output (current) Connected to external 300 Ohm resistor
DAC_AP	C8	O	DAC positive output (current) Connected to external 300 Ohm resistor

The resistors are required because the DAC output is a current source. Figure 12 shows how to connect the external resistors to the DAC output pins.

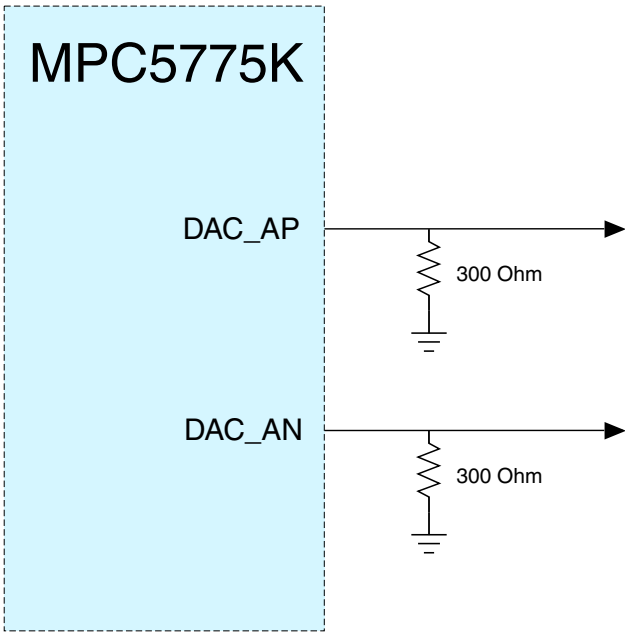

Figure 12. DAC Output Pin Connections

8.4 Sigma-Delta PLL

There are no external connections required for the Sigma-Delta PLL. Information on configuration can be found in the Analog Front End chapter in the device reference manual.

8.5 XOSC

Instructions on how to connect an external source to drive the XOSC clock can be found in Connecting External Clock Sources.

Table 18. XOSC external connections

Name	Pin (356MBGA)	Direction	Function
XOSC_EXTAL	E1	I	EXTAL analog input signal
XOSC_XTAL	D1	O	XTAL analog output signal

9 Example Communication Peripheral Connections

There are a wide range of peripheral pins available on the MCU. Many of these have fairly standard definitions for their use. This section provides example connections for some of the most commonly used communications peripherals, such as LIN, FlexCAN, FlexRay, and RS-232 communication interfaces.

9.1 Example RS232 Interface

The RS-232 (TIA/EIA-232-F) standard is a fairly common interface that is available on all computers. While this interface is disappearing, adapters are available to allow the use of RS-232 peripherals through other interfaces, such as USB. RS-232 was intended to be a very low-cost and low-performance interface. This interface was originally specified with signal voltages of +12 V and –12 V, typically. However, this has been lowered to a typical minimum voltage of +5 V and –5 V in recent years.

Figure 13 and Table 19 show the typical connections between the serial port of an MCU and the MAX3232-EP RS-232D transceiver from Texas Instruments http://www.ti.com/. The transceiver operates from either a 3.3 V or a 5 V supply and includes two charge pumps to generate the output voltages that are required. This device contains two transmit drivers and two receivers. The charge pumps require four external capacitors.

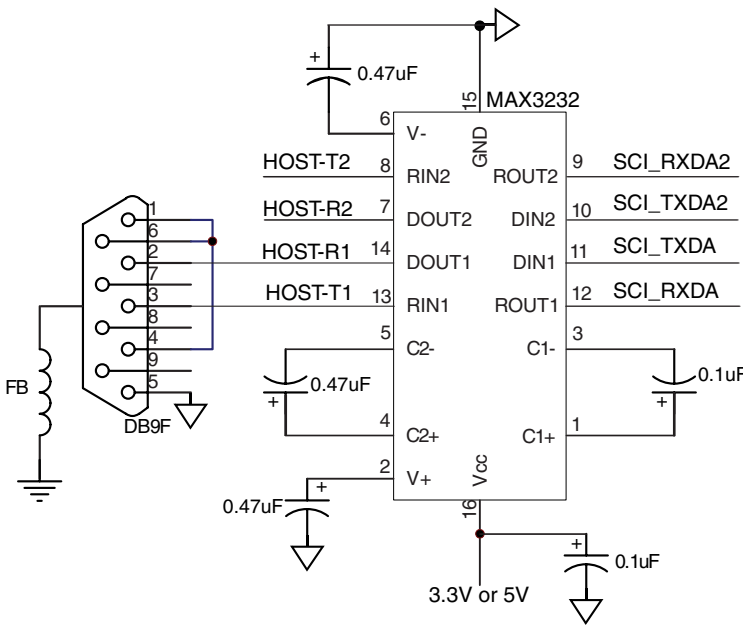

Figure 13. Typical SCI to RS232 circuit

NOTE

The commercial grade MAX3232 device is not rated for the full automotive temperature of -40 to +125° C and is not intended for automotive applications. This circuit should not be used or populated in a production module intended for automotive use. However, in many cases, the RS-232 interface is intended only as a development interface; therefore, the commercial device can be used for prototyping purposes. Texas Instruments does offer a device option with an operating temperature range of -40 to +85° C. Texas Instruments has an enhanced version of the device, MAX3232-EP, that is intended for aerospace, medical, and defense applications. This version is available with an operating temperature range of –55 to +125° C.

Table 19. Typical RS-232D connector definition

Pin number	Description
1	Connect to pin 4 and 6
2	RS-232 TX (Transmit)
3	RS-232 RX (Receive)
4	Connect to pin 1 and 6
5	GND

Table continues on the next page...

Table 19. Typical RS-232D connector definition (continued)

Pin number	Description
6	Connect to pin 1 and 4
7	N/C
8	N/C
9	N/C

NOTE

N/C pins are not connected. The shell of the connector should be connected through a ferrite bead to ground.

9.2 Example LIN Interface

Local Interconnect Network (LIN) is a commonly used low-speed network interface that consists of a master node communicating with multiple remote slave nodes. Only a single wire is required for communication and is commonly included in the vehicle wiring harness. Figure 14 shows a typical interface implemented using the Freescale MC33661 LIN transceiver.

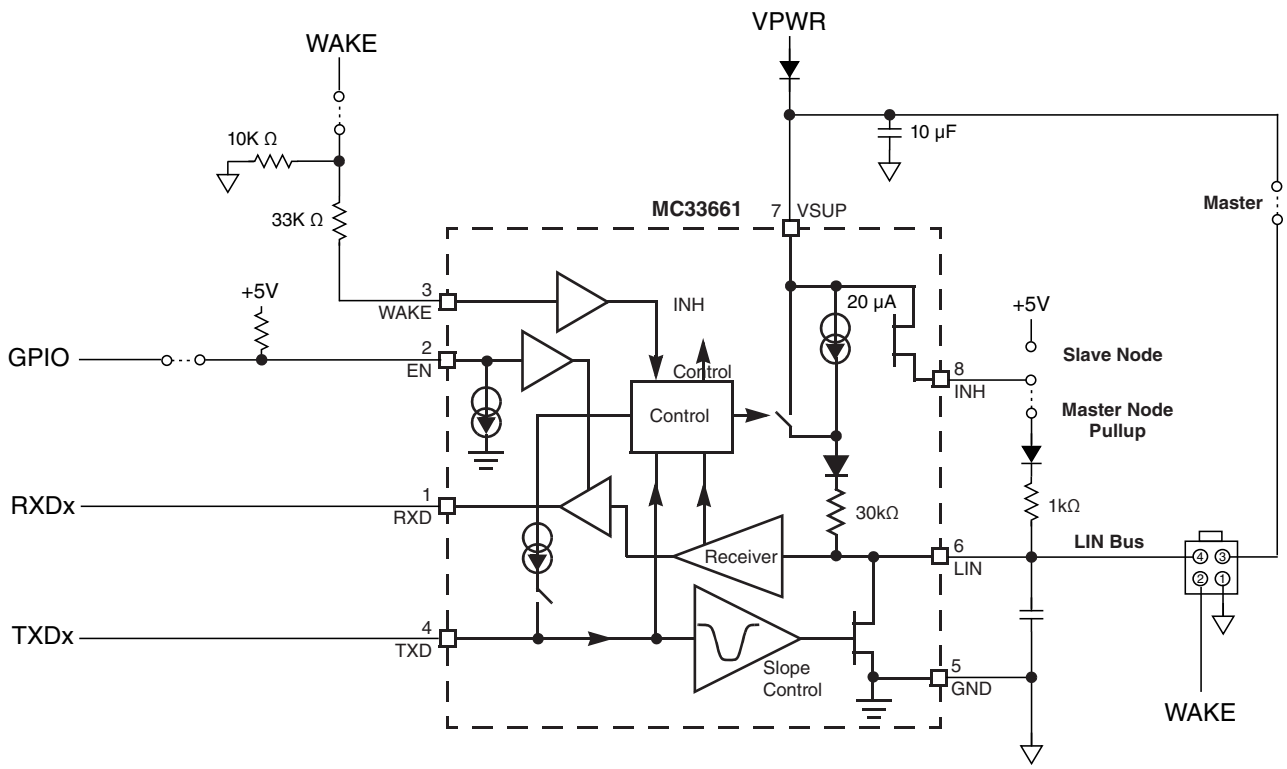

Figure 14. Typical LIN connections

Table 20 below shows the pins of the MC33661 and their typical connections to an MCU.

Table 20. MC33661 pin definitions and example system connections

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
1	RXD	Output	Receive Data Output	MCU LIN RXD	LIN Receive Data Output to the MCU
2	EN	Input	Enable Control	MCU GPIO	Enables operation of the device
3	Wake	Input	Wake Input	LIN Bus Wake[1]	Wake enables the devices out of sleep mode
4	TXD	Input	Transmit Data Input	MCU LIN TXD	LIN Transmit Data Input from the MCU
5	GND	Input	Ground	System Ground Reference	Device ground reference
6	LIN	Input/Output	LIN Bus	LIN bus	Bidirectional pin that represents the single-wire transmit and receiver
7	VSUP	Input	Power Supply	Protected battery voltage	This is the power supply for the device and is typically connected to a nominal 12 V
8	INH	Output	Inhibit Output	LIN Bus (if master)	The Inhibit pin controls either an external regulator to turn on a slave node or is connected through a resistor to the LIN bus on master nodes

1. Wake is an optional signal on the LIN connector, but may come directly from a switch.

There is no standard industry-defined LIN connector. Freescale uses a 4-pin Molex® connector that allows for the LIN bus pin, a power supply source (VPWR), a wakeup signal, and a ground reference. Slave nodes will often implement two connectors to allow a daisy-chain of multiple nodes to be easily implemented. Table 21 shows the Freescale pinout.

Table 21. LIN connector pinout recommendation

Function	Pin number	Pin number	Function
LIN Bus	4	3	VPWR
Wake	2	1	Ground

In a typical system, these pins would be used as follows:

- LIN bus—This is the single-wire LIN bus that connects between the master LIN node and the slave LIN nodes.
- VPWR—This connector input can be used as the power input to a slave node. Care should be taken that sufficient current is available for the total number of LIN slaves that are powered through this connection. In some systems, this may come from the master LIN node.

- Wake—The Wake signal is typically used for each individual slave node to enable the LIN physical interface of that node and to consequently enable the power supply (using the INH output) to power up the MCU to perform some action. For example, when the handle on a car door is lifted, to turn on the MCU that controls a function inside the vehicle, such as powering a smart dome light or enabling the controls of a smart seat.
- Ground—Ground reference for the module.

Part numbers for the 4-pin Molex Mini-Fit Jr.™ connector are shown in Table 22.

Table 22. Recommended connector part numbers

Description	Manufacturer part number (Molex)
4-pin right-angle connector with flange for target system, tin contacts, with latch	39-29-1048
4-pin right-angle connector with pegs for target system, tin contacts, with latch	39-30-1040
4-pin vertical connector with pegs for target system, tin contacts, with latch	39-29-9042
4-pin right-angle connector with flange for target system, gold contacts, latch	39-29-5043
Mating connector with latch for cable assemblies	39-01-2040
Socket terminal for mating cable assembly	39-00-0077

9.3 FlexRay Interface Circuitry using TJA1080A

FlexRay is an automotive fault-tolerant 2-wire communications interface. FlexRay is generally used at 10,000 Kbit/s (10 Mbit/s).

Freescale FlexRay devices implement a bus driver interface compliant with Communications System Electrical Physical Layer Specification, Version 2.1 Rev A.

Typically, FlexRay bus data rates of 10 Mbit/s, 8 Mbit/s, 5 Mbit/s, and 2.5 Mbit/s are supported and although the logic portions of the interface are implemented in the device, an external physical interface device is required to allow multiple FlexRay modules to be connected together.

The NXP™ (http://www.nxp.com) TJA1080A device is typically used as the FlexRay transceiver, although others are available. One transceiver is required for each FlexRay channel. The figure below shows the typical connections using the TJA1080A.

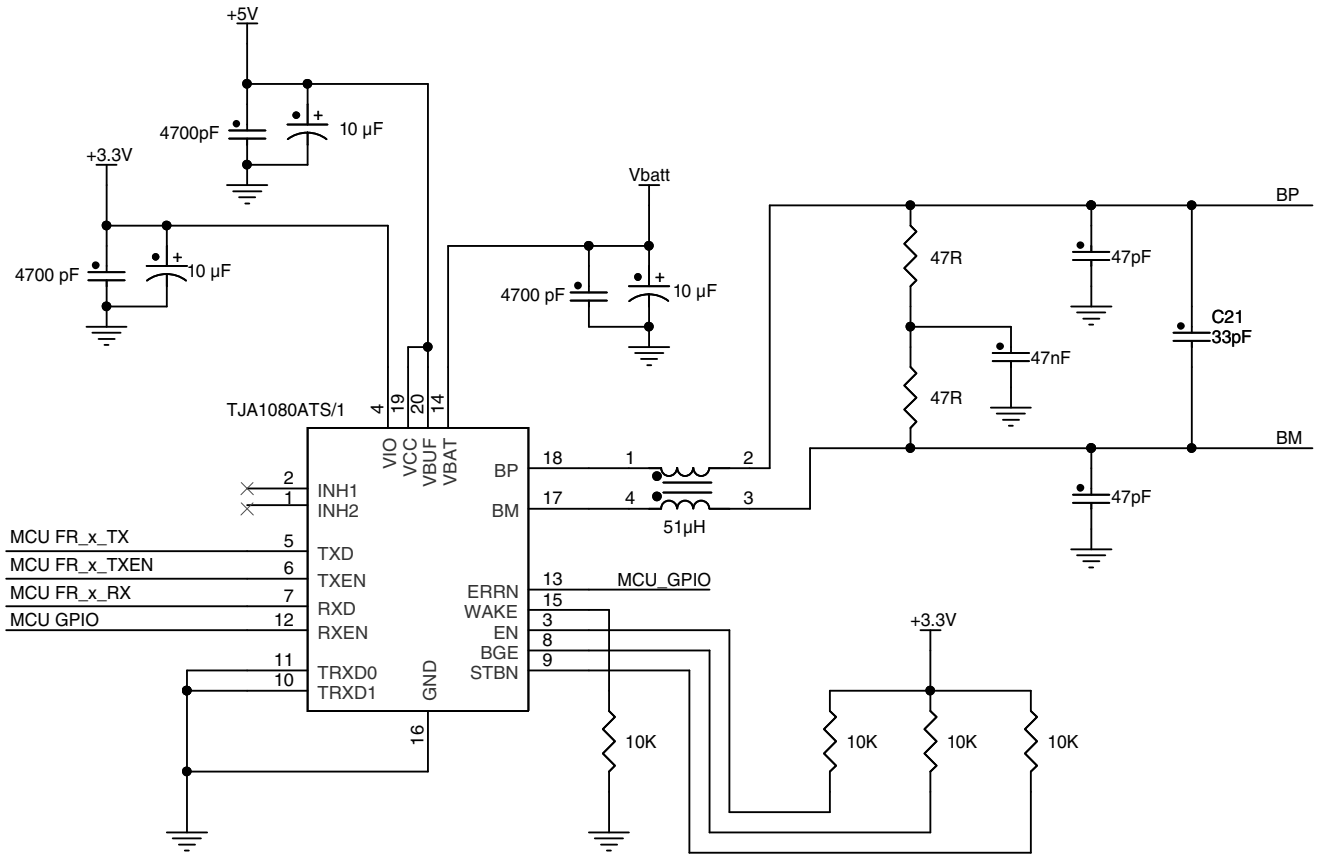

Figure 15. Typical FlexRay circuit

NOTE

- Decoupling shown as an example only
- TRXD0/TRXD1 is pulled to ground to enable the transceiver as a node device (not star configuration)
- In this configuration, only Normal mode is available. Further control is required to support low-power mode.

MCU and system connections to the TJA1080A are shown in the following table.

Table 23. TJA1080 pin definitions and example system connections

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
1	INH2	Output	Inhibit 2 Output	None	Inhibit output to enable/disable external power supply
2	INH1	Output	Inhibit 1 Output	None	Inhibit output to enable/disable external power supply
3	EN	Input	Enable Input	Pull up to 3.3 V or connect to a spare	Enable input (for mode selection (along with the

Table continues on the next page...

Table 23. TJA1080 pin definitions and example system connections (continued)

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
				MCU GPIO (output to MCU)	STBN pin). Internal pull-down (transmitter disabled, but allows reception, listen only mode)
4	V_{IO}	Input (power)	IO Power Supply	3.3 V	Power supply input for the MCU I/O signals
5	TXD	Input	Transmit Data	MCU FR_x_TX[1]	Transmit data from the MCU for transmitting on the FlexRay bus. Internal pullup
6	TXEN	Input	Transmit Enable	MCU FR_x_TXEN[1]	Transmit enable. A high level disables the transmitter. Internal pullup
7	RXD	Output	Receive Data	MCU FR_x_RX[1]	Receive data from the FlexRay bus to the MCU
8	BGE	Input	Bus Guardian Enable	Pull up to 3.3 V	The bus guardian input disables the transmitter. This feature is currently not supported
9	STBN	Input	Standby Input	Pull up to 3.3 V or connect to a spare MCU GPIO	Standby mode enable input (low to enter low power mode). Internal pull-down
10	TRXD1	Input/Output	Data Bus Line 1	Tie low	Data bus signal 1 for an inner star connection
11	TRXD0	Input/Output	Data Bus Line 0	Tie low	Data bus signal 0 for an inner star connection
12	RXEN	Output	Receive Enable	MCU GPIO (input to MCU)	Receive data enable indicates data is available from the bus (low during activity)
13	ERRN	Output	Error Output	MCU GPIO (input to MCU)	The error diagnostic output drives low upon an error
14	V_{BAT}	Input (power)	Battery Supply Voltage	Protected battery voltage	Battery supply voltage

Table continues on the next page...

Table 23. TJA1080 pin definitions and example system connections (continued)

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
15	WAKE	Input	Local Wake Up Input	Tie low or connect to switch or MCU GPIO	The local wakeup input forces
16	GND	Input	Ground	Ground	Ground, power supply return reference
17	BM	Input/Output	Bus Line Minus	To FlexRay Connector	FlexRay bus minus signal
18	BP	Input/Output	Bus Line Plus	To FlexRay Connector	FlexRay bus plus signal
19	V_{CC}	Input (power)	Supply Voltage	5 V	Supply voltage for internal logic
20	V_{BUF}	Input (power)	Buffer Supply Voltage	5 V	Supply voltage for the FlexRay bus minus/plus signals

1. x can be A or B depending on the channel requirements in the system.

To support the requirements of different worldwide OEMs, two connector types for FlexRay are used on evaluation boards:

- One socket DB-9 for both FlexRay channels
- Two Molex (Mini Fit Jr.™) headers, one for each FlexRay channel

However, there are various connectors used for production hardware. Figure 16 and Table 24 show example pin-outs for both connector types. The DB-9 connector allows for two channels on a single connector. The dual channels allow for redundant wiring for increased reliability. The dual channel capability is built into the FlexRay standard.

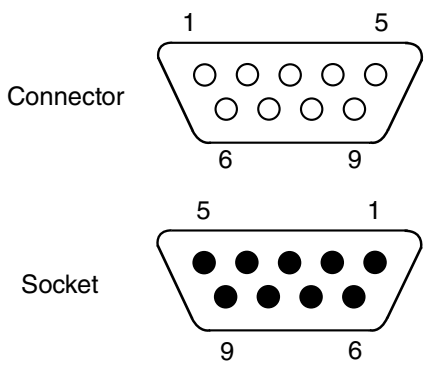

Figure 16. DB-9 connector and socket

Table 24. DB-9 pin-signal mapping

Pin Number	Signal Name	Full Name/Description
1	N/C	No connection
2	BM_A	Bus Minus Channel A
3	GND	No connection
4	BM_B	Bus Minus Channel B
5	SHIELD (OPTIONAL)	Optional Shield (if required)

Table continues on the next page...

Table 24. DB-9 pin-signal mapping (continued)

Pin Number	Signal Name	Full Name/Description
6	N/C	No connection
7	BP_A	Bus Plus Channel A
8	BP_B	Bus Plus Channel B
9	N/C	No connection

NOTE

- A socket is used on the evaluation board and a cable with a connector connects with this.
- The metal shell of the socket should be connected through a ferrite bead to GND.

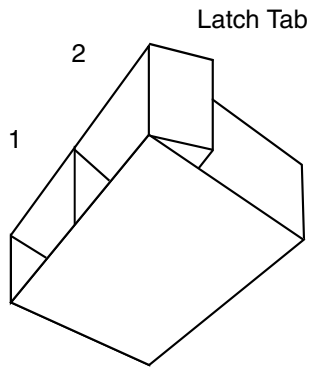

Figure 17. Molex connector picture

Table 25. Molex pin-signal mapping

Pin Number	Signal Name
1	BP
2	BM

NOTE

A connector is used on the evaluation board and a cable with a socket connects with this.

The Molex connectors are available in two types, one with pegs for mounting to the board and one without. The part numbers are shown in the following table.

Table 26. Recommended Molex Mini-Fit Jr. connector part numbers

Description	Manufacturer Part Number (Molex)
2-pin vertical connector with pegs for target system, tin contacts, latch	39-29-9022
2-pin vertical connector without pegs for target system, tin contacts, latch	39-28-8020
2-pin right-angle connector with pegs for target system, tin contacts, latch	39-30-0020

Table continues on the next page...

Table 26. Recommended Molex Mini-Fit Jr. connector part numbers (continued)

Description	Manufacturer Part Number (Molex)
2-pin right-angle connector with flange for target system, tin contacts, latch	39-29-1028
Mating connector with latch for cable assemblies	39-01-2020
Socket terminal for mating cable assembly	39-00-0077

9.4 CAN Interface Circuitry

Controller Area Network (CAN) is commonly used in almost all automotive applications to allow communication between various microchips in the car.

The number of CAN modules on-chip varies from device to device. A separate CAN transceiver is required for each CAN module, although some CAN transceivers may have more than one transceiver on a single chip. It is possible to connect two CAN modules to a single transceiver if the transmit pins are put into open-collector mode with an external pullup resistor. However, the value of this resistor may limit the maximum speed of the CAN module if not sized properly for the speed.

Freescale CAN modules conform to CAN protocol specification version 2.0 B, and the transceivers shown in this application note comply with ISO 11898 physical layer standard.

Typically, CAN is used at either a low speed (5 Kbit/s to 125 Kbit/s) or a high speed (250 Kbit/s to 1 Mbit/s). Powertrain applications typically use a high speed (HS) CAN interface to communicate between the engine control unit and the transmission control unit. Body and chassis applications typically use a low speed (LS) CAN interface. In the dashboard of a vehicle, there is typically a gateway device that interfaces between HS and LS CAN networks.

Freescale has a high-speed standalone CAN physical interface device with built-in diagnostic capabilities (MC33902), as well as CAN transceivers integrated with other functions[4]. Other popular CAN transceivers include the NXP devices shown in the following table. Example TJA1050 HS and TJA1054 LS circuits are shown in this application note.

Table 27. NXP CAN transceiver comparison

	TJA1050	TJA1054	TJA1040	TJA1041
Bitrate (Kbit/s)	1000	125	1000	1000
Modes of operation	Normal, Listen-only	Normal, Standby, Sleep	Normal, Standby	Normal, Listen-only, Standby, Sleep

9.4.1 High-Speed CAN With Diagnostics: MC33902 Interface

For target systems that require full diagnostics of the CAN interface, the Freescale MC33902 high-speed CAN transceiver is available. Features of this device are:

- High-speed CAN interface for baud rates of 40 Kbit/s to 1.0 Mbit/s
- Compatible with ISO 11898 standard
- Single supply from battery
- I/O compatible from 2.75 V to 5.5 V via a dedicated input terminal (3.3 V or 5.0 V logic compatible)
- Low-power mode with remote CAN wakeup and local wake-up recognition and reporting

4. An example device is the MC33905 that includes a 5 V power supply controller, a CAN transceiver physical interface, and a LIN transceiver physical interface.

- CAN bus failure diagnostics and TXD/RXD pin monitoring, cold start detection, and wake-up sources reported through the ERR pin
- Enhanced diagnostics for bus, TXD, RXD, and supply pins available through pseudo-SPI via existing terminals EN, STBY, and ERR
- Split terminal for bus recessive level stabilization
- INH output to control external voltage regulator

A block diagram of this transceiver is shown below.

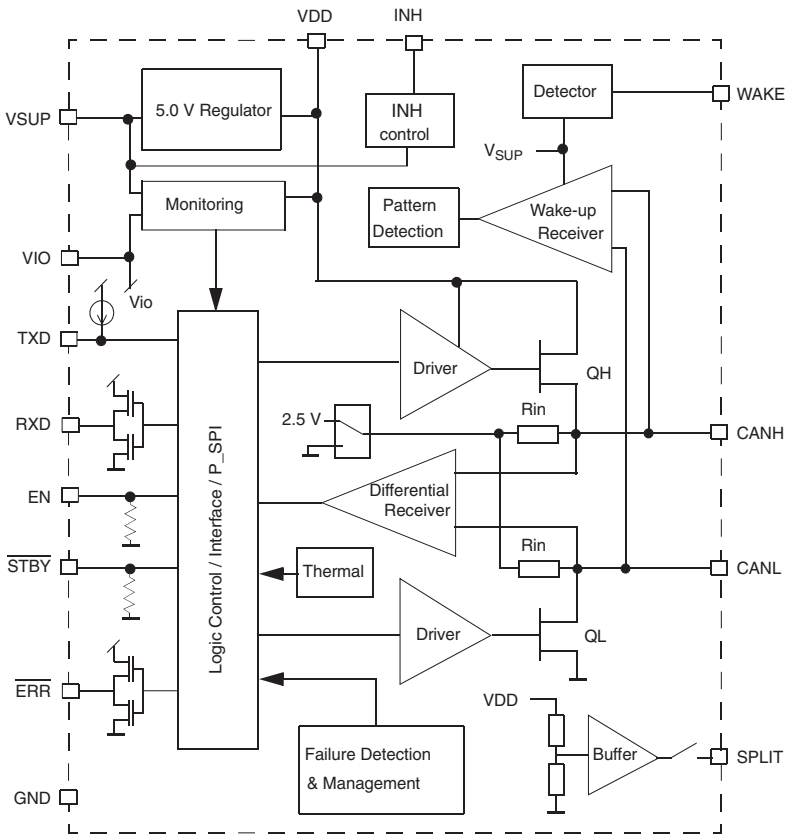

Figure 18. MC33902 block diagram

While a full SPI interface is not available for the diagnostic information, a quasi-SPI interface is available to communicate to the MCU. This interface is referred to as the P_SPI interface in the MC33902 data sheet.

The figure below shows an example schematic using the MC33902.

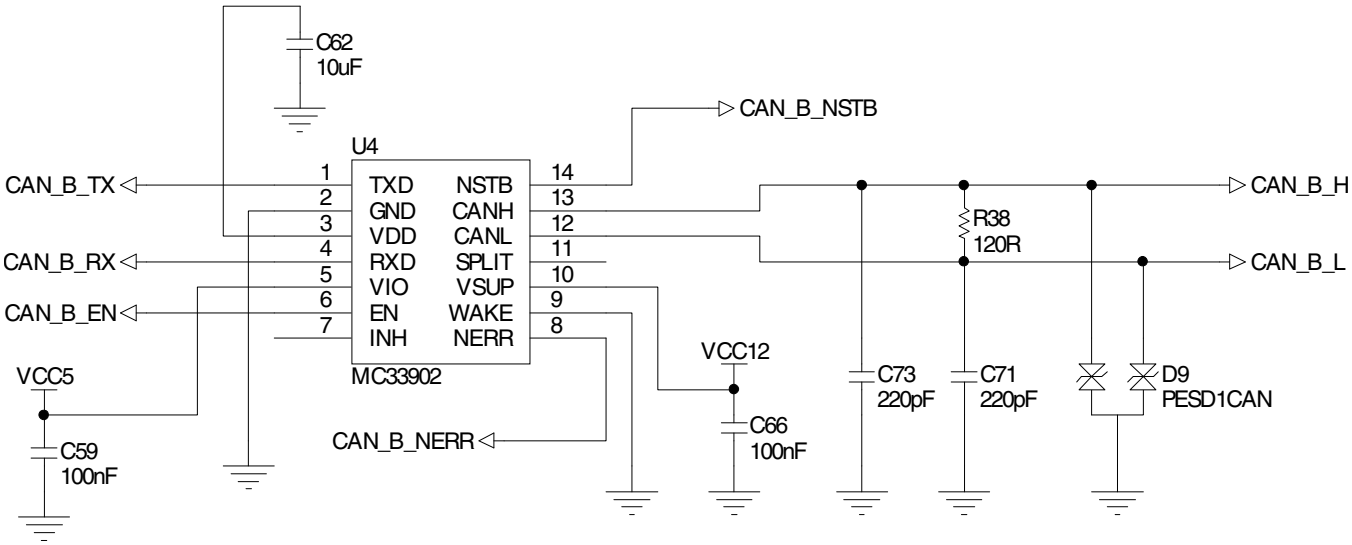

Figure 19. MC33902 high-speed CAN schematic

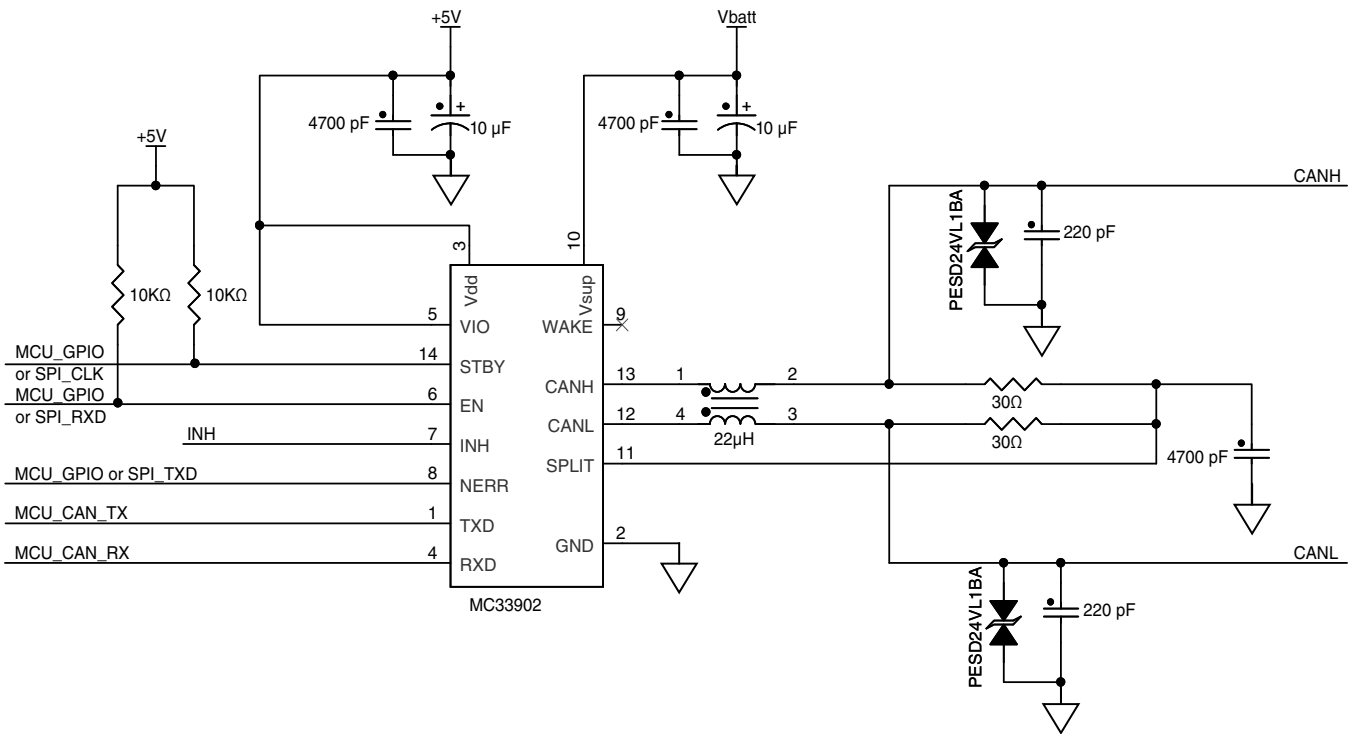

Figure 20. Typical high-speed CAN circuit using the MC33902

NOTE

- Decoupling and Bus protection shown as an example only.

The table below shows the pins of the MC33902 and the possible connections to a MCU and the target system.

Table 28. MC33902 pin definitions and example system connections

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
1	TXD	Input	Transmit Data	MCU CAN TXDA	CAN transmit data input from the MCU
2	GND	Output	Ground	Ground	Ground termination
3	VDD	Output	VDD Internal Regulator Output	Bypass capacitors only	5 V power supply output. Requires external bypass capacitors.
4	RXD	Output	Receive Data	MCU CAN TXDA	CAN receive data output to the MCU
5	VIO	Input	Voltage Supply for IO	3.3 V or 5 V	Supply voltage input for the digital input and output pins. This should be matched to the IO voltage supply of the MCU. Most typically, this is 5 V, but could also be 3.3 V.
6	EN	Input	Enable	Main MCU GPIO or SPI transmit data outputeTPUA31 (GPIO)	This is the enable input for the device in static mode control. This is the master output/slave input when used in SPI mode, and the MOSI (master out, slave in) during SPI operation.
7	INH	Output	Inhibit	Use depends on intended operation (see text below)	Inhibit output for control of an external power supply regulator
8	$\overline{\text{ERR}}$	Output	Active Low Error	Main MCU GPIO or SPI receive data inputeTPUA26 (GPIO)	Pin for static error and wakeup flag reporting MISO (master in, slave out) during SPI operation
9	WAKE	Input	Wake	MCU GPIO (output)Tied to ground	Wake input
10	VSUP	Input	Voltage Supply	Battery voltage	Battery supply pin, nominally 12 V
11	SPLIT	Output	Split	CAN termination midpointNot Used	Output for connection of the CAN bus termination middle point
12	CANL	Input/Output	CAN Bus Low	CAN Bus Connector	CAN bus low pin
13	CANH	Input/Output	CAN Bus High	CAN Bus Connector	CAN bus high pin
14	$\overline{\text{NTSB}}$	Input	Standby	Main MCU GPIO or SPI Clock outputeTPUA28 (GPIO)	Standby input for device static mode control. CLK (Clock) during P_SPI operation

The use of the Inhibit pin (INH) is dependent on the selected target system operation. INH can turn an external power supply on and therefore wake a connected MCU for operation to save power when MCU operation is not required. In MPC5500 and MPC5600 automotive power train applications (engine control), INH is typically not used. However, in automotive body and chassis applications, it may be used.

9.4.2 High-Speed CAN TJA1050 Interface

The figure below shows the typical connections for the physical interface between the MCU and the CAN bus for high-speed applications using the NXP TJA1050 HS CAN transceiver.

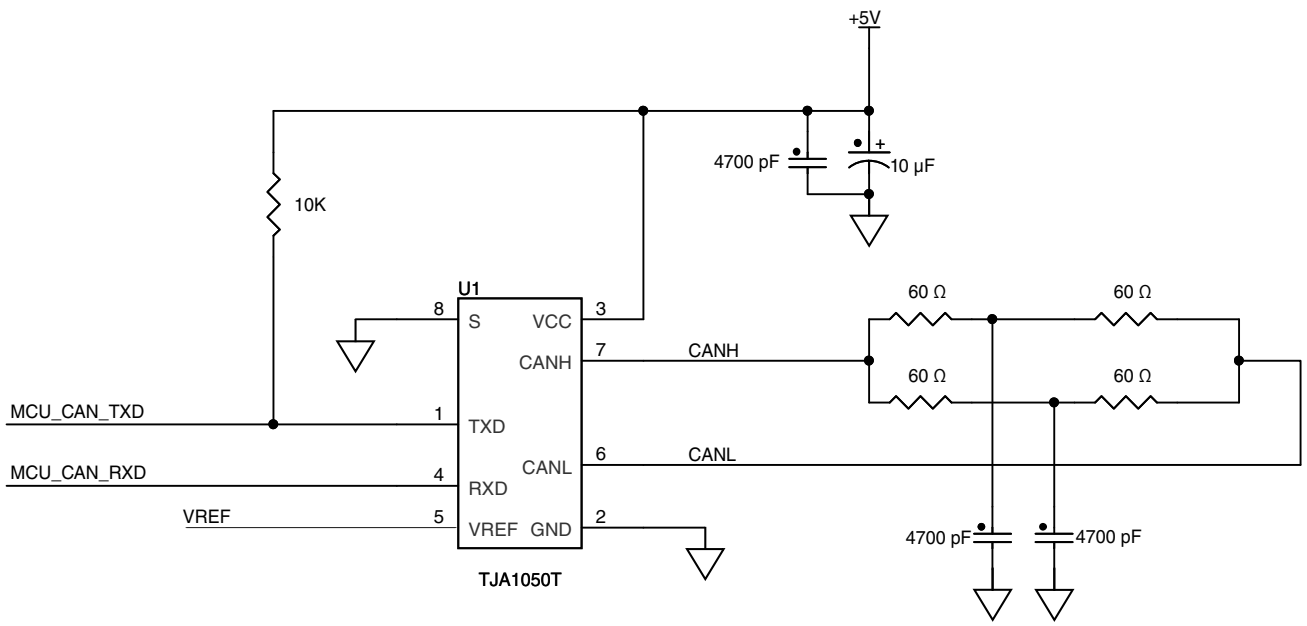

Figure 21. Typical high-speed CAN circuit using TJA1050

NOTE

- Decoupling shown as an example only.
- TXD/RXD pullup/pulldown may be required, depending on device implementation.

The table below describes the TJA1050 pin and system connections.

Table 29. TJA1050 pin definitions and example system connections

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
1	TXD	Input	Transmit Data	MCU CAN TXD	CAN transmit data input from the MCU
2	GND	Output	Ground	Ground	Ground return termination
3	VCC	Input	—	5 V	Voltage supply input (5 V)
4	RXD	Output	Receive Data	MCU CAN RXD	CAN receive data output to the MCU
5	VREF	Output	Reference voltage Output	Not used	Mid-supply output voltage. This is typically not used in many systems, but can be used if voltage translation needs to be done between the CAN transceiver and the MCU.
6	CANL	Input/Output	CAN Bus Low	CAN Bus Connector	CAN bus low pin
7	CANH	Input/Output	CAN Bus High	CAN Bus Connector	CAN bus high pin

Table continues on the next page...

Table 29. TJA1050 pin definitions and example system connections (continued)

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
8	S	Input	Select	Grounded or MCU GPIO	Select for high-speed mode or silent mode. Silent mode disables the transmitter, but keeps the rest of the device active. This may be used in case of an error condition.

9.4.3 Low-Speed CAN TJA1054 Interface

The figure below shows the typical connections for the physical interface between the MCU and the CAN bus for low-speed applications using the NXP TJA1054 LS CAN transceiver. Optionally, the standby and enable pins can be connected to MCU GPIO pins for additional control of the physical interface.

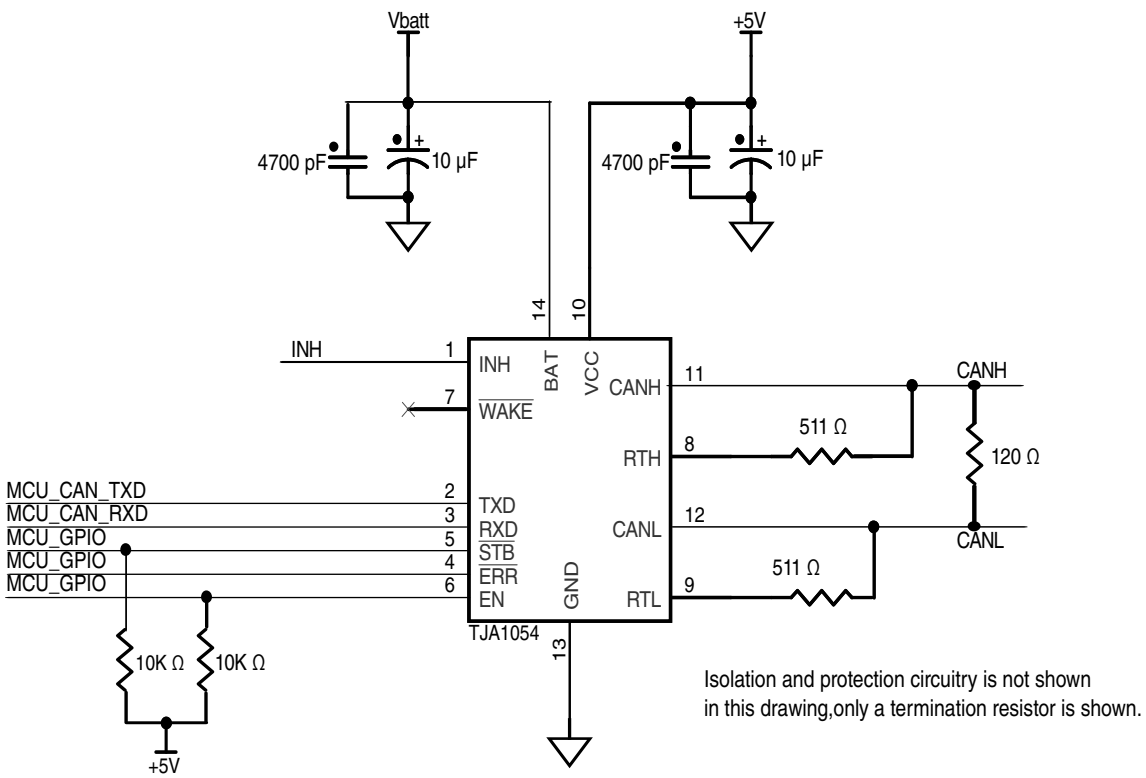

Figure 22. Typical low-speed CAN circuit using TJA1054

NOTE

- Decoupling shown as an example only.
- $\overline{\text{STB}}$ and EN should be pulled high for Normal mode. These signals can optionally be connected to MCU GPIO pins to allow MCU control of the physical interface.

The table below describes the TJA1054 pins and system connections.

Table 30. TJA1054 pin definitions and example system connections

Pin number	Pin name	Pin direction	Full pin name	MCU or system connection	Description
1	INH	Input	Inhibit	Typically not connected	Inhibit output for control of an external power supply regulator if a wake up occurs
2	TXD	Input	Transmit Data	MCU CAN TXD	CAN transmit data input from the MCU
3	RXD	Output	Receive Data	MCU CAN RXD	CAN receive data output to the MCU
4	$\overline{\text{ERR}}$	Output	Error	MCU GPIO	The error signal indicates a bus failure in normal operating mode or a wake-up is detected in Standby or Sleep modes.
5	$\overline{\text{STB}}$	Input	Voltage Supply for IO	MCU GPIO	Standby input for device. It is also used in conjunction with the EN pin to determine the mode of the transceiver.
6	EN	Input	Enable	MCU GPIO	Enable input for the device. It is also used in conjunction with the STB pin to determine the mode of the transceiver.
7	$\overline{\text{WAKE}}$	Input	Wake	Typically not connected	Wake input (active low), both falling and rising edges are detected
8	RTH	Input	Termination Resistor High	Resistor to CANH	Termination resistor for the CAN bus high[1]
9	RTL	Input	Termination Resistor Low	Resistor to CANL	Termination resistor for the CAN bus low[1]
10	VCC	Input	Voltage Supply	5 V	Digital IO supply voltage, 5 V
11	CANH	Output	CAN Bus High	CAN Bus Connector	CAN bus high pin
12	CANL	Input/Output	CAN Bus Low	CAN Bus Connector	CAN bus low pin
13	Ground	Output	Ground	Ground	Ground return termination path
14	BAT	Input	Standby	Battery voltage	Battery supply pin, nominally 12 V

1. This allows the transceiver to control the CAN bus impedance under an error condition.

9.4.4 Recommended CAN Connector

Generally DB-9 connectors are used for evaluation boards to connect CAN modules together, whereas there are various connectors used for production hardware. The following figure shows the DB-9 connector and socket configuration of a typical evaluation board connector. A socket is used on the evaluation board and a cable with a connector connects with it.

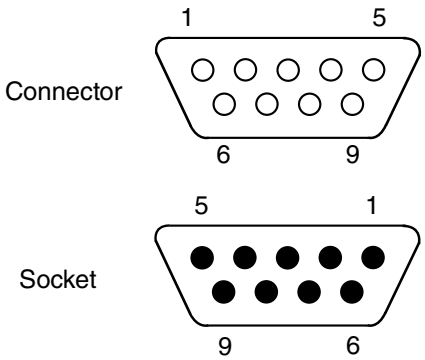

Figure 23. DB-9 connector and socket

The table below shows the typical connector pin-out definition.

Table 31. DB-9 pin signal mapping

Pin number	Signal name
1	N/C
2	CAN_L
3	GND
4	N/C
5	CAN_SHIELD (OPTIONAL)
6	GND
7	CAN_H
8	N/C
9	CAN_V+ (OPTIONAL)

NOTE

The metal shell of the socket should be connected through a ferrite bead to the chassis ground.

9.5 Ethernet Interface Examples

Ethernet is a communication technology that was originally developed for creating local area networks (LANs) between computers. Over time, it has become the standard wired communications network for the PC and is widely used within telecommunications and industrial applications. In recent years, Ethernet has found its way into automotive electronics with deployment in diagnostic and camera applications.

The Ethernet MAC-NET (ENET) module on the MPC5775K device is a communication controller that supports 10 and 100 Mbit/s Ethernet/IEEE 802.3 networks. It includes functionality to accelerate the processing of various common network layer protocols such as IP, TCP and UDP. An external transceiver interface and transceiver function are required to complete the interface to the media. The figure below shows a typical set up of the compete interface to the network. Here a DP83848VYB from Texas Instruments is used as the ethernet physical transceiver (PHY). This will be used throughout Ethernet Interface Examples to show an example interface.

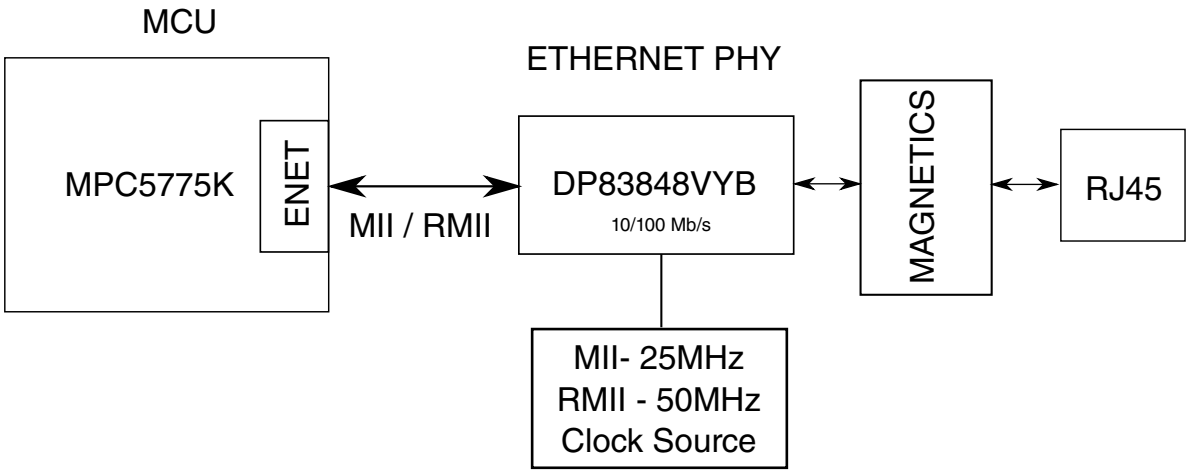

Figure 24. Ethernet application configuration example

As shown in Figure 24 the ENET can interface to a PHY using either the 10/100 Mbit/s MII or RMII or the 10 Mbit/s only MII-Lite/7-wire interface. The ENET signals from the MCU take their voltage level from the VDD_HV_IO supply domain. Most PHYs require signals in the 3.3 V range, so the VDD_HV_IO should be set accordingly. Be aware that this domain is shared with the FlexRay I/O.

The ENET signals are summarized in Table 32 and their use in each interface type is highlighted as REQ = Required, N/A = Not applicable for this mode and OPN = Optional.

NOTE

The signals required by different PHYs will vary in some cases for each interface option; see the data sheet of your selected PHY.

Table 32. MPC5775K ENET signal overview

Signal Name	Description	Direction	MII	RMII	7-Wire	Port Options
ENET_MDIO	Management Data Input/ Output	I/O	REQ	N/A	N/A	PG[8]
ENET_MDC	Management Data Clock	O	REQ	N/A	N/A	PG[9]
ENET_RMII_CLK	RMII Reference Clock Input/ Output	I/O	N/A	REQ	N/A	PG[11]
ENET_TX_EN	Transmit Enable	O	REQ	REQ	REQ	PC[15], PI[3]
ENET_TXD0	Transmit Data 0	O	REQ	REQ	REQ	PD[0], PG[3]
ENET_TXD1	Transmit Data 1	O	REQ	REQ	N/A	PD[3], PG[4]
ENET_TXD2	Transmit Data 2	O	REQ	N/A	N/A	PD[4], PG[6]
ENET_TXD3	Transmit Data 3	O	REQ	N/A	N/A	PM[5], PG[10]
ENET_TXCLK	Transmit Clock	I	REQ	N/A	REQ	PG[11]
ENET_RXDV	Receive Data Valid	I	REQ	REQ	N/A	PD[2], PI[2]
ENET_RXD0	Receive Data 0	I	REQ	REQ	REQ	PD[5]
ENET_RXD1	Receive Data 1	I	REQ	REQ	N/A	PD[6]
ENET_RXD2	Receive Data 2	I	REQ	N/A	N/A	PH[4]
ENET_RXD3	Receive Data 3	I	REQ	N/A	N/A	PH[5]
ENET_RXCLK	Receive Clock	I	REQ	N/A	REQ	PD[1], PH[13]

The following figure shows the typical connections for the physical interface between the MPC5775K MCU and the DP83848VYB PHY from Texas Instruments. The configuration has been set up to provide the option of using either MII or RMII interface from the MCU. A PulseJack™ J1011F21PNL RJ45 connector with integrated magnetics is also shown. When using RMII mode, the PHY must be clocked at 50 MHz. This can be done by supplying X1 with a clock output from the MCU in place of the 25 MHz crystal used in MII mode.

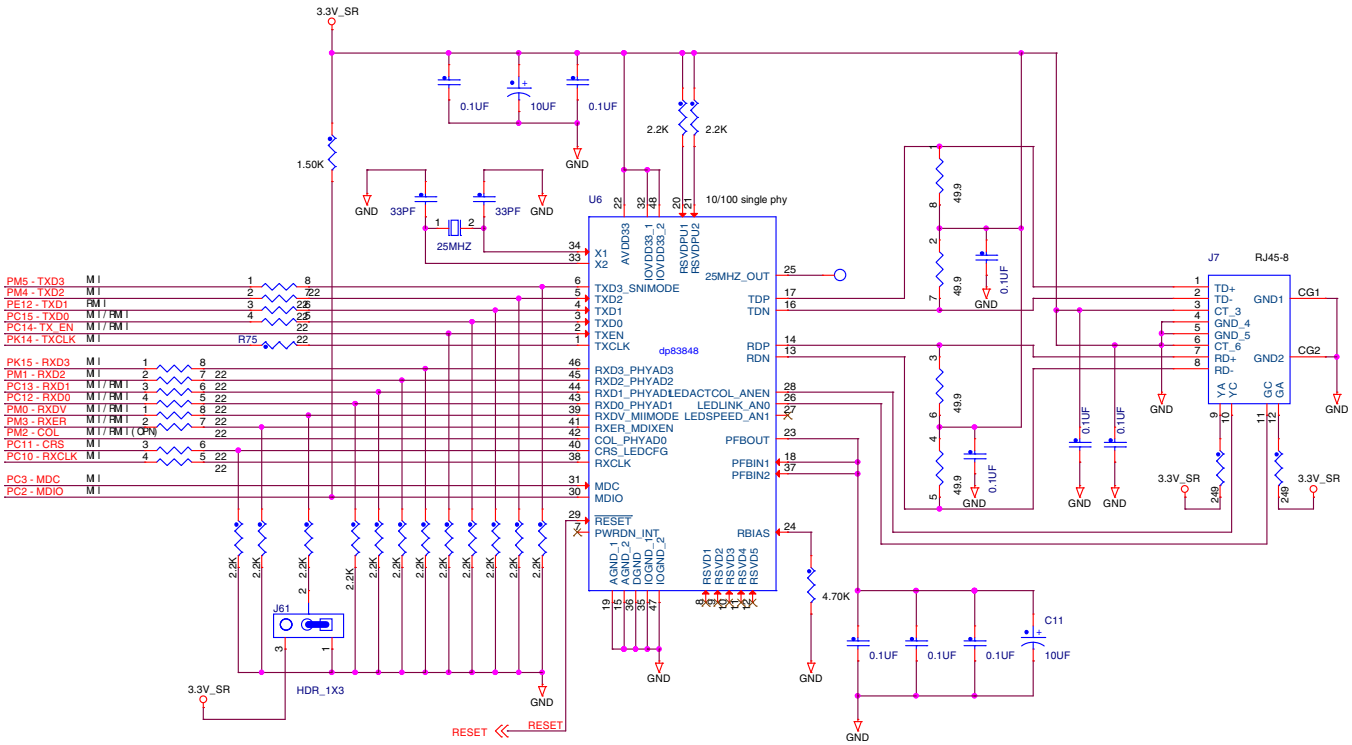

Figure 25. Ethernet example circuitry

10 Additional Connections

The device has several miscellaneous pins that require external connections. Information on these are covered in this section.

Internal Test

- K20 is a Freescale internal test pin and must always be connected directly to ground
- J3, J4, J1, J2, H3, H4, F1, F2, G1, G2 are Freescale internal measurement pins. These pins must be left floating as connecting to power or ground can cause damage to the device

Alternative Boot

Input pins for selecting alternative boot modes are available. Please see the Boot Assist Module (BAM) and System Status and Configuration Module (SSCM) chapters in the device reference manual for more information.

- FAB can be found on pin M18
- ABS[0] can be found on pin L18.
- ABS[2] can be found on pin M17

FCCU External Error Signal

The Fault Collection and Control Unit (FCCU) has error output signals for the communication of errors to external devices. The use of these signals is application specific, more information can be found in the FCCU chapter in the device reference manual.

Additional Connections

- FCCU_F0 can be found on Y15
- FCCU_F1 can be found on W15

Non-Maskable Interrupt (NMI)

NMI input can be found on pin Y18. The use of this pin is application specific; please see the Wake-up Unit (WKPU) chapter in the device reference manual for more information.

If the pin is not used, it can be rendered non-functional by connecting to VDD_HV_IO through a 4.7 Kilo Ohm or 10 Kilo Ohm pull-up resistor.

No Connection Pins

There are a number of non-functional pins that must be dealt with appropriately.

Table 33. No connection pins

Pins	No Connect Strategy
d3	Connect to ground (GND)
r19, r20	Connect to ground (GND)
t4	Leave floating
t18, t19	Connect to ground (GND)
u3	Leave floating
u10	Connect to ground (GND)
v10	Connect to ground (GND)
k20	Connect to ground (GND)

Appendix A Release Notes

Table A-1 summarizes revisions to this document.

Table A-1. Revision History

Rev	Date	Description of Changes

1	3/2015	• In section Power Supply removed mention of 5V SAR ADC reference option
		• In section Power Supply Signals and Decoupling
		  • Removed mention of 5V SAR ADC reference option
		  • Consolidated VDD_HV_PDI pins
		  • Changed name of VDD_LV_DRFPLL to VDD_LV_LFASTPLL and added explanation note
		  • Changed recommended capacitance configurations for supply pin decoupling
		• In section Decoupling Capacitors Layout Priority added VDD_LV_IO and consolidated VDD_HV_PDI pins
		• In section Power Management Controller
		  • Removed mention of 5V SAR ADC reference option
		  • Modified diagram to remove 5V SAR ADC reference option
		  • Added note describing function of VREG_POR_B
		• In section SMPS External Component Configuration added detail to description
		• In section External Supply Mode
		  • Removed mention of 5V SAR ADC reference option
		  • Modified diagram to remove 5V SAR ADC reference option
		• In section Power-up Sequence added rule on powering VDD_HV_IO and VDD_HV_PMU
		• In section External Reset Signals added note on VREG_POR_B functionality

Table continues on the next page...

Table A-1. Revision History (continued)

Rev	Date	Description of Changes

		• In section MPC5775K High-Speed Nexus Serial Trace Connector added part number for serial trace connector
		• In section Minimum External Circutiry corrected Nexus clock lines recommended capacitance values
		• In table AFE external component connections
		  • Changed SD_R trimming resistor tolerance
		  • Corrected function description on VDD_LV_SDADC and VDD_LV_RADARDIG pins

2	6/2015	• In section Power Supply Signals and Decoupling removed VDD_HV_IO_PWM and consolidated into VDD_HV_IOx supply.
		• Added footnote to VDD_LV_IO_AURORA
		• In section Power Management Controller modified the supply connections diagrams
		  • Removed HV_IO_PWM
		  • Combined HV_IO_PDI_0 and HV_IO_PDI_1 into HV_IO_PDI
		  • Removed regulator supplying HV_REG_3V8 and connected this to 3.3 V regulator
		• In section Connecting External Clock Sources removed mention of configurable load capacitance and added advice on parasitic capacitance on oscillator connection lines.

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