NXP Semiconductors
Application Note

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Hardware Design Considerations for MKW41Z/31Z/21Z BLE and IEEE 802.15.4 Device

1. Introduction

This application note describes Printed Circuit Board (PCB) design considerations for the MKW41Z, MKW31Z, and MKW21Z 48-pin Laminated QFN (LQFN) package. Included are layouts of the component copper layer, solder mask, solder paste stencil, PCB stack-up and component layout recommendations.

These recommendations are guidelines only and may need to be modified depending on the assembly house used and the other components on the board.

Contents

2. 48-pin LQFN component copper layer

Figure 1 shows a recommended component copper layer. This layer is also referred to as the top metal layer and is the layer to which the components are soldered. The footprint for the 48-pin LQFN package consists of 48 IC contact pads, and 16 centered ground pads. The copper pattern is as shown in *Figure 1*.

Use 0.25 mm via holes to connect to the ground plane layers. These are required for RF grounding and help to prevent solder float.

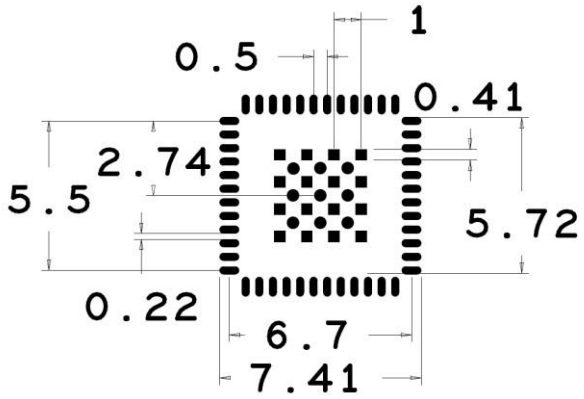


Figure 1. 48-pin LQFN component copper layer

2.1. 48-pin LQFN solder mask

The solder mask limits the flow of the solder paste during the reflow process. *Figure 2* shows a recommended solder mask pattern. The pattern represents openings in the solder mask.

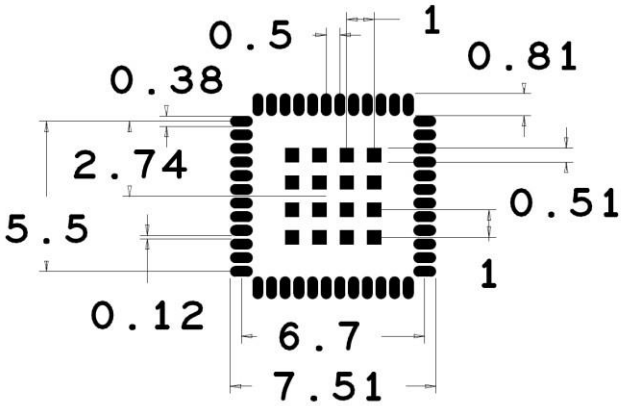


Figure 2. 48-pin LQFN solder paste stencil

2.2. 48-pin LQFN solder paste stencil

The solder paste stencil controls the pattern and thickness of the solder paste dispensed on the board. *Figure 3* shows a recommended solder stencil pattern. Stencil thickness should be approximately 0.1 mm.

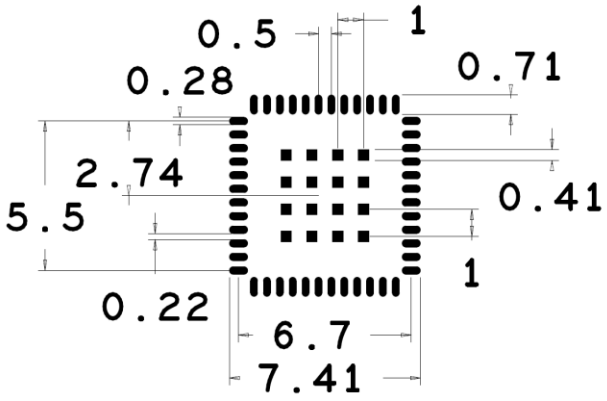


Figure 3. 48-pin LQFN solder stencil pattern

2.2.1. LGA problems with excess solder

Excess solder may cause the LGA to float or bridge between the package contacts. To use the correct amount of solder paste applied to the PCB, take into consideration the following:

- Stencil thickness
- Other components mounted on the PCB
- Manufacturing equipment
- Assembly house experience

3. 48-pin LQFN soldering profile

Figure 4 shows the recommended soldering profile for the MKW41Z 48-pin LQFN package, in a board size approximately 3.20 inches × 2.10 inches.

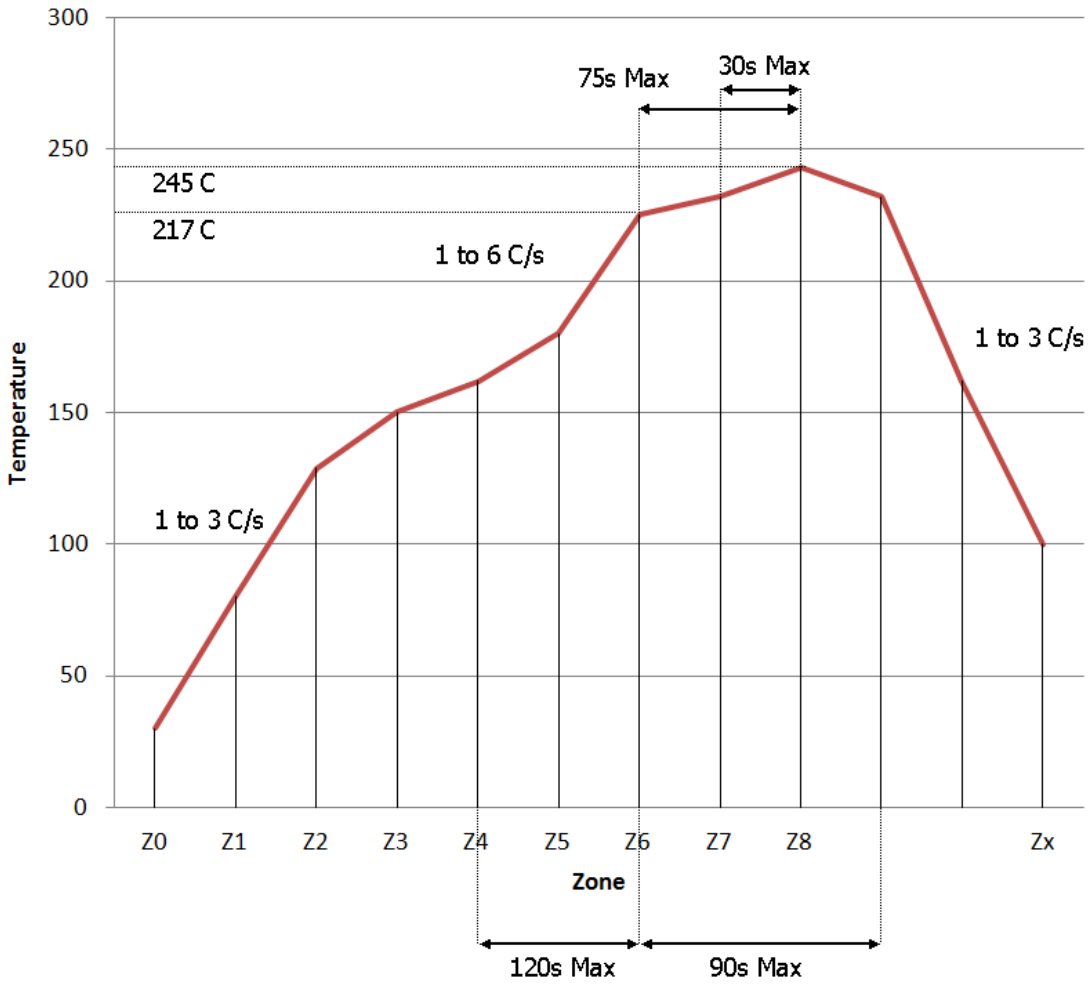


Figure 4. 48-pin LQFN soldering profile

4. 48-pin LQFN package dimensions

Figure 5 shows the 48-pin LQFN package dimensions.

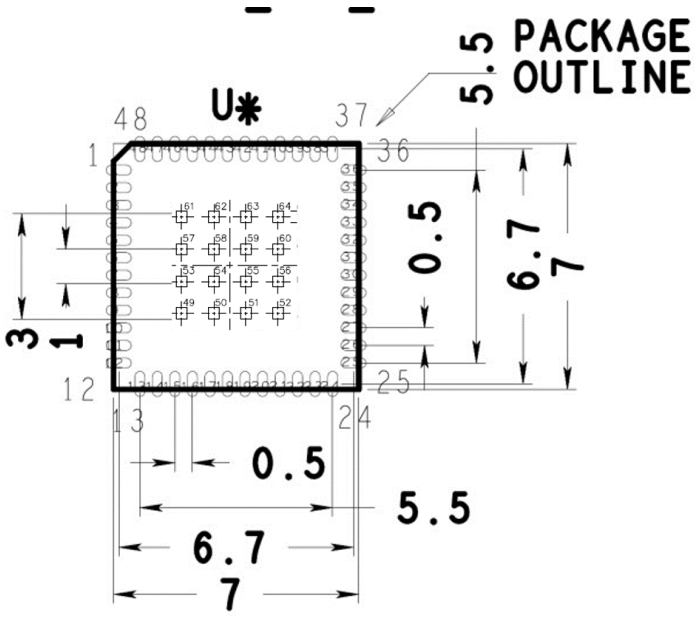


Figure 5. 48-pin LQFN package dimensions

5. 48-pin LQFN device marking details

The MKW41Z, MKW31Z, and MKW21Z devices are in the 48-pin LQFN (7 x 7 mm). *Figure 6* shows device marking examples for the LQFN device.

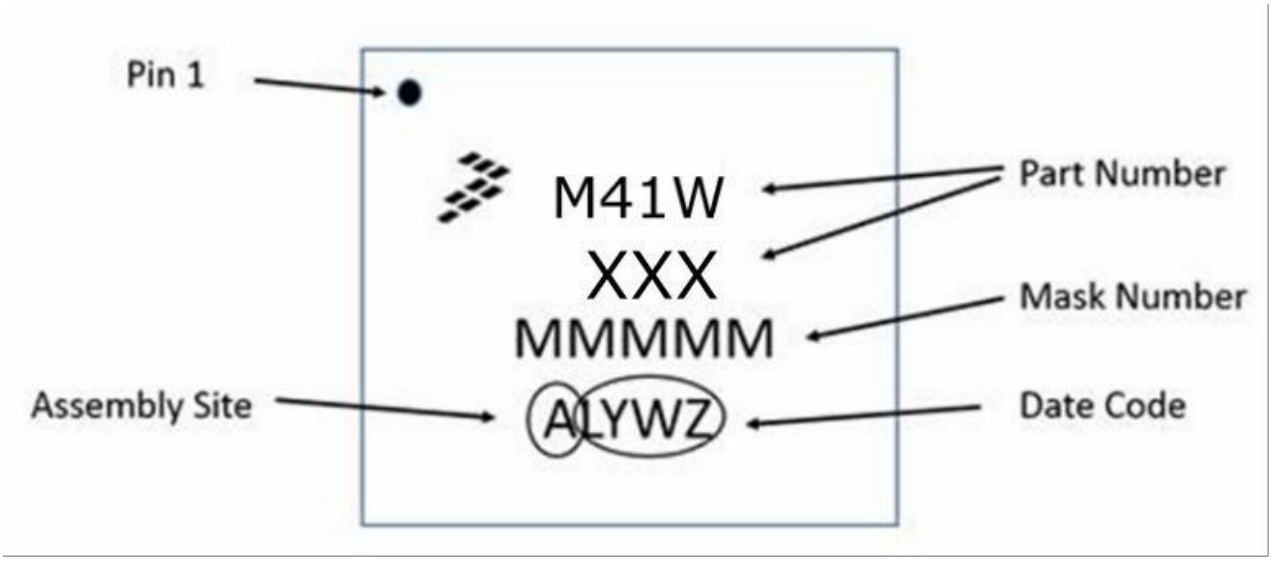


Figure 6. 48-pin LQFN device marking

NOTE

Your device part number may differ from the part number shown in *Figure 6*.

6. Design and board layout considerations

To have successful wireless hardware development, the proper device footprint, RF layout, circuit matching, antenna design, and RF measurement capability are essential. RF circuit design, layout, and antenna design are specialties requiring investment in tools and experience. With available hardware reference designs from NXP, RF design considerations, Design-in checklist (insert link here), and the guidelines contained in this application note, hardware engineers can successfully design BLE and IEEE 802.15.4 radio boards with adequate performance levels. *Figure 7* shows the FRDM-KW41Z development board. It contains the MKW41Z device and all necessary I/O connections.

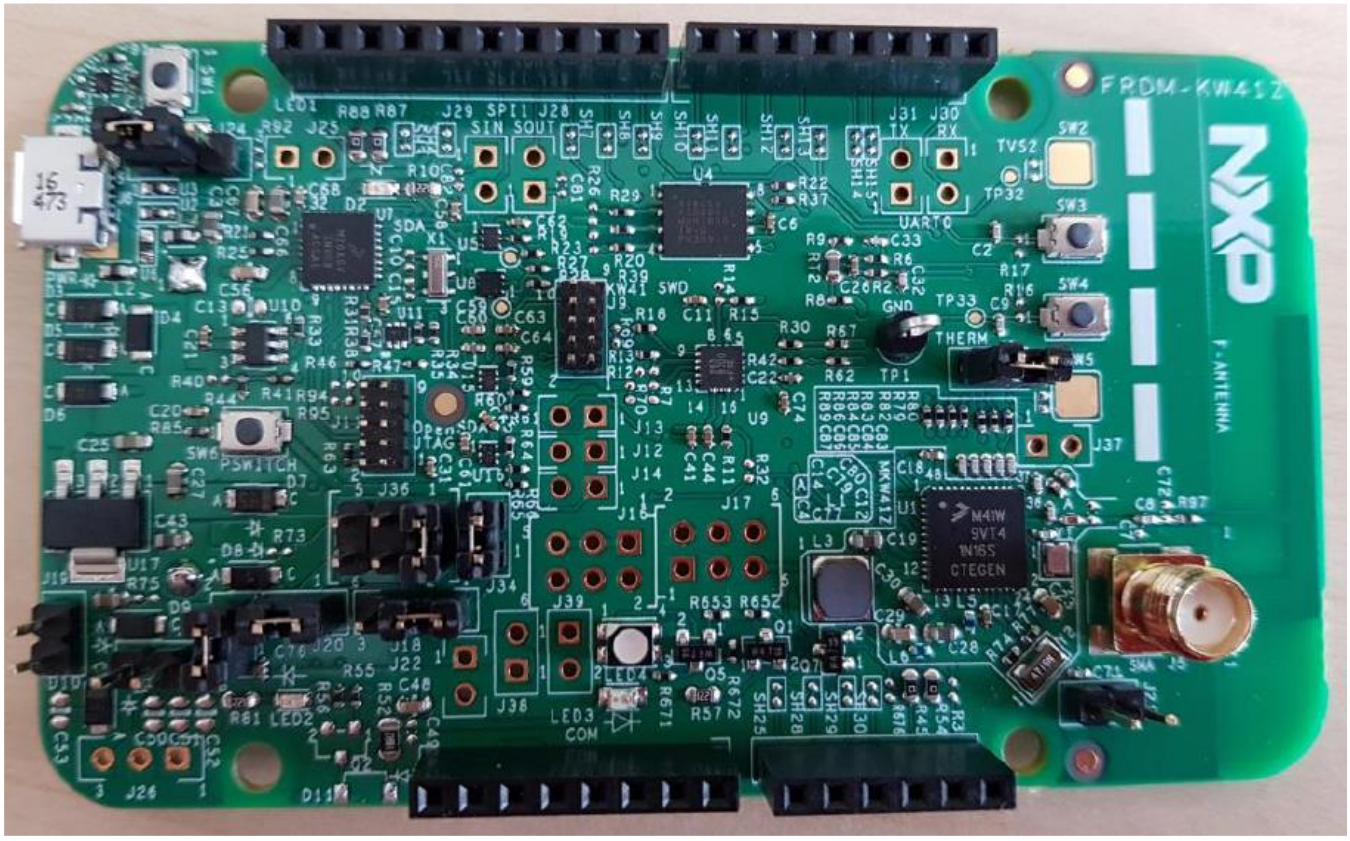


Figure 7. FRDM-KW41Z rev C1 development board

The device footprint and layout are critical and the RF performance is affected by the design implementation. For these reasons, use of the NXP recommended RF hardware reference designs are important for successful board performance. Additionally, the reference platforms have been optimized for radio performance. Even minor changes in the location of components can mistune the circuit. If the recommended footprint and design are followed exactly in the RF region of the board; sensitivity, output power, harmonic and spurious radiation, and range will have a high likelihood of meeting regulatory requirements.

The following subsections describe important considerations when implementing a wireless hardware design starting with the device footprint, RF circuit implementation, layout, PCB stack-up, component selection, antenna selection, and power supply layout. *Figure 8* shows an example of a typical layout with the critical RF section which must be copied exactly for optimal radio performance. The less critical layout area can be modified without reducing radio performance.

NOTE

Exact dimensions are not given in this document, but can be found in the design files for the FRDM-KW41Z and USB-KW41Z.

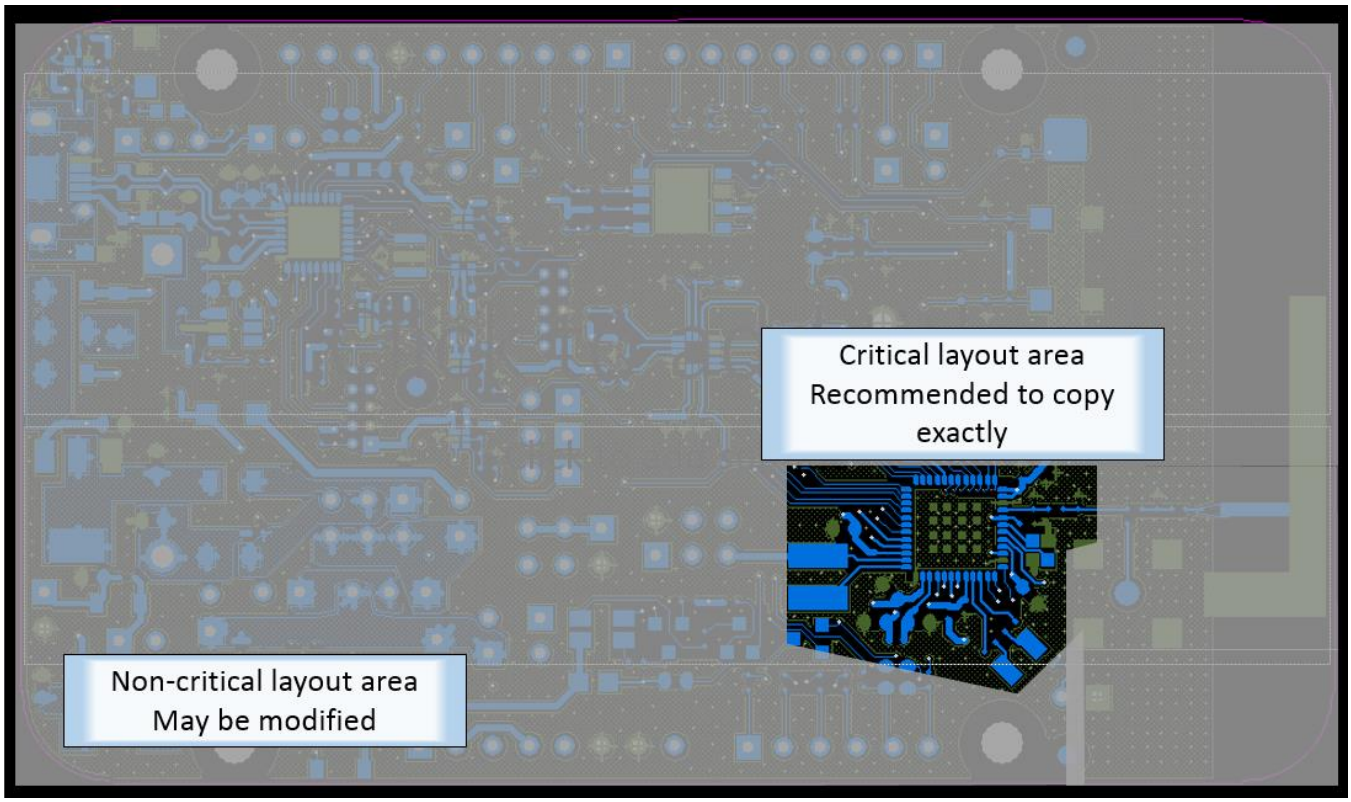


Figure 8. Critical layout areas

6.1. MKW41Z device footprint

The performance of the wireless link is largely influenced by the device's footprint. As a result, a great deal of care has been put into creating a footprint so that receiver sensitivity and output power are optimized to enable board matching and minimal component count. NXP highly recommends copying the die flag exactly as shown in *Figure 9*. This includes via locations as well. Deviation from these parameters can cause performance degradation.

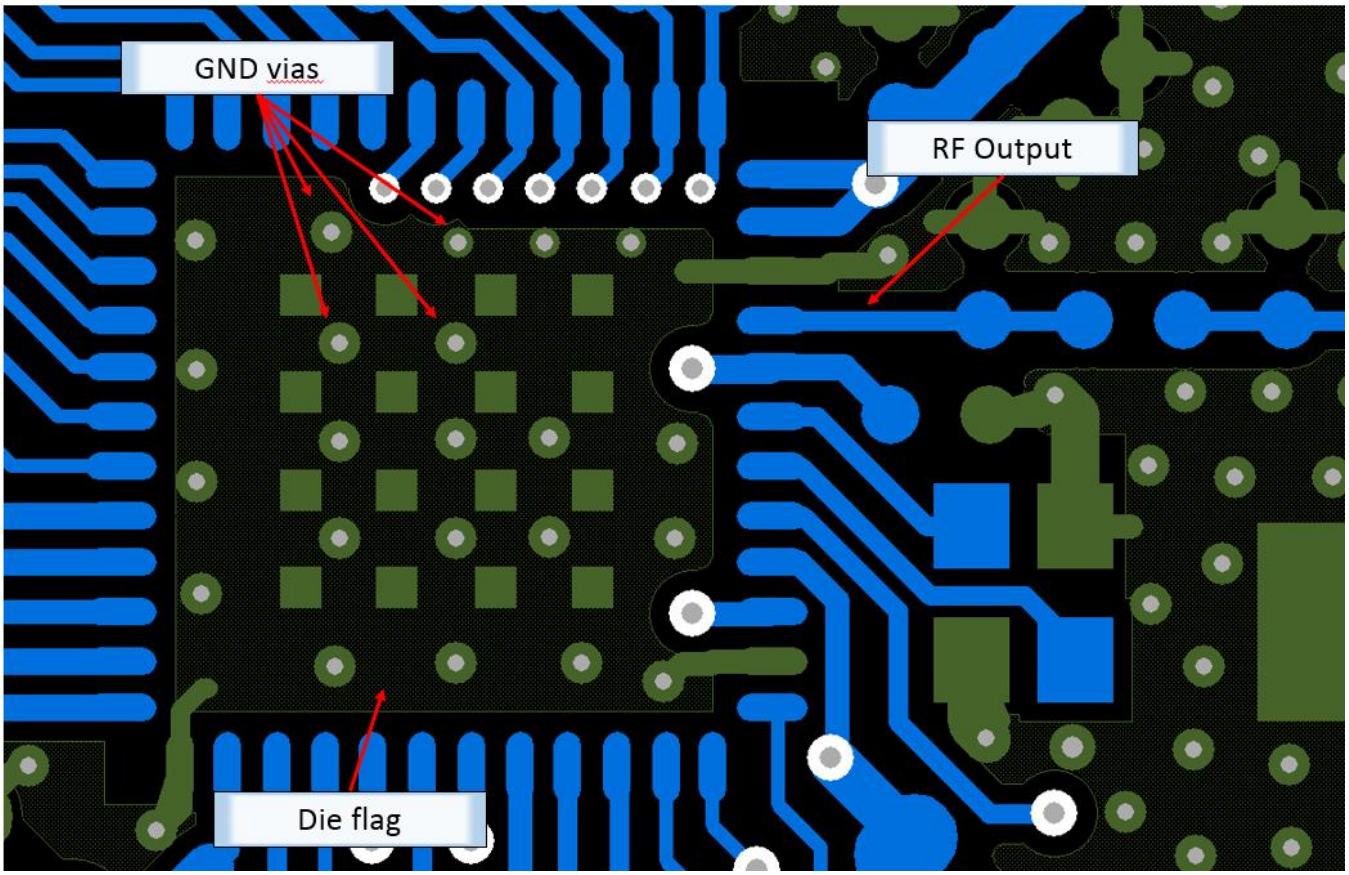


Figure 9. Critical layout of die flag area

Figure 9 shows the critical areas of the device die flag, as below:

- Ground vias and locations
- RF output and ground traces
- Die flag shape

6.1.1. GPIOs

The GPIOs traces are generally long lines that can cover long distances. They can carry undesirable signals that are likely to radiate in any direction.

On some of the KW41Z boards that require a complex routing due to the large number of GPIOs it has been observed that the PTC lines sometimes carry a spurious signal at twice the LO frequency.

To avoid this specific spurious frequency to be radiated, it is recommended to add footprints for shunt capacitors to GND on PTC1 and PTC2 traces close to the chip pins. In case a 2*LO signal is unintentionally radiated, it can be attenuated by populating these capacitors that must have a self-resonant frequency around 4.8 to 5 GHz. The value of the capacitors will depend on the model and manufacturer; one possibility is the 3 pF Murata capacitor GRM1555C1H3R0.

An alternative to these 3 pF shunt capacitors is to bury the sensitive GPIOs in layer 3 in order that the GND plane in layer 2 acts as a shield and avoids unwanted spurious to be radiated.

Figure 10 is an example of how the PTC lines can be routed on the top layer:

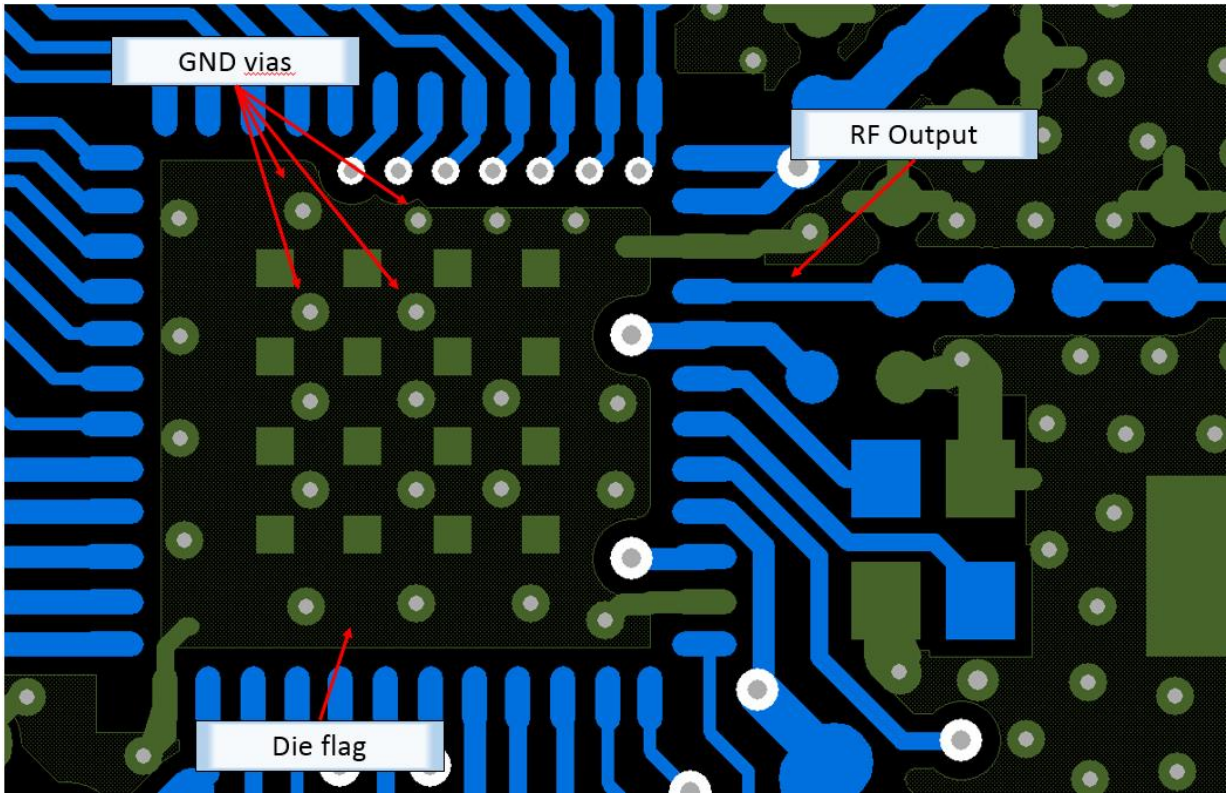


Figure 10. Routing and placement of key PTC lines decoupling capacitors

6.2. RF circuit implementation

It is important to understand that the antenna pin of the KWx1Z connects to its antenna via a transmission line, not just a standard trace. Transmission lines can take on different shapes such as microstrip, coplanar waveguide, and stripline. For BLE and 802.15.4 applications built on FR4 substrates, the types of transmission lines typically take the form of microstrip or coplanar waveguide (CPW). These two structures are defined by the dielectric constant of the board material, trace width, and the board thickness between the trace and the ground.

Additionally, for CPW, the transmission line is defined by the gap between the trace and the top edge ground plane. These parameters are used to define the characteristic impedance of the transmission line (trace) that is used to convey the RF energy between the radio and the antenna.

KW41 has a single ended RF output with a 2-component matching network composed of a shunt capacitor and a series inductor. These two elements transform the device impedance to 50 ohms. The value of these components may vary depending on your specific board layout. The recommended RF-matching network is shown in *Figure 11*.

Avoid routing traces near or parallel to RF transmission lines or crystal signals and keep the RF trace as short as possible. Maintaining a continuous ground under an RF trace is critical to maintaining the characteristic impedance of that trace. Avoid any routing on the ground layer that will result in disrupting the ground under the RF traces.

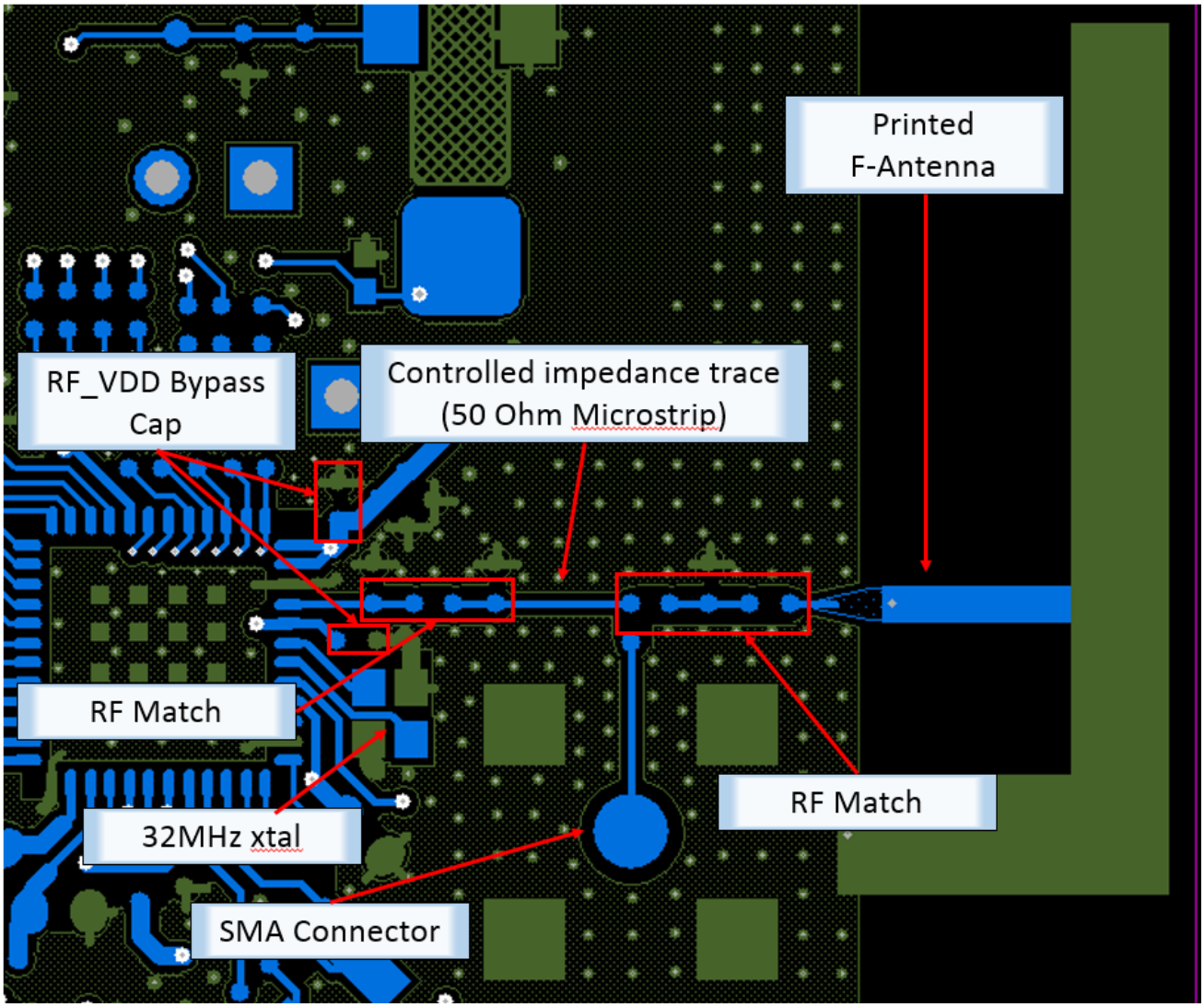


Figure 11. RF matching network

6.3. Layout and PCB stack-up

6.3.1. Reference oscillator

Route the connections from the 32 MHz XTAL to the chip oscillator pins with traces as short as possible.

The XTAL should be placed away from high frequency devices and traces to reduce the capacitive coupling between XTAL pins and PCB traces.

Keep other digital signal lines, especially clock lines and frequently switching signal lines, as far away from the crystal connections as possible.

6.3.2. GND planes

It is recommended to use a solid (continuous) ground plane on Layer 2, assuming Layer 1 (top) is used for the RF components and transmission lines; avoid cut-outs or slots in that area.

Keep top ground continuous as possible. This also applies for the other layers.

Connect ground on the components layer to the ground plane beneath with a large quantity of vias.

Ground pours or "fingers" can act as antennas that unintentionally radiate. To avoid this, eliminate any finger that is not connected to the ground reference with a via; put a via in any trace that "doesn't go anywhere".

6.3.3. Layer interconnections

Avoid vias in the RF traces. Typically for a 1.6mm thickness PCB material, a single via can add 1.2 nH of inductance and 0.5 pF of capacitance, depending upon the via dimensions and PCB dielectric material.

Provide multiple vias for high current and/or low impedance traces.

Connect carefully all the ground areas of any layer to the reference GND plane.

6.3.4. PCB stack-up

Complexity is the main factor that will determine whether the design of an application board can be 2-layer, 4-layer, or more. From an RF point of view a 4-layer PCB is preferred to a 2-layer PCB. Nevertheless, in a very simple application, it should be possible to use a 2-layer PCB.

The recommended board stackup for either a 4-layer or 2-layer board design is as follows:

- 4-layer stackup:
  - Top: RF routing of transmission lines
  - L2: RF reference ground
  - L3: RF reference ground
  - Bottom: Signal routing
- 2-layer stackup:
  - Top: RF routing of transmission lines, signals, and ground
  - Bottom: RF reference ground, signal routing, and general ground

It is important to copy not just the physical layout of the circuit, but also the PCB stackup. This information can be found on the fabrication notes for each board design. Even minor changes in the thickness of the dielectric substrate under the transmission line will have a significant change in impedance. As an illustration, consider a 50-ohm microstrip trace that is 18 mils wide over 10 mils of FR4. If that thickness of FR4 is changed from 10 to 6 mils, the impedance will only be about 36 ohms.

In any case, the width of the RF lines must be re-calculated according to the PCB characteristics to ensure a 50-ohm impedance.

When the top layer dielectric becomes too thin, the layers will not act as a true transmission line; even though all the dimensions are correct. There is not universal industry agreement on which thickness at which this occurs, but NXP prefers to use a top layer thickness of no less than 8-10 mils.

There is also a limit to the ability of PCB fabricators to control the minimum width of a PCB trace and the minimum thickness of a dielectric layer. A tolerance of ±1 mil will have less impact on an 18-mil-wide trace and a 10-mil-thick dielectric layer, than on a much narrower trace and thinner top layer.

This can be an especially insidious problem. The design will appear to be optimized with the limited quantity of prototype and initial production boards, in which the bare PCB's were all fabricated in the same lot. However, when the product goes into mass production, there can be variations in PCB fabrication from lot-to-lot which can degrade performance.

The use of a correct substrate, like the FR4 with a dielectric constant of 4.3, will assist you in achieving a good RF design.

6.4. Components

All electronic components have parasitic characteristics that cause the part to act in a non-ideal way. Typically, these effects become worse as the frequency of operation is increased.

For most component suppliers, this quality is expressed by the Self Resonant Frequency (SRF) specification. For example, a capacitor has parasitic inductance introduced by the metal leads of the components. As frequency increases, at some point the impedance due to the parasitic inductance is greater than the impedance of the capacitor, and at that frequency and higher, the component no longer acts as a capacitor and now acts as an inductor. At the point at which the impedance from both inductive and capacitive components is the same, the part will resonate as a LC parallel resonant circuit, and this is called the Self Resonant frequency. *Figure 12* shows a typical response curve.

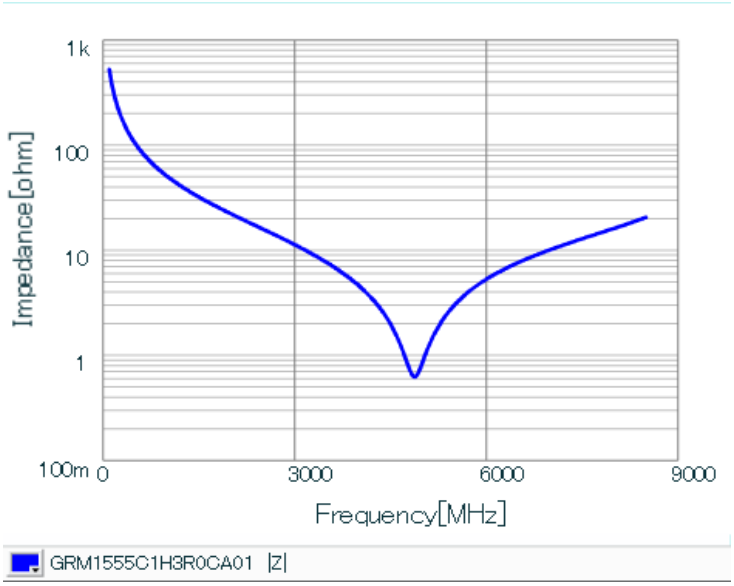


Figure 12. RF plots for 0402 3pF ceramic capacitor (Murata GRM1555 type)

The same is true of inductors. There is parasitic capacitance in an inductor, mainly due to capacitive coupling between the turns of wire. At some point in frequency, this capacitance will have a higher impedance than the inductance of the part. From this frequency and higher the part acts as a capacitor and not as an inductor.

The Bill Of Materials (BOM) is available for all NXP reference designs. The BOM shows the specific vendors and part numbers used on NXP designs. It is certainly possible to substitute another vendor's parts, but it may impact the performance of the circuit, therefore, it may be necessary to use different component values when parts from another vendor are used.

If there is a performance issue on a new design, and part substitutions were made on that design, then it is strongly recommended that components identical to those used in the NXP reference design be placed on the new design for test purposes. Once the design is working properly with components that are identical to those used by NXP, then it will be possible to substitute components from other vendors one at a time, and test for any impact on circuit performance.

6.5. Antenna considerations

There are a large variety of antenna types available to choose from when designing for a wireless system. These include small footprint chip antennas, trace antennas, loop monopole, and dipole, each with their own set of pros and cons depending on the goal of the application. NXP recommends using one of the proven antenna implementations used in many of our hardware reference designs. For more information on compact antenna designs, see AN2731.

Steps for good antenna performance:

- Be mindful of critical dimensions:
  - Critical dimensions should be copied exactly.
  - Customer final board sizes may differ from the NXP reference designs. As a result, the last leg of the trace antenna should be made longer or shorter to allow for final board tuning.
  - Antenna tuning may be required to operate at the proper frequency. Ideally, the minimum return loss needs to be centered at 2445 MHz. 10 dB return loss looking into the antenna at the band edges is sufficient to achieve good range and receive sensitivity.
- Antenna impedance is 50 ohms.
  - This is maintained from balun to antenna feed.
  - The example uses microstrip topology but co-planer waveguide with ground can also be used if desired. In this case, the dimensions will change, so take care when changing from one topology to another.
- The antenna should be reasonably clear of metallic objects and oriented properly with the ground plane.
- Always check the antenna in its final environment, including the PCB, components, case enclosure, hand effects (if appropriate), and battery. Plastic and other materials in the near-field may cause detuning.
- Actual antenna performance can be evaluated in a variety of ways, such as range testing, measuring radiated signal level under controlled conditions, and characteristic testing in an anechoic chamber.

6.6. Power supply layout considerations

6.6.1. General considerations

Decouple the power supplies or regulated voltages as close as possible to the supply pin of the IC. The decoupling capacitors must be connected to a localized ground pad on the top layer that is connected to the main ground plane layer through multiple vias.

Ensure that each decoupling capacitor has its own via connection to ground. When possible, use 2 vias to connect the capacitor to the ground layer.

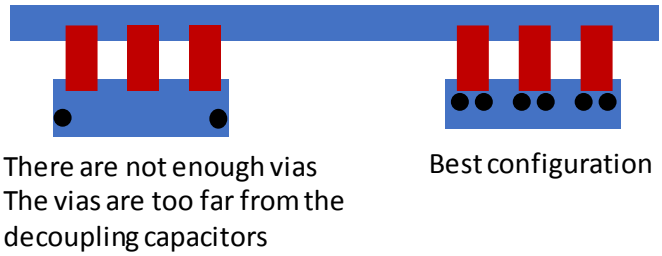


Figure 13. Decoupling capacitor via layout

The capacitor with a smaller capacitance must be placed nearer to the IC.

The decoupling capacitor must be placed between the main supply line and the supply pin, as shown in *Figure 14*.

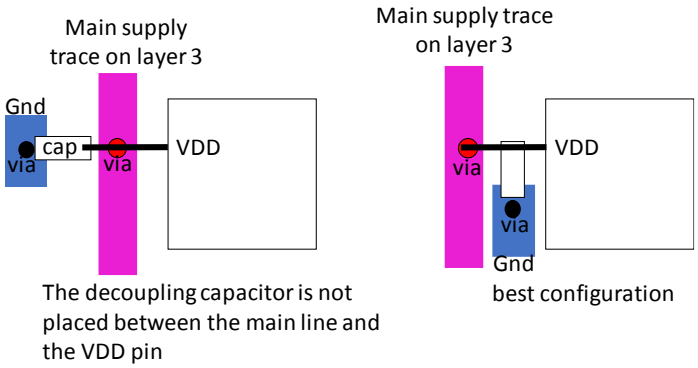


Figure 14. Decoupling capacitor placement configuration

6.6.2. DCDC inductor

If using the on-board DCDC converter of the KW41Z, an inductor will be required in the design. Proper inductor layout is required. The copper area between the pads of the inductor can often be "finger" shaped. As such, this area can act as an antenna and be susceptible to coupling noise into the design from other sources, or radiating noise generated by the KW41Z. Vias must be added in the GND trace between the two ends of the 10 uH inductor (L12) to prevent these undesired effects. *Figure 15* demonstrates an example.

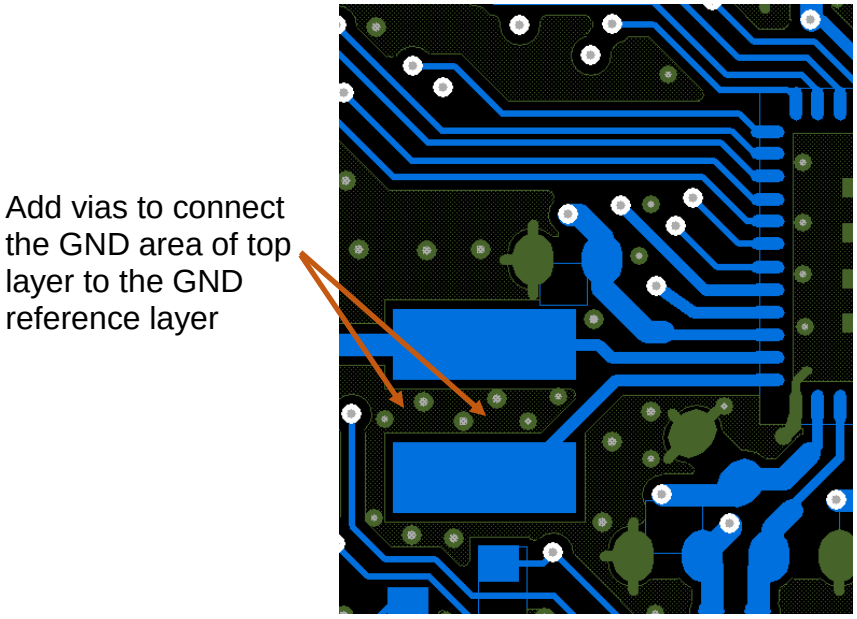
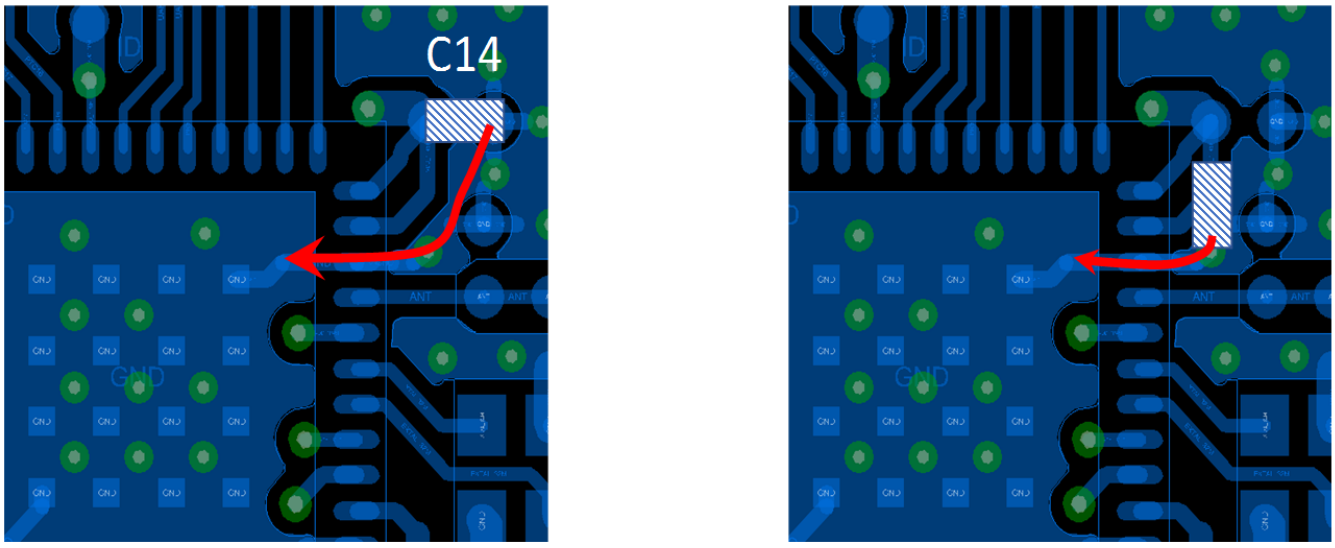


Figure 15. DCDC inductor layout with vias

6.6.3. VDD_RF1 & VDD_RF2 decoupling

On the FRDM-KW41Z, the pins VDD_RF1 and VDD_RF2 use a common decoupling capacitor (C14). This capacitor must be connected to the GND in such a way that the connection to the die flag is as short as possible.



Example of **unoptimized** capacitor placement.

Example of **optimized** capacitor placement.

Figure 16. VDD_RF pin decoupling capacitor placement

7. Revision history

Table 1. Sample revision history

Revision number	Date	Substantive changes
0	11/2016	Initial release
1	03/2017	**Figure 6** updated
2	12/2017	**Figure 5** updated and **Appendix A** added

Appendix A. Additional supporting tools

- www.nxp.com/KW41Z_DESIGN_CHECKLIST
- www.nxp.com/KW31Z_DESIGN_CHECKLIST
- www.nxp.com/KW21Z_DESIGN_CHECKLIST

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