

# Beyond DSPs

Giving Customers Another Choice

INCLUDING

StarCore MSC8xxx and  
DSP56K Families  
(Including Symphony  
Audio DSPs)

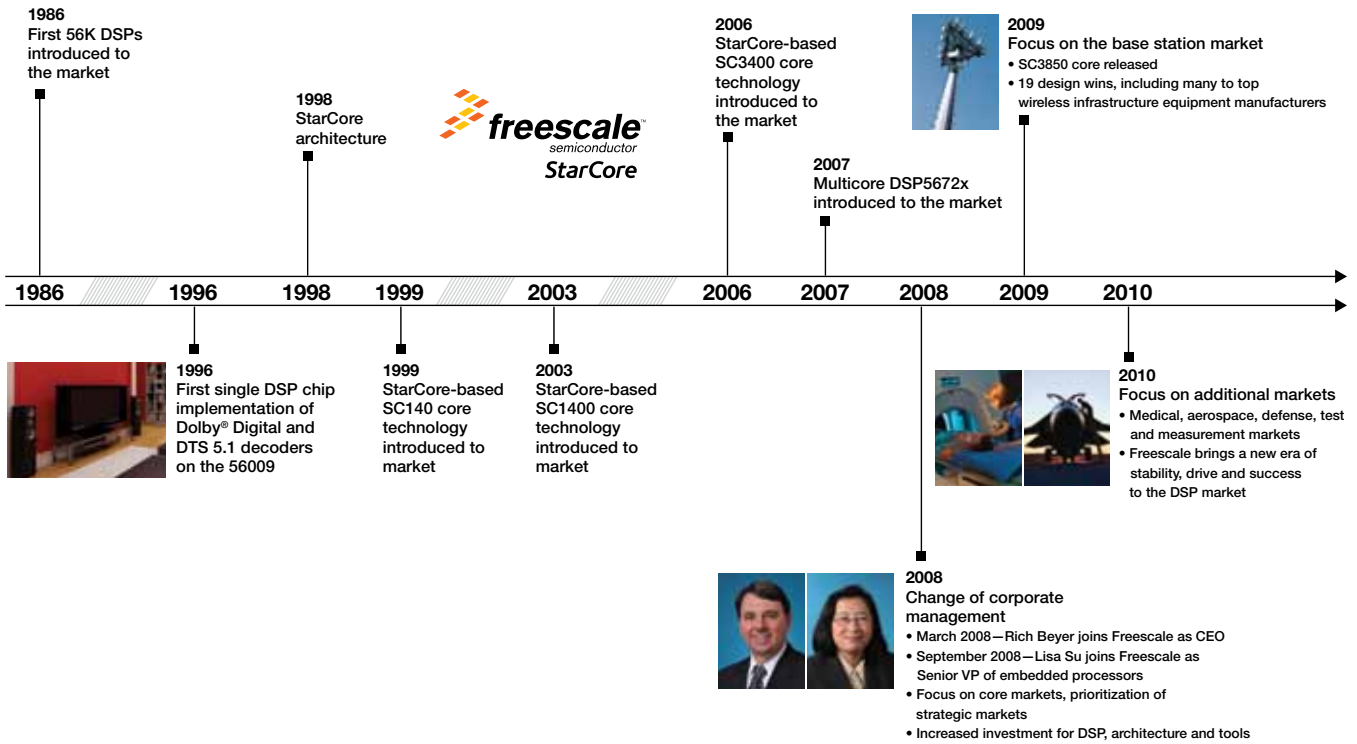
# Beyond DSPs

## Table of Contents

|   |           |
|---|-----------|
| <b>History of Freescale/Motorola DSPs</b>                               | <b>2</b>  |
| <b>Technical Highlights: A closer look at the StarCore DSP families</b> | <b>3</b>  |
| MSC815x and MSC825x Family Overview .....                               | 4         |
| StarCore DSP Roadmap .....  | 6         |
| SC3850 Core .....   | 7         |
| DSP Core Subsystem .....  | 9         |
| MAPLE-B .....   | 11        |
| CLASS Fabric .....  | 12        |
| RISC-Based QUICC Engine Subsystem .....                                 | 13        |
| Serial RapidIO® Architecture .....                                      | 14        |
| PCI Express® Controller .....   | 15        |
| DDR2/3 .....  | 16        |
| Time-Division Multiplexing.....   | 17        |
| <b>Application Solutions</b>  | <b>18</b> |
| Wireless Base Stations .....  | 19        |
| Video .....   | 20        |
| Voice .....   | 22        |
| Medical Imaging.....  | 24        |
| Aerospace and Defense .....   | 26        |
| Advanced Test and Measurement .....                                     | 28        |
| <b>Development Software, Tools and Reference Designs</b>                | <b>30</b> |
| CodeWarrior Development Studio for StarCore 10.0 DSPs.....              | 31        |
| Voice Software .....  | 32        |
| Video Software .....  | 32        |
| Base Station Software .....   | 33        |
| MSC8156 Evaluation Module .....   | 35        |
| MSC8156ADS .....  | 37        |
| MSC8156AMC .....  | 39        |
| P2020—MSC8156 AdvancedMC™ Reference Design .....                        | 41        |
| <b>Technical Highlights: A closer look at the DSP56K families</b>       | <b>43</b> |
| DSP56K Family Overview .....  | 44        |
| DSP56K Core .....   | 45        |
| Application Solutions.....  | 48        |
| <b>DSP56K Family Development Software, Tools and Reference Designs</b>  | <b>49</b> |
| Development Software .....  | 50        |
| DSPAUDIOEVM Evaluation Module .....                                     | 51        |
| Symphony SoundBite Development Kit .....                                | 52        |
| DSP563xx Evaluation Module (DSP563xxEVME) .....                         | 54        |
| Additional Resources .....  | 56        |
| Ecosystem Partners .....  | 56        |

This document contains information on a new product. Specifications and information herein are subject to change without notice.

## Freescale DSP Evolution



# History of Freescale/Motorola DSPs

Freescale Semiconductor (under the Motorola brand) introduced our first DSP to the market in 1986 with the introduction of the general purpose digital signal processors (DSPs) based on the 56K architecture. The 56K general purpose DSPs evolved into an extensive family of embedded DSPs, including 56K DSPs with integrated audio software called the Symphony DSP line. These DSPs remain popular across a wide range of applications, including audio and industrial control. Due to the very large customer base and continued popularity of these products, we will be releasing new 56K products in 2011.

In 1998, Freescale introduced the high-performance StarCore architecture to the broad market. In 2008, Rich Beyer joined Freescale as CEO and Lisa Su was appointed Senior Vice President for embedded processors. They recognized the growth potential in DSP markets and substantially increased investments in the StarCore DSP architecture and tools. This increased investment in StarCore has resulted in the highest performance DSPs on the market today. Initially, the base station market was the primary focus for high-performance StarCore DSPs. In 2009, the SC3850 core was released as the building block core of the MSC8156 six-core high-performance DSP. The MSC8156 has been an overwhelming success in the base station market with 17 major design wins, including eight of the top 10 wireless infrastructure equipment companies.

In 2010, the focus for the StarCore DSPs expanded with the introduction of the MSC825x family and the MSC8152/ MSC8251 broad market DSPs. These new products are targeted for process intensive applications in the video, voice, medical, aerospace, defense and test and measurement markets and provide the optimal blend of cost effectiveness and high performance throughput.





# Technical Highlights

A closer look at the  
StarCore DSP families

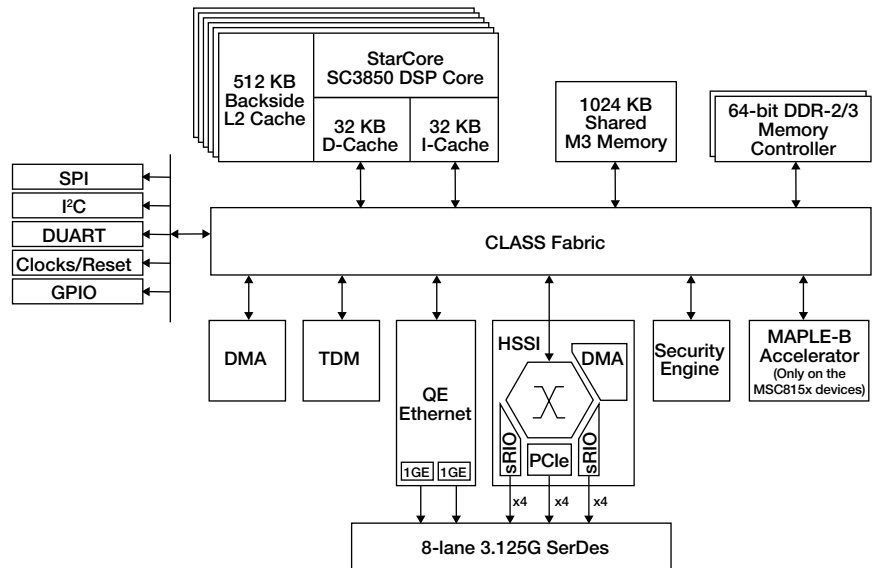


# MSC815x and MSC825x Family Overview

The MSC815x and MSC825x families of DSPs are based on the industry's highest performance DSP core, built on StarCore technology, and designed for the advanced processing requirements and capabilities of today's high-performance, high-end industrial applications for the video, voice, medical imaging, aerospace, defense and advanced test and measurement markets.

By leveraging the 45 nm process technology in a highly integrated SoC, the MSC815x and MSC825x families of DSPs deliver industry-leading performance and power savings. These DSPs are based on SC3850 StarCore technology. The SC3850 DSP core has earned leading benchmark results from independent signal-processing technology analysis firm Berkeley Design Technology, Inc. (BDTI). Specifically, Freescale's SC3850 1.2 GHz core registered a fixed-point BDTIsimMark2000™ score of 18,500—the highest score of any DSP architecture tested by BDTI to date. The combination of the award-winning SC3850 core and the richest and highest performance DSP peripherals available serve to accelerate system performance and result in a family of DSPs that offer up to twice the performance of competitors' parts.

**MSC815x and MSC825x Family**



Despite being the highest performing DSP available in the broad market today, these DSPs are also extremely price competitive. Starting at \$75 USD MSRP, the MSC815x and MSC825x DSP families offer the industry's best value and integration and may save customers up to one million USD over the product's lifetime in processor cost. In addition to silicon savings, pin and peripheral compatibility across the

MSC815x and MSC825x families helps to enable software and tool reuse, allowing scalability from a single-core device to multicore devices, or to create multiple products from the same hardware.

## Pin for Pin Compatibility

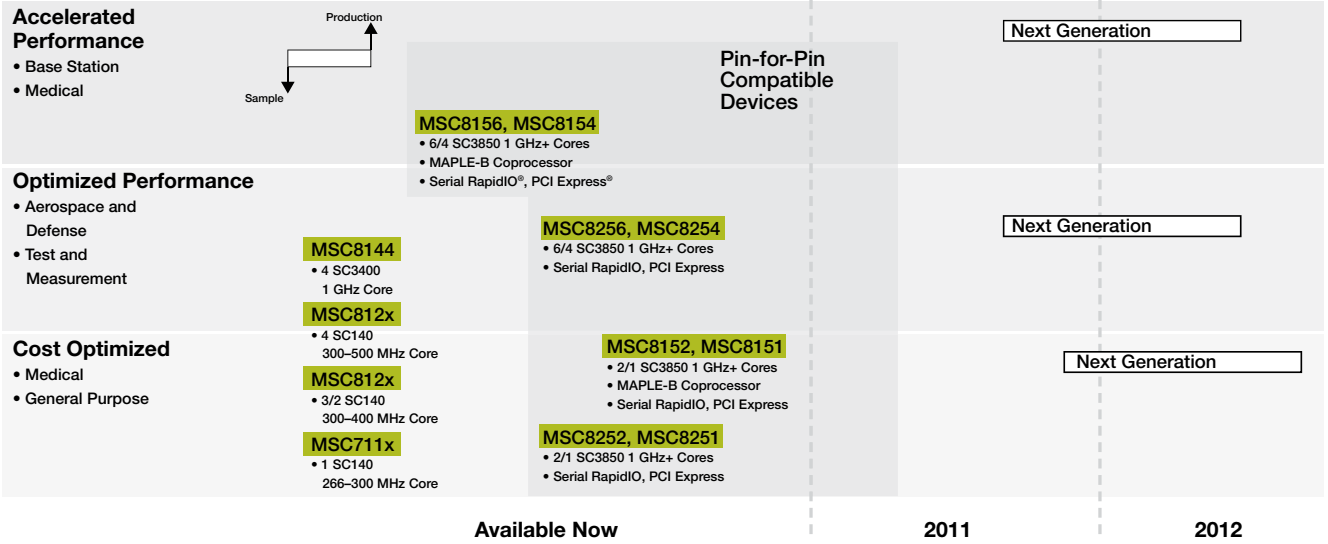
| Device                             | MSC8156             | MSC8154        | MSC8152        | MSC8151    | MSC8256             | MSC8254          | MSC8252        | MSC8251    |
|------------------------------------|---------------------|----------------|----------------|------------|---------------------|------------------|----------------|------------|
| SC8350 DSP Cores                   | 6                   | 4              | 2              | 1          | 6                   | 4                | 2              | 1          |
| Core Speed (MHz)                   | 1 GHz               | 1 GHz          | 1 GHz          | 1 GHz      | 1 GHz<br>800 MHz    | 1 GHz<br>800 MHz | 1 GHz          | 1 GHz      |
| Core Performance<br>(16-bit MMACs) | Up to<br>48000      | Up to<br>32000 | Up to<br>16000 | Up to 8000 | Up to<br>48000      | Up to<br>32000   | Up to<br>16000 | Up to 8000 |
| Shared M3 Memory                   | 1 MB                |                |                |            | 1 MB                |                  |                |            |
| I-Cache (per core)                 | 32 KB               |                |                |            | 32 KB               |                  |                |            |
| D-Cache (per core)                 | 32 KB               |                |                |            | 32 KB               |                  |                |            |
| L2 I-Cache (per core)              | 512 KB              |                |                |            | 512 KB              |                  |                |            |
| DDR2/3                             | 2 (800 MHz)         |                |                |            | 2 (800 MHz)         |                  |                |            |
| PCI Express®                       | 1                   |                |                |            | 1                   |                  |                |            |
| GEMAC (RGMII, SGMII)               | 2                   |                |                |            | 2                   |                  |                |            |
| Serial RapidIO®                    | 2                   |                |                |            | 2                   |                  |                |            |
| TDM                                | 4                   |                |                |            | 4                   |                  |                |            |
| SPI                                | 1                   |                |                |            | 1                   |                  |                |            |
| UART                               | 1                   |                |                |            | 1                   |                  |                |            |
| I <sup>2</sup> C                   | 1                   |                |                |            | 1                   |                  |                |            |
| Turbo/Viterbi Accelerators         | 1                   |                |                |            |                     |                  |                |            |
| FFT/DFT/CRC Accelerators           | 1                   |                |                |            |                     |                  |                |            |
| Processor Technology               | 45 nm               |                |                |            | 45 nm               |                  |                |            |
| Package                            | 783 Ball<br>FC-PBGA |                |                |            | 783 Ball<br>FC-PBGA |                  |                |            |

## Key Features and Benefits

- The MSC815x and MSC825x DSPs deliver a high level of performance and integration, combining one, two, four or six new and enhanced, fully programmable SC3850 cores, each running at up to 1 GHz.
- The MSC815x family has added performance from a multi-accelerator platform engine (MAPLE-B) for fast Fourier transforms (FFT), inverse fast Fourier transforms (iFFT), discrete Fourier transforms (DFT), inverse discrete Fourier transforms (iDFT) and Turbo and Viterbi decoding.
- A high-performance internal RISC-based QUICC Engine subsystem supports multiple networking protocols to help provide reliable data transport over packet networks while significantly offloading processing from the DSP cores. TCP/IP stack control via the integrated QUICC Engine coprocessor allows fast communication between FPGA and DSP to DSP.
- Comprehensive memory support includes two 64-bit DDR3 running at 800 MHz to enable fast system throughput for multicore DSPs, GPP capability with an integrated MMU and full ECC protection on all memories.
- A rich peripheral set includes two Serial RapidIO® (four lane) interfaces, two Gigabit Ethernet interfaces for network communications, a PCI Express® x4 interface and four multi-channel TDM interfaces.
- The system is tied together with high-speed, high-bandwidth chip-level arbitration and switching fabric (CLASS). The CLASS is a non-blocking, fully pipelined, low latency fabric interconnect based on a single module and therefore has uniformity in data transfer.
- Supports industrial temperature grade: -40°C to +105°C junction.

# StarCore DSP Roadmap

## StarCore DSP Roadmap



Freescale is no stranger to multicore DSP design. From the StarCore inception in 1998, we are on our fourth generation of StarCore cores and our third generation of multicore DSPs with additions to the StarCore family already in development. We offer cost-effective, high-performance DSPs to meet the performance requirements of process-intensive applications such as medical imaging or voice communications. The new MSC825x and MSC815x DSPs are the world's first DSPs available in the 45 nm process technology.

## Freescale Product Longevity

Freescale has a longstanding track record of providing long-term production support for our products. Freescale is pleased to provide a formal Product Longevity Program for the market segments we serve. For market segments in which Freescale participates, Freescale will make a broad range of devices available for a minimum of 10 years. Life cycles begin at the time of launch.

The MSC815x, MSC825x and 5672x families of DSPs are included in the Product Longevity Program. For terms and conditions and to obtain a list of available products, visit [freescale.com/productlongevity](http://freescale.com/productlongevity).



# SC3850 Core

The SC3850 DSP core features an innovative architecture that addresses the performance requirements of today's processing intensive DSP applications. This flexible DSP core supports compute-intensive applications by providing high performance, low power, efficient compilation and high code density. Each high-performance core is binary compatible with previous generations of StarCore technology.

Performing eight MACs per cycle, the SC3850 core delivers up to 8000 16-bit MMACS using an internal 1 GHz clock at 1V. Operation includes a multiply-accumulate command with associated data movements and pointer updates.

The StarCore SC3850 DSP core and subsystem is an evolution of the StarCore SC3400 DSP core and subsystem that enhances many of the original core and subsystem components and optimizes overall performance and memory hierarchy to target future application needs.

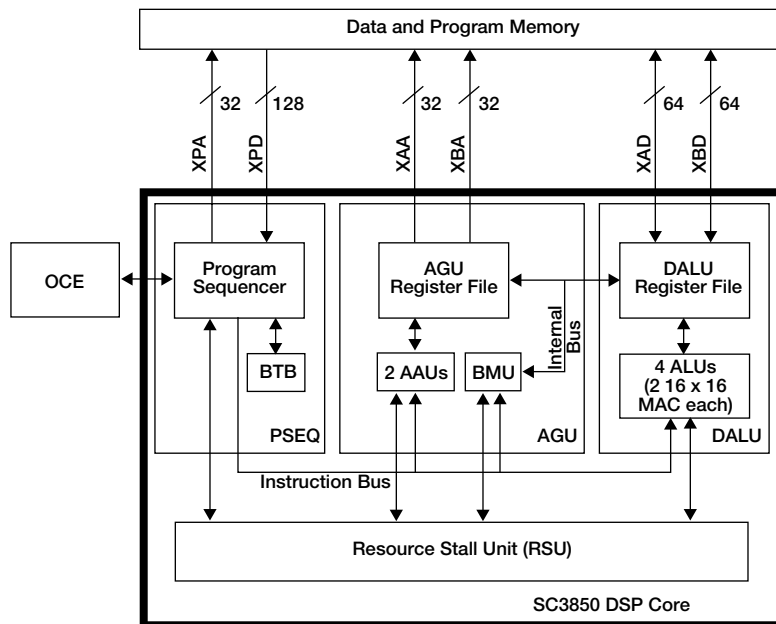
## SC3850 Benefits

- Improved control/compiled code performance
- Better operation of DSP intensive kernels
- Minimizing memory system stalls to increase core use

## Key Features

- Main core resources
  - Four data ALU execution units
  - Two integer and address generation units
  - 16 40-bit data registers with eight guard bits, freely accessible by data ALU instructions

## SC3850 DSP Core Block Diagram



- 16 32-bit address registers, freely accessible by address generation instructions
- Instruction set
  - 16-bit instruction set, expandable to 32 and 48 instructions
  - High orthogonality of operands
  - Rich instruction set for DSP and control features
  - Good compiler target
- Very high execution parallelism
  - Up to six instructions executed in a single clock cycle, statically scheduled
  - Variable length execution set (VLES) execution model
  - Up to four data ALU instructions and two memory access/integer instructions per cycle
- Data type support
  - Byte (8-bit), word (16-bit) and long (32-bit) data widths, supported by instructions and memory moves
  - Both integer (signed and unsigned) and fractional data types
  - Packed fractional complex data type
  - Several packed data types (two to four objects on the same register) for SIMD operations
- Very high numerical throughput for DSP operations
  - Each data ALU can perform two 16 x 16 multiplications per cycle (total of eight multiplications for all ALUs), which can be used for:
    - Dot product acceleration (40 + (16 x 16) + (16 x 16))
    - SIMD2 multiplication and accumulation into two 20-bit register portions
    - Acceleration of complex multiplication
    - Acceleration of extended precision multiplication



- Application specific instructions for acceleration of the following algorithms:
  - FFT
  - Video processing
  - Viterbi
  - Baseband operations
- High throughput memory interface
  - Unified, 32-bit byte addressable memory space
  - Dual Harvard architecture that permits one 128-bit program access and two 64-bit data accesses per cycle
  - Core to data memory throughput of up to 16 GB per second, at 1 GHz core frequency
  - Support of Big Endian, Little Endian and Mixed Endian memory policies
- Zero overhead modulo arithmetic support for address pointers
- Advanced pipeline
  - 12-stage, fully interlocked pipeline
  - No stalls for memory load to register MAC operation and result storage
  - Speculation of conditionally executed instructions and change of flow execution paths
- Control features
  - Zero-overhead hardware loops with up to four levels of nesting
  - A branch target buffer (BTB) for accelerating execution of change of flow instructions
- OS support
  - Precise memory exception support for advanced OS
  - User and supervisor privilege levels, supporting a protected, task-oriented execution model
  - Full support for memory protection and address translation in the off-core memory management unit
  - Exception and normal stack pointer for software stack support
  - Low task switch overhead using wide stack save and restore instructions
- Rich set of real-time debug capabilities through an on-chip emulator (OCE)
  - Real-time PC, data address and data breakpoint capabilities
  - Up to six hardware breakpoint channels and unlimited debugger-enabled software breakpoints
  - Single stepping
  - Externally forced instructions in debug mode by the host processor
  - Precise detection of PC breakpoints
  - PC tracing with filtering and compression options
  - Support for Nexus IEEE-ISTO 5001-2003™ standard with off-core ready modules
- Low-power design
  - Low-power wait and stop instructions
  - Fully static logic

TheSC3850 DSP core technology achieved a BDTI<sub>sim</sub>Mark2000 score of 18,500—the highest score of any DSP architecture tested by BDTI to date. This score exceeds the BDTI<sub>mark</sub>2000 score of 16,690 previously set by Texas Instrument's 1.2 GHz C66X DSP.

# DSP Core Subsystem

Each SC3850 core is embedded in a DSP subsystem that enhances the power of the SC3850 core and provides a simple interface to each SC3850 core.

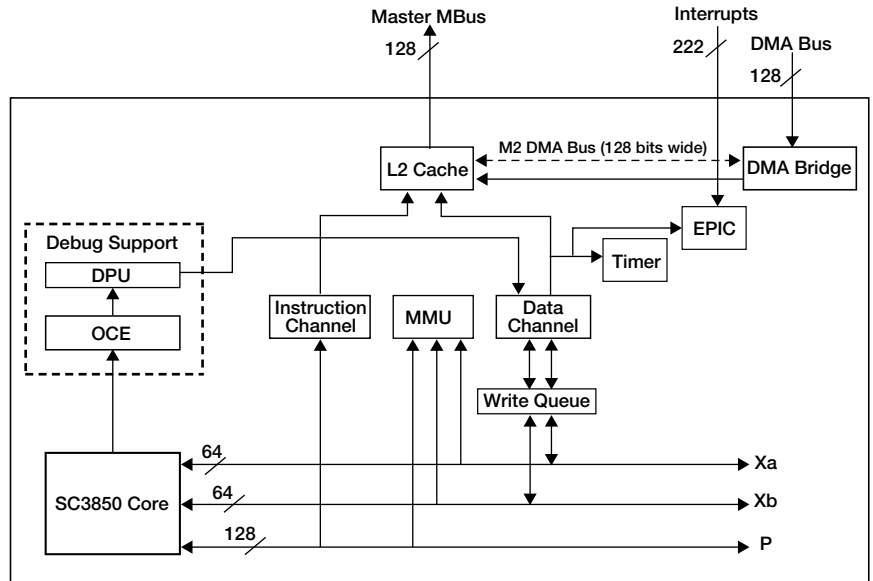
The DSP core subsystem includes:

- An SC3850 core
- Instruction channel with a 32 KB instruction cache that supports advanced prefetching
- Data channel built around a 32 KB data cache, which supports advanced prefetching
- Memory management unit (MMU) for task protection and address translation
- Unified 512 KB L2 cache with partitioning support for multitasking reconfigurable in 64 KB partitions as M2 memory
- Write queue that interfaces between the core and the data channel
- Dual timer for internal use (such as RTOS)
- Extended programmable interrupt controller (EPIC) supporting 256 interrupts
- Real-time debug support with the OCE and a debug and profiling unit (DPU)

The subsystem has the following units and distinctive features:

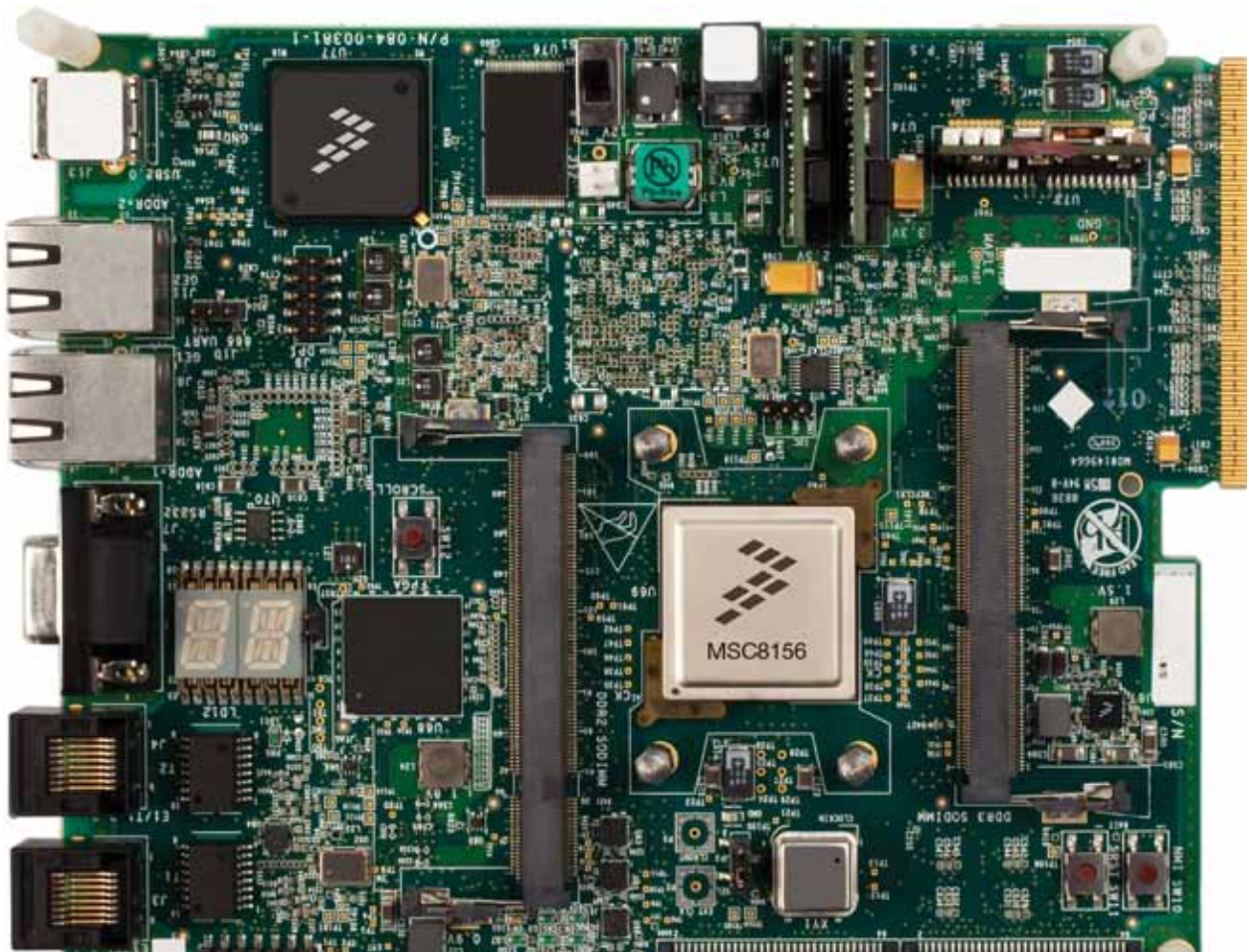
- Instruction cache
  - 32 KB
  - Eight ways with 16 lines per way
  - Multi-task support
  - Real-time support through locking flexible boundaries
  - Prefetch capability
  - Software coherency support (sweep)
  - PFETCH touch loading instruction support

## DSP Subsystem Block Diagram



- Data cache
  - 32 KB
  - Eight ways with 16 lines per way
  - Can serve two data accesses in parallel (XA, XB)
  - Multi-task support
  - Real-time support through locking flexible boundaries
  - Software coherency support (Cache ISA or sweep)
  - Write-back writing policy
  - Write-through writing policy
  - Hardware line prefetch capability
  - Cache performance ISA support (DFETCH touch loading and DMALLOC)
- MMU
  - Virtual to physical address translation
  - Task protection
  - Defines the memory and access attributes of memory regions
- Unified L2 cache
  - 512 KB
  - Eight ways with 1024 indices
  - 64-byte line size
  - Physically addressed
  - Maximum user flexibility for real-time support through address partitioning of the cache
  - Rich cache policy support
  - Multi-channel, two-dimensional software prefetch support
  - Software coherency support with seamless transition from L1 cache coherency operation
  - External memory interface
  - MBus unified address separate data bus, with 32-bit address and 128-bit data
  - Supports asynchronous clock ratio

- Debug and profiling
  - On-chip emulator (OCE) for core-related debug and profiling support
  - Debug and profiling unit (DPU) for subsystem level debug and profiling support
  - Debug state, single stepping and command insertion from the host debugger
  - Breakpoints on PC, data address and data bus values
  - More than 40 event counting options in six parallel counters
  - Cache debug mode enabling observation of the cache state (cache array, tags, valid and dirty bits, etc.) and to change the contents of the data cache array
  - Real-time tracing of PC, task ID and profiling information to the main memory
- Interrupt handling
  - Extended programmable interrupt controller (EPIC) to handle 256 interrupts, including from internal sources
  - Supports 222 interrupts external to the MSC8156 SC3850 DSP subsystem, independently configured as maskable or non-maskable
  - 32 priority levels for interrupts
  - Asynchronous and synchronous interrupts
- Two general-purpose 32-bit timers for RTOS support
- Low-power design modes of operation
  - Wait processing state, where the clocks of the core and caches are gated but peripherals operate
  - Stop processing state for full clock gating



# MAPLE-B

The MAPLE-B is an algorithm accelerator for Turbo, Viterbi, FFT/iFFT, DFT/iDFT and CRC algorithms. It consists of a programmable system interface (PSIF), controller with CRC accelerator, DMA capabilities and three accelerators attached using an IP interface.

- Turbo/Viterbi processing element: Performs up to 200 Mbps of Turbo decoding (six iterations) or up to 115 Mbps of K=9 (zero tail) Viterbi decoding
- FFT processing element: FFT and iFFT for sizes 128, 256, 512, 1024 or 2048 points at up to 350 million samples per second
- DFT processing element: DFT and iDFT for sizes up to 1536 points at up to 175 million samples per second

The PSIF has two 64-bit wide MBus master ports used to transfer input and output data to and from system memory and a 64-bit MBus slave port that allows any host to access its internal memories. Hosts access internal memories to perform the following functions:

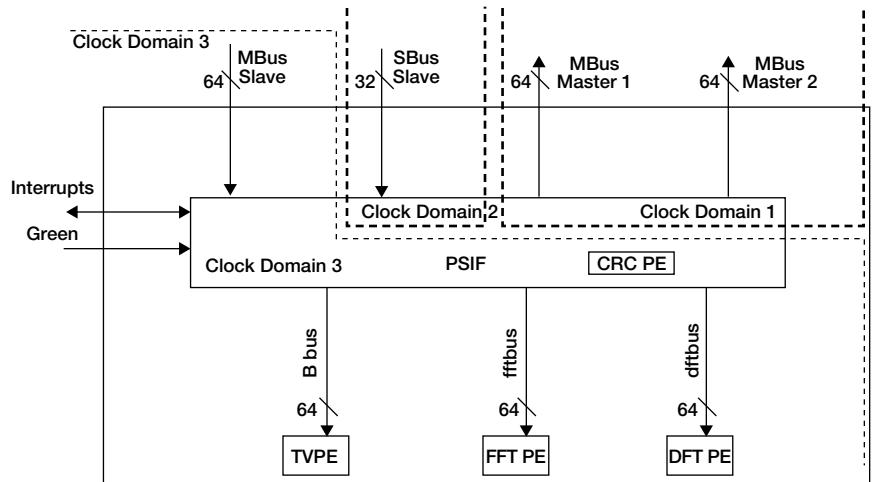
- Place buffer descriptors in the PSIF internal memory
- Access the MAPLE-B parameter RAM
- Access the processing element registers

The PSIF internal registers are accessed using the SBus.

The four accelerator processing elements include the following:

- Turbo/Viterbi Processing Element (TVPE)
- FFT processing element (FFTPE)
- DFT processing element (DFTPE)
- CRC processing element (CRCPE)

## MAPLE-B



Highlights of the MAPLE-B include:

- Software-friendly buffer descriptor-based handshake and task assignment with minimal overhead on DSP cores for control
- Runs at 450 MHz
- Highly flexible and programmable Turbo and Viterbi decoder supporting various configurable decoding parameters (polynomials, rate, binary/duo, tail bit, zero tail)
  - Up to 200 Mbps of Turbo decoding for low latency and advanced antenna systems or up to 100 Mbps of K=7 tail bit multi-iteration Viterbi decoding for low latency data/control channels decoding
  - Support for WCDMA, CDMA2K, WiMAX and 3G-LTE standards
  - CB CRC (LTE) or APQ (all standards) Turbo decoding stopping criteria for low power/low latency and higher statistical system capacity
  - Rate de-matching, HARQ support accelerated
- Flexible and advanced FFT/DFT acceleration:
  - FFT/iFFT for sizes 128, 256, 512, 1024, 2048 points at up to 280 Msps
  - DFT/iDFT for LTE sizes at up to 175 Msps
  - In 10 MHz WiMAX case up to 350 Msps of 1024 points FFT
- High-speed CRC calculation/check accelerator for:
  - LTE code and transport block in UL and DL
  - WiMAX PHY burst CRC in UL and DL

# CLASS Fabric

The chip-level arbitration and switching system (CLASS) is the central internal interconnect system for the MSC815x and MSC825x DSP families. The CLASS is a non-blocking, full-fabric interconnect that allows any initiator to access any target in parallel with another initiator-target couple. The CLASS uses a fully pipelined low latency design and demonstrates per-target prioritized round-robin arbitration, highly optimized to the target characteristics.

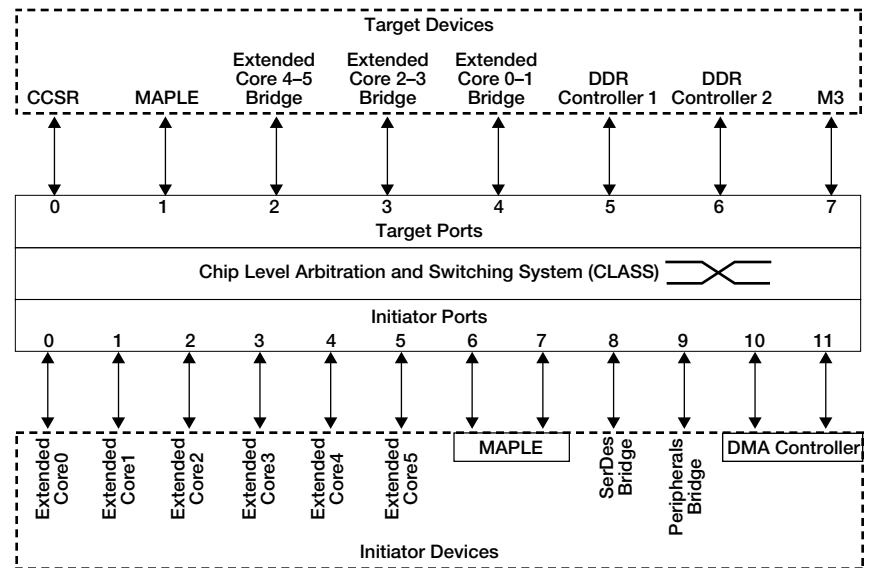
The CLASS operates at 500 MHz (half the SC3850 core speed). The CLASS clock is separate from the SC3850 core clock to provide an optimized trade off between power dissipation, memory technology and miss latency. Controlling the intradevice data flow, the CLASS reduces bottlenecks and permits high bandwidth fully pipelined traffic.

The CLASS is ready for use and does not require any special configuration to perform non-blocking pipelined transactions from any initiator to any memory.

The CLASS modules implement the following features:

- Non-blocking, full-fabric interconnect
- Full bandwidth utilization toward each target
- Allows full pipeline when a specific initiator accesses a specific target
- Allows full pipeline when accesses are generated by one or more initiators to specific targets
- Read transactions can have a maximum pipeline of 16 acknowledged requests before completing the transaction toward the initiator

## CLASS Fabric



- Write transactions can have a maximum pipeline of three acknowledged requests before completing the transaction toward the initiator
- Programmable priority mapping
- Programmable auto priority upgrade
- Address decoding for target selection and multi target demultiplexing
  - Programmable address space start/end registers per target for flexible address decoding (resolution of 4 KB). Not supported in the reduced configuration option
  - Fixed priority between address decoding results, allowing overlapping and deduction of address windows
- Per-target arbitration algorithm
  - Four-level prioritization
  - Each level implements pseudo round-robin arbitration algorithm
  - Weighted arbitration
  - Optimized data bus utilization mode
- Programmable masking priority for starvation elimination
- Multiplexing the initiator buses according to the arbitration winner
- Normalizing mode that splits non-aligned transactions according to the target capabilities (maximal burst size, power-of-2 burst, burst alignment, full size burst, data-beat alignment, wrap size)
- Error detection and handling
  - The CLASS identifies illegal addresses addresses that do not belong to any of the address windows or fall inside the negative windows
  - The CLASS stores the illegal address, reports the error and generates an interrupt
- Debug and profiling unit (CDPU) support



# RISC-Based QUICC Engine Subsystem

The QUICC Engine subsystem is a versatile RISC-based communication processor that supports multiple external interfaces and protocols independently from the core processor(s) in an integrated processing device.

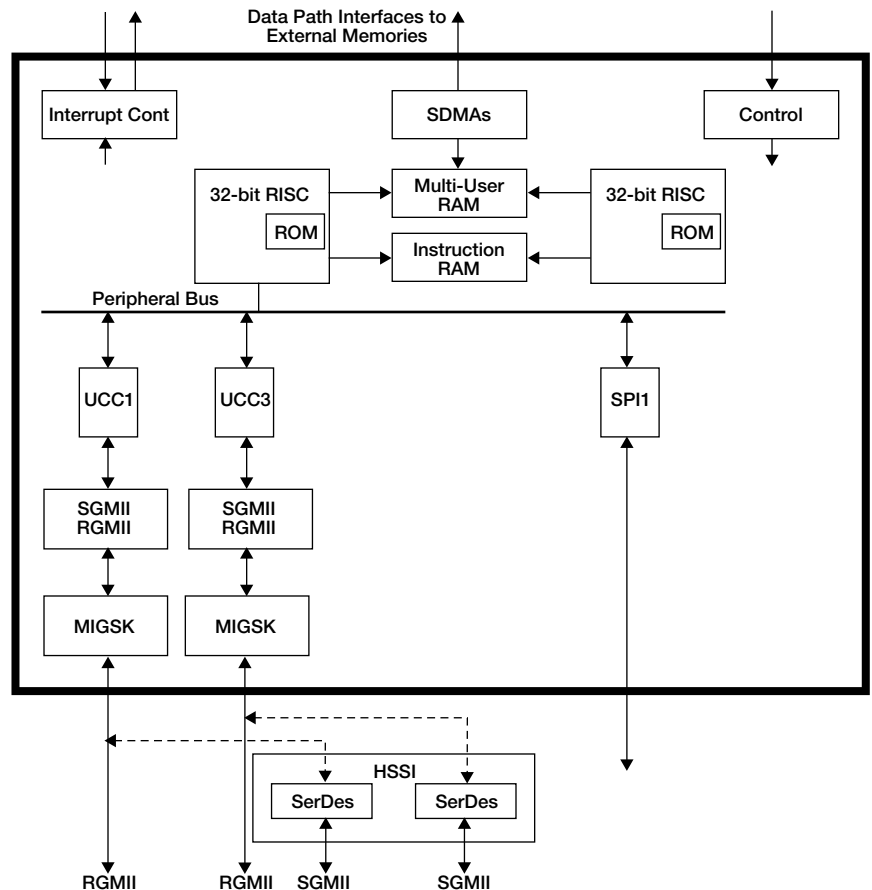
In the MSC815x and MSC825x, the QUICC Engine includes two Gigabit Ethernet controllers (supporting both RGMII and SGMII interfacing) and one SPI interface. With the QUICC Engine block, packet processing up to and beyond layer 4 (TCP/UDP) can be offloaded from the SC3850 cores. This allows the cores to be relieved of the data transfer and handling overhead commonly associated with Ethernet tasks.

QUICC Engine packet processing allows the programmer to create multiple independent data and control flows between each core and each QUICC Engine Ethernet controller enabling the flexibility of both symmetric and asymmetric multicore processing models.

The QUICC Engine can be clocked at up to 500 MHz, and is comprised of:

- Dual RISC engines
  - Internal interfaces to the core and peripherals
  - Parameter RAM
  - Buffer descriptors
  - Multi-threading operation
  - Serial numbers
  - Instruction RAM (IRAM)
- Serial DMA controller
- Clocking
  - Signal multiplexing
  - Baud-rate generation
- Dedicated interrupt controller with interrupt signals for each MSC815x core
- Two programmable unified communication controllers (UCCs), each of which provides dedicated support for an Ethernet controller for RGMII/SGMII interfaces
  - Supports lossless flow control and PAUSE flow control for full duplex operation
    - Transmit flow control via a host command
    - Automatic transmit flow control according to programmable receive FIFO thresholds
    - Programmable MAC parameter in flow control frame
  - Full collision support
  - Framing support for single and multi-buffered Ethernet frames
- Serial management interface MDC/MDIO
- Transmitter network management and diagnostics
- Receiver network management and diagnostics
- Enhanced MIB statistics
- Frame filtering and address recognition
- VLAN support
- IEEE® Std. 802.1p/Q QoS support
- Serial peripheral interface (SPI)

## RISC-Based QUICC Engine



# Serial RapidIO® Architecture

The RapidIO architecture provides high data bandwidth, low-latency capability, and support for high-performance I/O devices. The MSC815x and MSC825x parts include a Serial RapidIO architecture that supports two ports, a RapidIO message unit (RMU) and two RapidIO DMA units. The Serial RapidIO ports comply with the RapidIO Interconnect Specification, Revision 1.2, which supports 1x/4x operation up to 3.125 Gbaud.

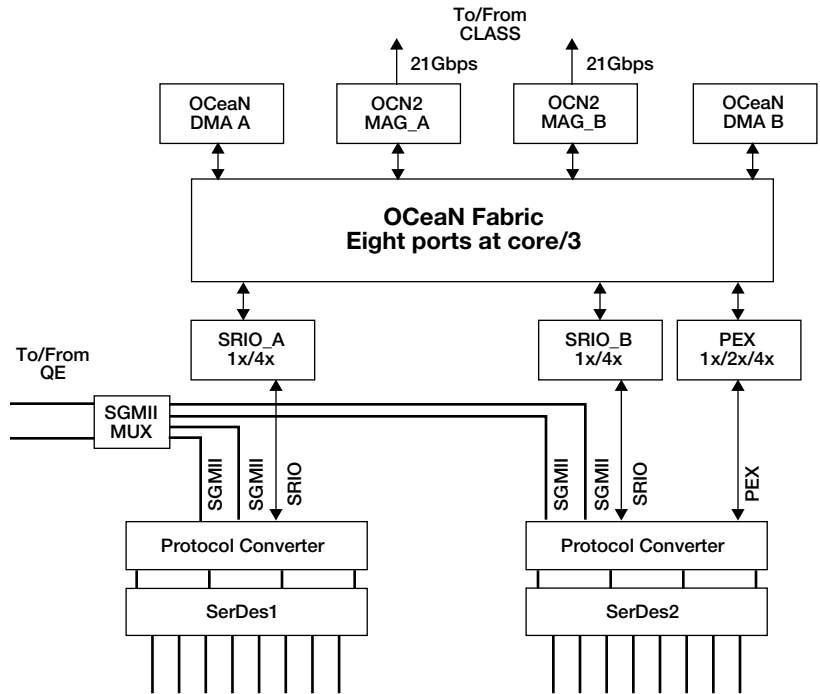
The MSC815x and MSC825x devices can either connect directly to a host or a Serial RapidIO switch. Packets ready for processing are sent from the host to the MSC815x/825x device and the processed packets are sent back to the host. Each Serial RapidIO port supports read, write, messages, doorbells and maintenance accesses. The RapidIO DMA units are used for NWRITE, NWRITE\_R, NREAD and SWRITE operations, while the RMU controls message and doorbell operations. The buffers in the Serial RapidIO endpoints support packets up to 256 bytes.

The two Serial RapidIO ports can be configured to perform pass-through operations between them. This connectivity allows packets to be forwarded to the next device connected to the second RapidIO port.

## Features

- Two Serial RapidIO ports supporting 1x/4x operation up to 3.125 Gbaud with a RapidIO messaging unit and two RapidIO DMA units

### Serial RapidIO®



- Each Serial RapidIO port supports read, write, messages, doorbells and maintenance accesses
  - Small and large transport information field only
  - Priority flow
  - Pass-through between the two ports that allows cascading devices using the Serial RapidIO and enabling message/data path between the two Serial RapidIO ports without core intervention. A message/data not designated for the specific device passes through to the next device
- RapidIO messaging unit supports:
  - Two outbound message queues
  - Two inbound message queues
  - One outbound doorbell queue
  - One inbound doorbell queue
  - One inbound port-write queue
- Each RapidIO DMA unit supports:
  - Four high-speed/high-bandwidth channels accessible by local and remote masters
  - Basic DMA operation modes (direct, simple chaining)
  - Extended DMA operation modes (advanced chaining and stride capability)
  - Programmable bandwidth control between channels
  - Up to 256 bytes for DMA sub-block transfers to maximize performance over the RapidIO interface
  - Three priority levels supported for source and destination transactions

# PCI Express® Controller

The PCI Express® controller supports communication with PCI Express devices connected to the MSC815x or MSC825x devices for high-bandwidth data transfers. It complies with the PCI Express Base Specification, Revision 1.0a and connects to a 2.5 GHz serial interface configurable for up to a x4 interface.

The PCI Express controller can be configured to operate as either a root complex (RC) or an endpoint (EP) device. As an RC device, the PCI Express controller connects the core and memory subsystem to I/O devices and configures the EP devices during device discovery and enumeration. It can also act as an initiator and a target device. As an initiator, the PCI Express controller supports memory read and write operations with a maximum transaction size of 256 bytes. As a target interface, the PCI Express controller accepts read

and write operations to local memory space. When configured as an EP device, the PCI Express controller accepts configuration transactions to the internal PCI Express configuration registers. Message generation and acceptance are supported in both RC and EP modes.

The address translation mapping unit (ATMU) maps transactions from the MSC815x or MSC825x devices to the PCI Express controller as a memory, I/O, message or configuration transaction via translation windows. Transactions from the PCI Express controller are mapped to the MSC815x/MSC825x internal platform via inbound translation windows. For outbound transactions, the MSC815x/MSC825x supports four translation windows and one default window. For inbound transactions, the MSC815x/MSC825x supports three inbound windows and one configuration window.

## Features

- Complies with the PCI Express Base Specification, Revision 1.0a
- Supports root complex (RC) and endpoint (EP) configurations
- 32- and 64-bit address support
- x4, x2 and x1 link support
- PCI Express configuration registers (type 0 in EP mode, type 1 in RC mode)
- 256 byte maximum payload size
- ATMU
- Three inbound general purpose translation windows and one configuration window
- Four outbound translation windows and one default window
- Supports eight non-posted and four posted PCI Express transactions
- Credit-based flow control management
- Supports PCI Express messages and interrupts

# DDR2/3

The MSC815x and MSC825x DSP families support two DDR controllers for external memory expansion. The DDR SDRAM interface is useful when an application requires additional code or data storage to supplement the internal M2 or M3 memory.

The DDR controllers can interface with JEDEC-compliant 8- or 16-bit DDR2 or DDR3. The data bus interface is 64/72 or 32/40 bits wide. Each controller supports two physical bands or chip selects to

provide up to a maximum 1 GB of DDR space for each controller. Discrete, unbuffered and registered dual rank memory modules (DIMMs) are supported.

Built-in error checking and correcting (ECC) protection ensures reliable operation. When ECC is enabled, the DDR memory controller corrects all single-bit errors and detects all double-bit errors within the 64-bit or 32-bit data bus.

The memory interface supports voltages of 1.5V (SSTL\_15) for DDR3 and 1.8V (SSTL\_18) for DDR2. Accesses to memory are burst oriented, with support for burst length of eight for DDR3 and burst length of four for DDR2. For DDR3, on-chip ZQ calibration is supported to adjust output driver and on-die termination impedance. DDR3 also supports write leveling to compensate for the flight time skew delay with respect to the strobe and clock signals.

| Features/Category        | DDR2  | DDR3  |
|--------------------------|---|---|
| <b>Package</b>           | <b>BGA</b>  | <b>BGA</b>  |
| Densities                | 256 MB to 8 GB  | 512 MB to 8 GB  |
| Voltage                  | 1.8V core and I/O   | 1.8V core and I/O   |
| I/O Signalling           | SSTL_18   | SSTL_15   |
| Internal Memory Banks    | 4 to 8  | 8   |
| Data Rate                | Up to 800 Mbps  | Up to 800 Mbps  |
| Termination              | On-die termination for data group, VTT termination for address, command and control | On-die termination for data group, VTT termination for address, command and control. Supports dynamic ODT |
| Data Strokes             | Differential (recommended) or single-ended  | Differential  |
| Burst Length             | BL-4, 8 (4-bit prefetch)  | BL-8 (Burst chop4) 8-bit prefetch   |
| CL/tRCD/tRP              | 15 ns each  | 12 ns each  |
| Master Reset             | No  | Yes   |
| ODT (On-Die Termination) | Yes   | Yes   |
| Driver Calibration       | Off-chip (OCD)  | On-chip with ZQ pin (ZQ calibration)  |
| Leveling                 | No  | Yes   |
| Interface Data Bus Width | 32/40-bit and 64/72-bit   | 32/40-bit and 64/72-bit   |
| DIMM Support             | Discrete, unbuffered and registered 64 MB through 8 GB                              | Discrete, unbuffered and registered 64 MB through 8 GB and mirrored DIMMS                                 |
| Full ECC Support         | Single error correction/detection, double error detection                           | Single error correction/detection, double error detection   |
| Self Refresh Support     | Yes   | Yes   |

# Time-Division Multiplexing

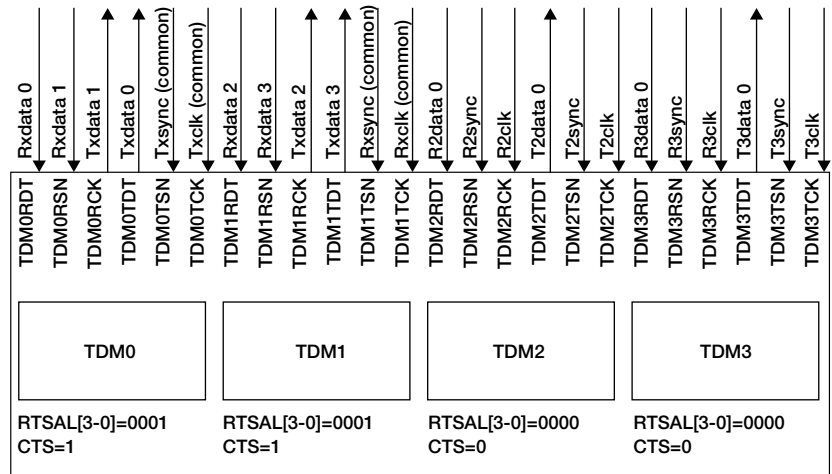
The time-division multiplexing (TDM) interface provides a glueless connection to most E1/T1 framers as well as to common buses such as the ST-Bus. The TDM interface is composed of four identical TDM modules, each supporting 256 bidirectional channels running at up to 62.5 Mbps. Time slot sizes can be configured to 2, 4, 8 or 16 bits. A hardware A-law/ $\mu$ -law conversion is supported for 8-bit channels.

Each TDM module can operate in independent or shared mode. In independent mode, the transmit and receive have separate clock, frame sync and data links with up to 256 transmit channels and up to 256 receive channels. In shared clock and sync mode, the clock and frame sync signals are shared between the two receive data links and two transmit data links. Each of the two transmit and data links support up to 128 channels. In shared data link mode, up to four full-duplex data links share the same clock and frame sync. Each link supports up to 128 channels.

## Features

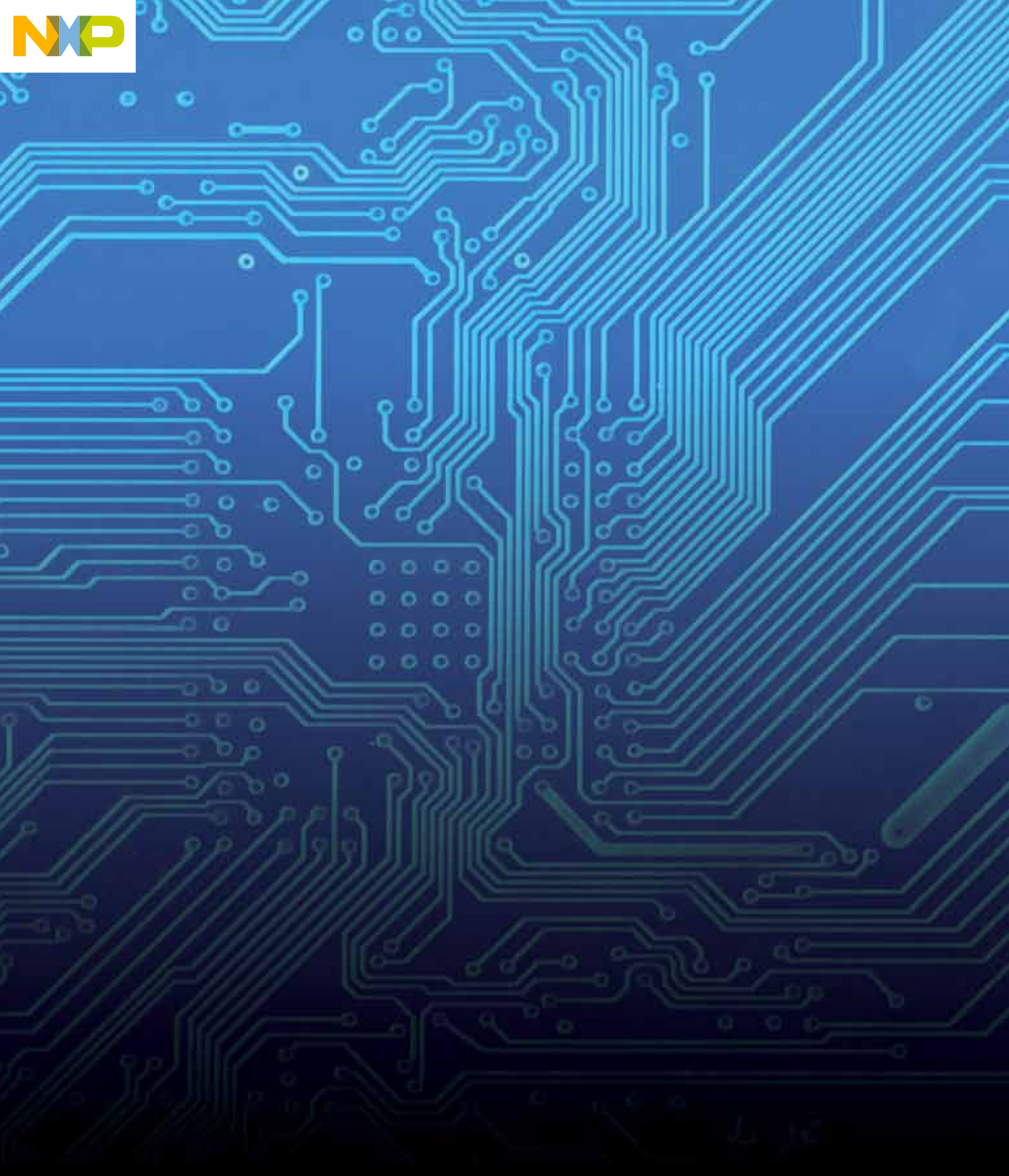
- Four independent TDM modules. Together, the four TDM modules support up to 1K time slots for receive and 1K time slots for transmit

**TDM Modules Diagram**



- Independent receive and transmit mode
- Shared sync and clock mode
- Shared data link
- 2-, 4-, 8- or 16-bit word size. All channels share the same size
- Hardware A-law/ $\mu$ -law conversion
- Up to 62.5 Mbps data rate per TDM module
- Up to 16 MB per channel buffer where A/ $\mu$  law buffer size has double size
- Separate or shared interrupts for receive and transmit
- Each channel can be programmed as active or inactive
- Support for either 0.5 ms (4 frames) or 1 ms (8 frames) latency
- Glueless interface to E1/T1 framers





# Application Solutions

# Wireless Base Stations

The MSC8156 and MSC8154 high-performance StarCore DSPs are the perfect solution for the industry's need for the very highest performance in multicore baseband DSPs. With up to 6 GHz DSP core performance, this fully programmable advanced DSP subsystem offers up to 48 GMACs (8- or 16-bit) of processing performance. This performance is proven by successful deployments of the MSC8156 at several of the top wireless infrastructure OEMs.

Code compatibility with the previous generation MSC8144 DSP ensures seamless software migration to the new MSC8156 DSPs.

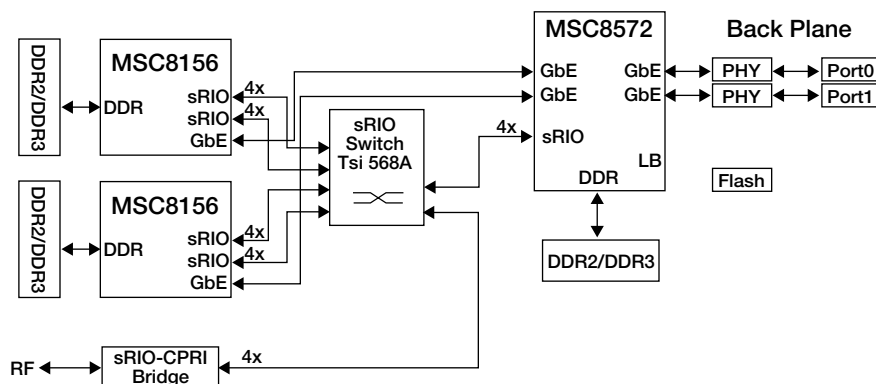
Additional value drivers for the base station market include:

- Control code efficiency at GPP level
- Low latency memory hierarch
- High-throughput, low-latency baseband accelerators
- Advanced high-speed interfaces pertinent to different systems topologies
- High speed/wide external DDR interfaces
- Drives a low BOM channel card

## 3G-LTE, Single Sector 20 MHz Channel Card

- 20 MHz use case, 4 x 4 DL and 2 x 2 UL MIMO
- Suitable for UL SIMO and basic UL MIMO schemes
- Peak data rates per sector are assumed to be 300 Mbps DL/150 Mbps UL as supported by category 5 type user equipment with multi-user UL MIMO
- One MSC8156 device allocated to UL processing

### 3G-LTE, Single Sector 20 MHz Channel Card



- One MSC8156 device allocated to DL processing
- sRIO switch for full connectivity between devices, with option to remove sRIO switch using pass through feature (TBV)
- Small front-end bridge needed in case of CPRI/OBSAI backplane

## WiMAX Three Sector 10 MHz Channel Card

- Three sectors 10 MHz
- Downlink: Four Tx antenna, beamforming, 100 Mbps max per sector
- Uplink: Eight Rx antenna, 14 Mbps max per sector
- Serial RapidIO switch for full connectivity between devices, with option to remove Serial RapidIO switch using pass-through feature (TBV)
- Small front-end bridge needed in case of CPRI/OBSAI backplane

# Video

High-definition video applications requiring superb video quality and support for scalable solutions are best served by the MSC825x DSP family coupled with Freescale's extensive off-the-shelf codec libraries.

Freescale was first to introduce a fully featured 1080P30 HD H.264/SVC embedded solution supporting temporal, spatial and quality scalability, available for free download and evaluation. SVC, together with over 30 video, audio and voice codecs, running on the high-performance MSC825x devices, enables a variety of high-end video applications.

Key advantages of Freescale's hardware and software solutions for video applications:

- Highest performing multicore DSP platform available with the ability to support HD H.264/SVC and other advanced codecs
- Programmable DSP and software codecs allow customers to add proprietary code and tweak solution to best suit the target market
- Rich device peripherals: Dual 4x Serial RapidIO, 4x PCI Express and dual Gigabit Ethernet allow flexible multi-device system solutions and seamless connectivity to FPGAs or other system components
- 2x DDR3 at 800 MHz for high data rate video applications
- 2-, 4- and 6-core, pin-compatible devices for scalable system solutions
- All codecs scale to support multiple streams of lower resolution with no performance degradation
- H.264/SVC, H.264BP, MPEG-4, MPEG-2, G.729, AAC and many other video, voice and audio components available from Freescale or ecosystem partners
- Freescale video and audio production codecs are shipping in today's leading media products

## Videoconferencing

MSC825x devices, together with the rich media codec libraries, are well suited for videoconferencing applications and their H.264/SVC, high video quality and system flexibility requirements.

Freescale's software codecs support low delay encoding and decoding required in videoconferencing applications and maintain high quality at low bitrates. The support of fully featured SVC further assists when combating unreliable networks or network bottlenecks by use of the scalability options for maintaining a high quality video transmission.

Rich device peripherals allow seamless connectivity to other system components, such as FPGA or a host processor, and also allow for multi-device solutions required in videoconferencing MCUs.

Freescale offers a rich portfolio of video software technologies, including H.264 baseline profile running at 1080p30 and legacy support for H.263/MPEG-4. Please contact your Freescale representative for more information.

## Multipoint Control Unit

The videoconferencing multi-point control unit is a key element in modern videoconferencing systems, enabling interoperability and communication between participants using a wide variety of end point terminals. The multi-point control unit, often referred to as a bridge, establishes conference calls between three or more people for converged video, voice and data conferences.

MSC825x is used for performing encode, decode and other image processing functions required in the multi-point control unit.

Serial RapidIO and PCI Express high bandwidth interfaces enable transfer of raw video data between devices in multi-device solutions that are prevalent in videoconferencing infrastructure systems.

Rich software codec libraries allow interoperability of participants connecting with advanced and legacy end-points and enable maximum flexibility in MCU design with no performance degradation for support of lower resolution streams.



## Videoconferencing End Point (EP)

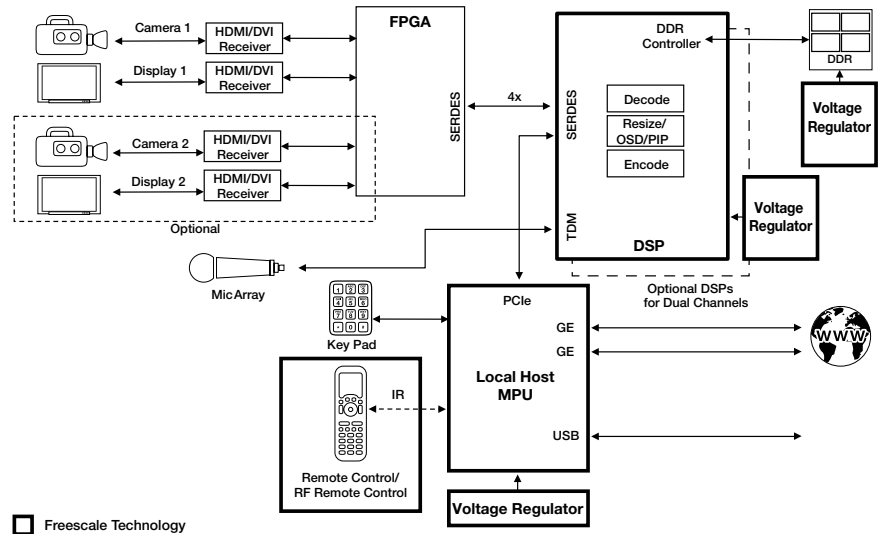
Videoconferencing end point (EP) systems are used to make video-enabled calls between two participants (point to point) or multiple participants (multi point). A typical EP will feature at least one HD camera and one screen while high-end (telepresence) systems will include three HD cameras and three large screens to better emulate a face to face meeting and an additional data channel. Processing elements in the EP must perform at least a single encode and decode of HD video and additional image processing functions, such as image resize and on-screen display. High-end room systems require multiple simultaneous encodes and decodes at frame rates up to 60 frames per second.

MSC825x is used for performing the encode, decode and other image processing functions connected on the one end via PCIe interface to an FPGA for image capture and display and on the other end to a host processor for network connectivity. Based on specific system requirements, one or more DSP devices can be used to perform the multiple encode and decode functions while utilizing the high bandwidth Serial RapidIO ports for inter-device connectivity.

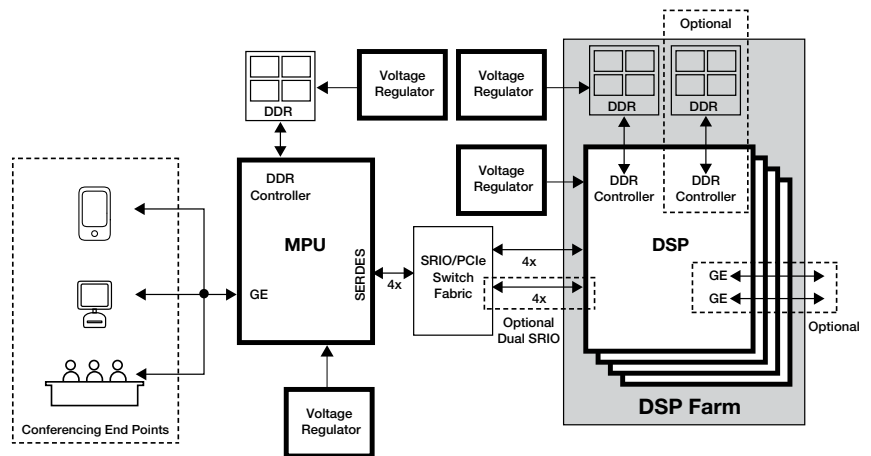
## Media Gateway

Please refer to media gateway application section on page 23.

### Room System and Telepresence Videoconferencing End Point



### Enterprise IP-PBX Block Diagram





# Voice

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VoIP (Voice over IP) is becoming a more frequently utilized technology as customers discover its cost and quality benefits. As the communications industry completes the migration from circuit-switched to packet-switched infrastructure, equipment manufacturers require system solutions that include:

- Comprehensive design tools and system-level solutions
- DSP devices that offer increasing levels of signal processing and integration
- Peripherals that provide the ability to interface with both packet- and circuit-switched networks and software support

The challenges in today's packet-based networks are to reduce overall cost (increased integration), reduce power consumption and create a unified approach to transporting voice, video and additional media. The Freescale MSC825x family of DSPs is a fully software-programmable series of DSP solutions suitable not only for voice,

video and data applications. Customers can use the MSC825x family to architect very flexible and scalable solutions for media-over-IP equipment. Due to the programmability and flexibility of the DSP family, customers can adjust the mix of media traffic being processed in real time.

The DSP subsystem is designed to run essential signal processing functions for voice, fax and modem data applications. At the heart of a typical media processing subsystem are multiple MSC825x DSPs.

Typical functions include voice encoding and decoding (wide band and narrow band), tone detection, voice activity detection/comfort noise generation/packet loss concealment (VAD/CNG/PLC), echo cancellation (EC), as well as modem and fax data modulation and demodulation.

The DSP subsystem interfaces to a host processor (typically a Freescale processor built on Power Architecture® technology, such as a QorIQ processor) via the PCI

Express and/or the Gigabit Ethernet interfaces. The MSc825x family offers up to four TDM interfaces, each supporting a maximum of 256 channels of narrow-band voice. These can then connect to T1/E1 TDM ports.

Freescale offers a rich portfolio of voice (narrow and wide-band) software technologies, along with voice enhancement, tone detection and generation, video and modem/fax-related functions.

Please contact your Freescale representative for more information.



## Media Gateway (Unified Communications)/ Session Border Controllers

Application highlights and requirements:

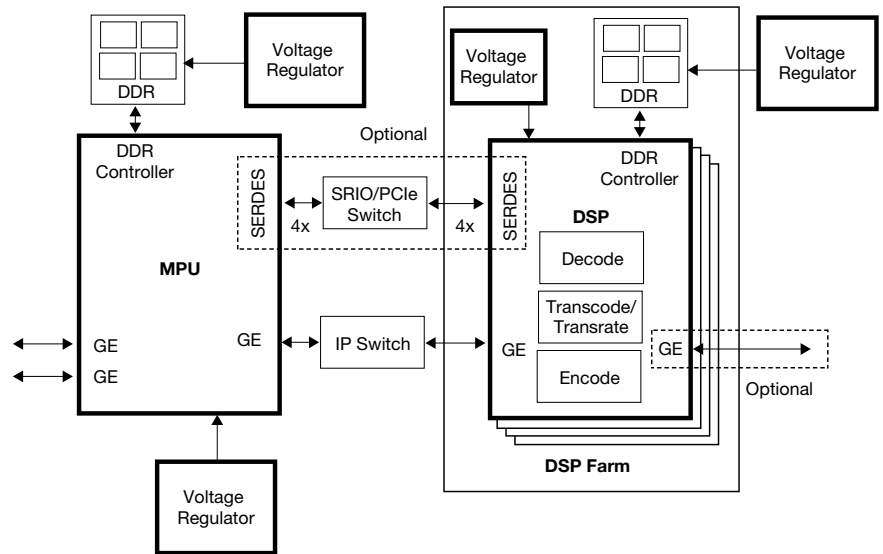
- Packet based (IP to IP)
- Programmability and flexibility for converged voice and video communications
- High-bandwidth/low-latency DSP layer 2 interconnect
- Low power consumption
- High channel density, 100s to 1000s of channels
- Hardware support for redundancy

## Enterprise Application

Application highlights and requirements:

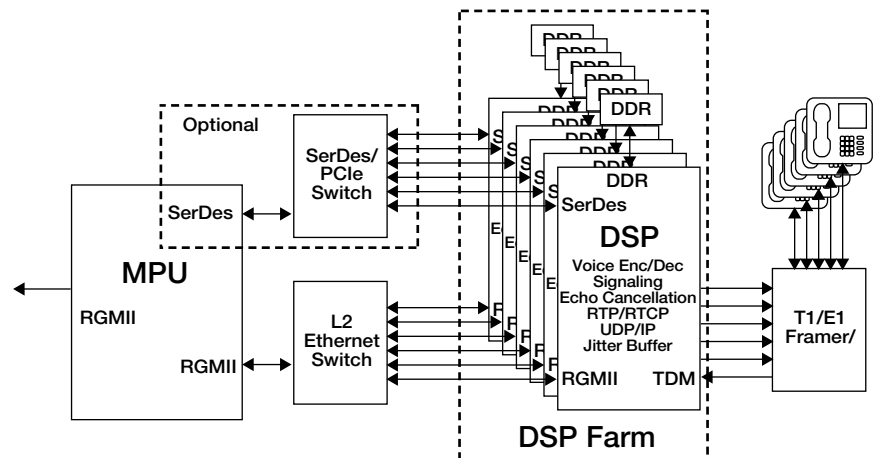
- TDM support for conventional POTs or T1/E1 interfaces (TDM to IP)
- Medium to low channel density, scalability from 10s to 100s of channels
- Requires specialized functions for telephone interface such as line echo cancellation

### Media Gateway Block Diagram



Freescale Technology

### Enterprise IP-PBX Block Diagram



# Medical Imaging

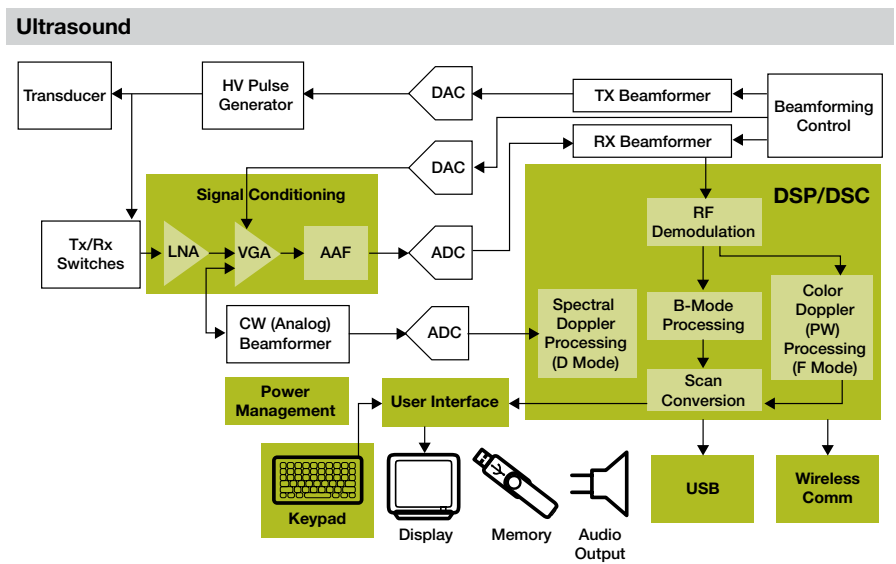
The complexities of medical imaging require extraordinary processing power. Modalities such as ultrasound, X-ray, magnetic resonance imaging (MRI) and computed tomography (CT) scans all push performance limits for advanced integrated I/O, rigorous data processing and high levels of connectivity. These needs are addressed by the MSC815x and MSC825x families of high-performance DSPs which are capable of performing the compute intensive image reconstruction and image processing at the heart of medical imaging systems.

MSC815x and MSC825x devices offer unprecedented I/O and memory bandwidth with the ability to combine PCI Express, Serial RapidIO and/or Gigabit Ethernet and one or two 64-bit DDR2/3 interfaces for data intensive applications such as medical image reconstruction.

The MSC815x device family also features a dedicated DFT/FFT hardware accelerator capable of running up to 350 Mega samples/sec. Off-loading these functions from the cores leaves ample processing headroom for additional system requirements or enables the use of single- or dual-core devices.

## Ultrasound

Ultrasound is a non-invasive medical imaging technique used to visualize muscles, tendons, pathological lesions and many internal organs and other structures. It plays an important role during prenatal care and is commonly used as a diagnostic tool. Ultrasound



■ Freescale Technology

sends ultrasonic waves through the patient and detects the echoes of the bounced back waves, applies digital processing to these signals and builds an image to be shown on a screen.

Image reconstruction and processing can be best realized on MSC815x or MSC825x high-performance single- or multicore DSP devices which are capable of performing the data intensive B mode image reconstruction and the different modes of doppler processing that are integral parts of any ultrasound system. Doppler processing can be accelerated by use of the dedicated FFT/DFT units in the Maple hardware coprocessor to achieve greater throughput and better utilization of the device's resources. MSC815x and MSC825x DSP families are also ideal for

additional signal processing functions, such as filtering, demodulation and scan conversion required for achieving the desired output image.

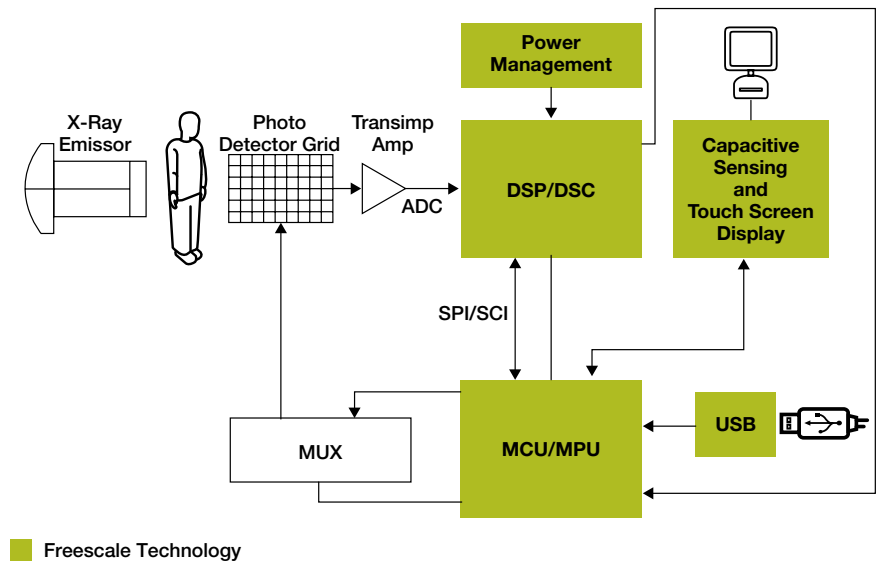
Freescale plans to offer B-mode processing libs in order to accelerate development time for our end customers. Please contact your Freescale representative for more information.

## Digital X-Ray Scanner

Digital X-ray imaging uses digital sensors instead of traditional photographic film. A common X-ray system is composed of an analog front end where the actual X-ray is performed and transmitted to a digital image processing unit for image reconstruction, processing and display generation.

The signal processing and conditioning used to generate radiography involves the transformation of signals from the spatial domain to frequency domain by use of Fourier Transform, performing convolutions on the transformed data and inverse transform back to spatial domain. The MSC815x family of devices with the MAPLE coprocessor containing the dedicated DFT/FFT hardware accelerators is ideal for implementing these functions and other image processing techniques used in X-ray applications.

### Digital X-Ray



### MAPLE Coprocessor DFT/FFT Performance

| Standard Compliance  | Data Rates  | Comments                      |
|--|---|-------------------------------|
| FFT sizes: 128, 256, 512, 1024, 2048 points  | FFFT 2048: Up to 280 Mega samples/sec                                   | Advanced scaling options      |
| DFT sizes: Variable-length DFT/IDFT processing of $2^k \cdot 3^m \cdot 5^n \cdot 12$ , up to 1536 points | FFT 1024: Up to 350 Mega samples/sec<br>DFT: Up to 175 Mega samples/sec | Guard bands insertion in iFFT |

# Aerospace and Defense

## Mission-Critical Applications

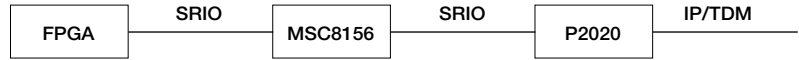
MSC815x and MSC825x DSPs provide a number of features critical to the aerospace and defense industries, including high processing performance, high throughput I/Os, flexible programmable architecture, extended temperatures and 10+ years of product longevity\*.

A key need for aerospace and defense customers is test time and costs. With the scalability allowed by the MSC815x and MSC825x families, customers can use the single-core MSC8251 for one program and the MSC8256 six-core DSP for different projects using the same hardware enabled by the pin-for-pin compatibility of our MSC825x and MSC815x families, reducing the need for full retest or verification.

## Software Defined Radio

Software defined radio (SDR) systems have become prevalent in the last decade in order to overcome wireless communication interoperability issues. SDR is now necessary for emergency/public safety and military communications with a strong pull from consumer segments. The common requirements of this application space include pure programmable processing performance and multitasking. The MSC815x math capability allows it to handle various modem processing functions, including filtering, modulation, demodulation, error correction encoding and decoding as well as a minimum product lifetime of 10 years\*. The MSC815x is complimented by the MPC8572 communications

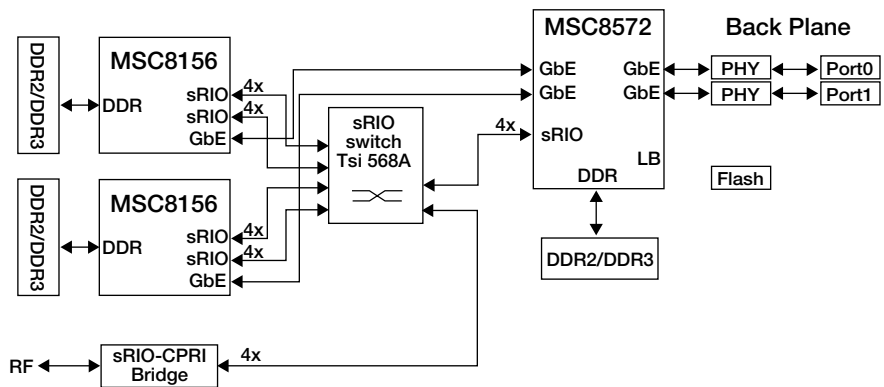
### MSC8156 and P2020 Hardware Block Diagram



Many mission critical devices have an inherent need for fast capture of data and processors with high processing performance as well as high throughput. Mission critical applications also use a large number of FFT/DFT calculations. The high performance of the MSC815x and MSC825x families of DSPs, ranging from 1 GHz single-core DSPs up to 6 GHz multicore DSPs with FFT/DFT/Viterbi and Turbo coprocessor blocks, combined with a 500 MHz switching fabric, make them a perfect solution for a number of mission critical needs. In a large portion of mission critical applications, high-performance DSPs connect to FPGAs or to QorIQ devices. All MSC815x and

MSC825x family members have both PCI Express 1.0 and multiple four lane Serial RapidIO interfaces in order to create the fastest possible throughput between FPGA, QorIQ communications processors or other DSPs. Freescale provides multiple development platforms with MSC8156 to FPGA (MSC8156ADS) or MSC8156 to QorIQ (MSC8156 and P2020 AdvancedMC™ reference design) with freely available schematics, gerber and orchard files to accelerate board development. A small front-end bridge is required in case of a CPRI/OBSAI backplane.

### Software Defined Radio



processor, built on Power Architecture technology, which is an optimized networking processor that allows high communications throughput and reliability in a wireless radio communication product.

## Key Features

- Downlink: Four Tx antennas, beamforming, 100 Mbps max per sector
- Uplink: Eight Rx antennas, 14 Mbps max per sector
- Serial RapidIO switch for full connectivity between devices, with option to remove Serial RapidIO switch using pass-through feature (TBV)

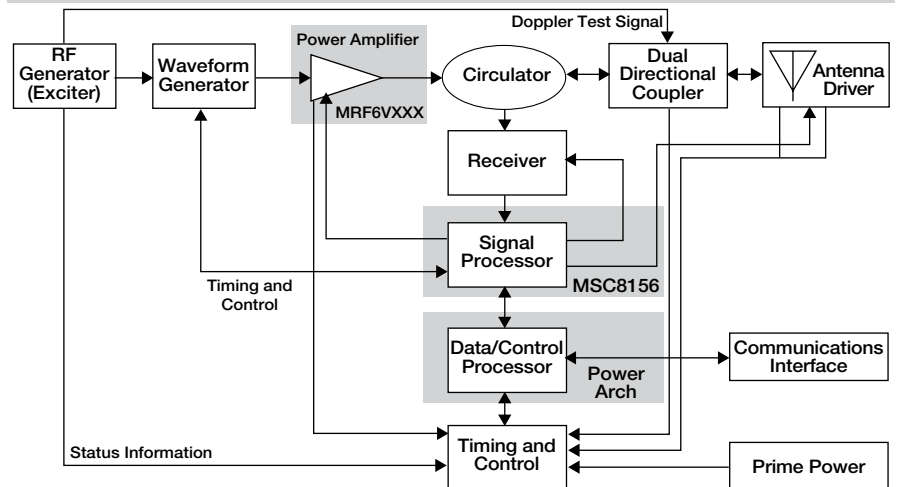
\*Products may be supported by Freescale's Product Longevity Program. For Terms and Conditions and to obtain a list of available products, visit [freescale.com/productlongevity](http://freescale.com/productlongevity).



## Radar/Sonar

The MSC8156 DSP is ideally suited for radar, sonar or infrared as a stand-alone system or as an integrated part of a military or aerospace end product. With 6 GHz of processing power, full ECC memory protection and a 10+ year product life cycle\*, the MSC8156 DSP is an ideal choice for high-performance radar, sonar or infrared solutions. With many application processing requirements relying heavily on FFT/DFT/FIR algorithms, the MAPLE-B coprocessor with a hardware accelerated FFT/ DFT and Turbo/Viterbi coprocessing allow customers to call the required functions via predefined APIs.

### Radar/Sonar Block Diagram



\*Products may be supported by Freescale's Product Longevity Program. For Terms and Conditions and to obtain a list of available products, visit [freescale.com/productlongevity](http://freescale.com/productlongevity).



# Advanced Test and Measurement

Testing is a necessary requirement for manufacturers of consumer and industrial electronic equipment. Irrespective of the market segment, products must be tested before being shipped to the end customer. There are certain sub segments within the overall test and measurement market where the use of advanced digital signal processing is prevalent. The three sub segments and applications are as follows:

- Communications test equipment
  - Wireless testers (WiMAX, Wi-Fi, WCDMA, 4G-LTE)
  - Wireline testers (packet switched and circuit switched)
- Automated/semiconductor test equipment
  - Digital/analog testers
- General purpose test
  - Signal generators and analyzers

Freescale's MSC815x and MSc825x families of devices are particularly well suited to many of these sub-segments. Boasting not only the highest performing fixed-point DSP core on the market, but also a rich array of high-speed interconnect and memory interfaces. Furthermore, the MSC815x family of DSPs is backed by MAPLE-B technology, which accelerates common algorithms found on DSPs targeted at many of the applications listed at left. One of the common challenges of DSPs, generally in test and measurement, and wireless test and measurement in particular, is the availability and use of high-speed peripheral interfaces that allow high amounts of data to be stored and processed in real time.

Freescale's latest generation of DSP processors helps to solve these challenges by offering a total of eight lanes of SerDes high-speed interconnect designed to support un-paralleled bandwidth and low latency data exchange with the following interface combinations:

- Two 1x/4x Serial RapidIO ports
- One 1x/4x Serial RapidIO ports, one 1x Serial RapidIO port and two SGMII ports
- One 1x/4x Serial RapidIO port and a PCI Express port
- One 1x/4x Serial RapidIO port, two SGMII ports and a PCI Express port

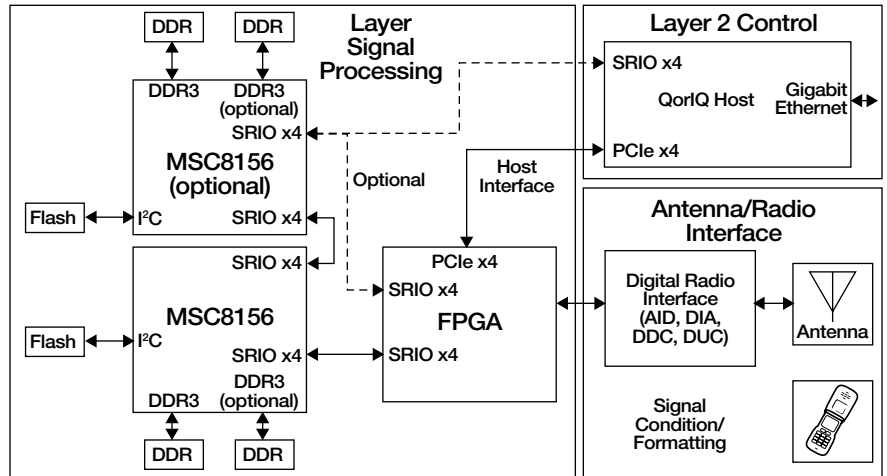
Freescale complements this interconnect with two 64-bit, 800 MHz data rate, DDR-III interfaces.



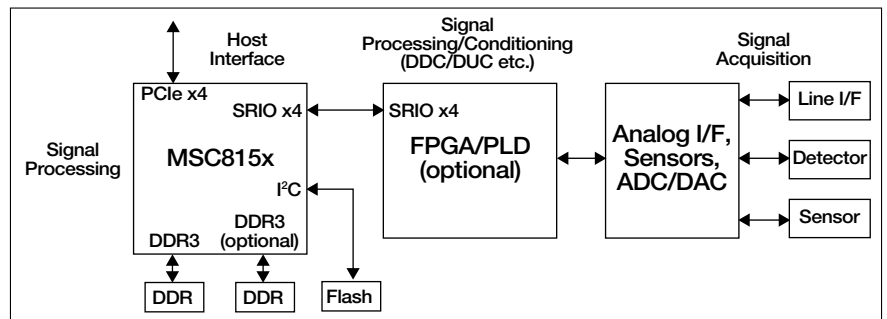
## Wireless Handset Test Equipment

The following system diagrams show examples of a DSP-based wireless handset test and measurement system. The system demonstrates a standard baseband system where modulated radio data is sent and received from the radio and antenna interfaces. Oversampled data is down converted (decimated) or upsampled (interpolated) from and to the radio card. An FPGA may be used to perform physical layer formatting between the layer 1 processing functions performed on the MSC8156, or multiple MSC8156s, and the radio card. Processing is subsequently split into layer 1 (MIMO support, downlink and uplink physical and transport channel processing) and layer 2 processing (media access, radio link control and packet data convergence) typically performed on a host processor such as Freescale's QorIQ P4040 or P4080 communications processors.

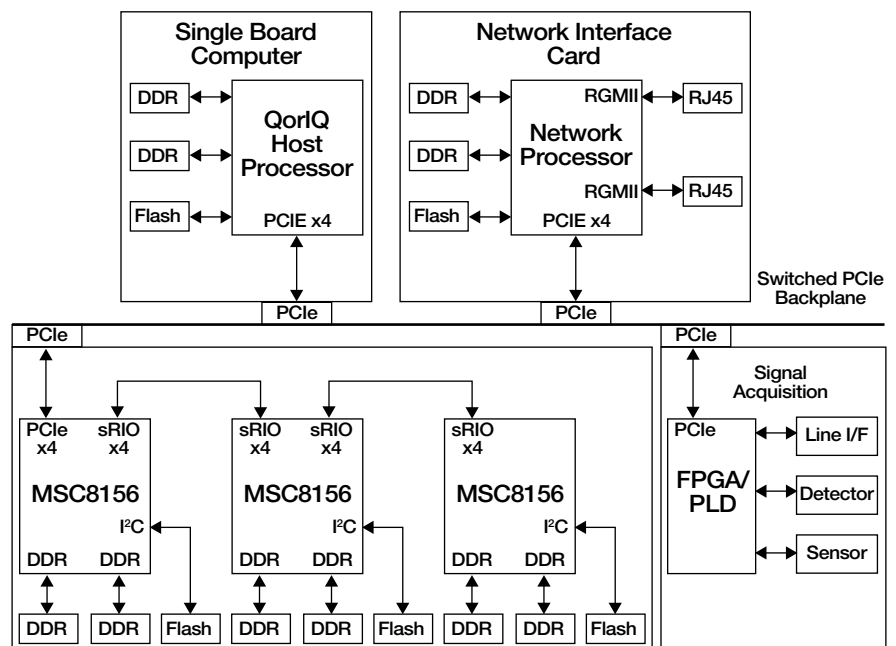
### Wireless Handset Test Equipment



### PCI-Based Single DSP Test System



### Modular Test Platform





# Development Software, Tools and Reference Designs





# CodeWarrior Development Studio for StarCore 10.0 DSPs

CodeWarrior Development Studio is an Eclipse-based, completely integrated development environment (IDE) that provides a highly visual and automated framework to accelerate the development of the most complex embedded applications.

## Debugging Tools

Debugging multicore architectures can be a challenging task. CodeWarrior IDE includes a wide range of debugging tools simplifying the task of multicore embedded programming. CodeWarrior's multicore debugging features such as core grouping and multicore run control make this task much easier. The MMU configurator provides a way to debug RTOS virtual memory management problems by allowing the developer to see and experiment with and even generate code for different MMU settings. The on-chip emulation (OCE) configurator provides an easy way for developers to monitor for different types of accesses to critical areas of memory.

## Software Analysis, Profiling and Trace

With an extensive array of tools, developers save time by quickly identifying and resolving functional and performance issues. CodeWarrior IDE for StarCore DSPs has a sophisticated profiler that helps the developer pinpoint cache performance or stall problems as well as show how ALUs and AGUs are being utilized. The trace analyzer provides a view of the sequence of instruction execution that led the processor to be in a problem state. Through trace points, the developer can pinpoint the precise segments of code that are of interest. Sometimes user applications corrupt system register values. The register analyzer can quickly identify unexpected hardware states and alert the programmer to a problem.

## Compiler

CodeWarrior's optimizing compiler provides developers with choices in developing high-performance code. For developers who do not want to spend time hand-tuning their applications for the maximum possible performance, CodeWarrior's compiler has aggressive optimization options that do the job. Developers who want to obtain the maximum performance possible can choose from a wide selection of intrinsic functions that implement common tasks in a way that most efficiently utilizes the architecture. The documentation provided with the tools includes descriptions of how and when to use different intrinsic functions, and examples that illustrate their use.

## SmartDSP OS RTOS (SDOS)

SDOS is Freescale's optimized multicore StarCore OS. It offers highly efficient program execution with extensive functionality, including an integrated network stack, a compact and lightweight kernel with real-time, priority-based, pre-emptable execution. It is offered royalty free to Freescale customers and offers packaged drivers along with kernel and driver source code.

# Voice Software

Freescale and certain key partners offer an extensive range of voice-related software technologies for license in source code or binary code format. Our voice software portfolio covers many standardized ITU-T, IETF and 3GPP voice and voice-related technologies. In addition, Freescale has a number of patented technologies for advanced voice applications like wide band conferencing, sample rate conversion, automatic level control and narrow band line echo cancellation.

Whatever your voice application, whether circuit-switched, packet-switched, TDM or IP-based, narrow band, wide band or extended wide band, Freescale and our third-party network are likely to have the technology you need.

All software is covered by complete documentation explaining the memory, performance requirements and integration of the respective technologies.

| Voice Codecs                             |  |                    |
|--|--|--------------------|
| <b>Low Complexity: Narrow/Wide Band</b>  |  |                    |
| G711                                     | G.729 B  | GSM-FR             |
| PLC                                      | G722.1 ( C )                                     | VADCNG             |
| G.726 ( A )                              |  |                    |
| <b>Mid Complexity: Narrow/Wide Band</b>  |  |                    |
| G.723.1A                                 | GSM-HR (raw bitstream output)                    | AMR-NB             |
| G.729 ( I )                              | GSM-EFR  | G722 with Annex IV |
| iLBC                                     |  |                    |
| <b>High Complexity: Narrow/Wide Band</b> |  |                    |
| G.728                                    | EVRC-A   | EVRC-B             |
| G722.2 (AMR-WB)                          |  |                    |
| <b>High Complexity: Wide Band</b>        |  |                    |
| AAC-LC/LD                                | AAC-HE   | EVRC-WB            |
| <b>Voice Enhancement Devices</b>         |  |                    |
| Low Complexity                           | Sample Rate Convertor                            | Mid Complexity     |
| ALC-WB                                   | N-Way Conferencing                               | G.168              |
| NR                                       | Voice Activity Det (VAD)<br>Stand Alone          |                    |
| <b>FAX/Modem</b>                         |  |                    |
| Caller ID (depends on v.23 pump)         | V.21/V.27/V.29/V.17<br>(as part of T.38 package) | V.32/V.32bis       |
| T.38                                     | V.23   |                    |

Please contact your Freescale sales representative or our third-party providers for further information on licensing and commercial terms and conditions.

# Video Software

Freescale offers a wide variety of video codecs necessary for implementing today's leading media communication systems, such as videoconferencing and media gateways. All codecs are optimized for high quality and maximum efficiency running on the StarCore-based MSC815x and MSC825x high-performance DSPs. Codecs are available in binary form for quick download and evaluation or can be licensed in source form open to customer edits. Freescale's flexible software codecs running on high-performance single- and multicore DSP devices enable scalable,

cost-effective programmable system solutions required for winning in today's competitive market place.

Freescale's video codec offering includes the first fully featured implementation of HD H.264/scalable video coding (SVC) standard, allowing single encode to multiple targets and overcoming network reliability issues.

Detailed codec information and quick downloads can be found at [freescale.com/DSP](http://freescale.com/DSP).

| Video Codecs |
|--------------|
| <b>Codec</b> |
| H.264/SVC    |
| H.264BP      |
| H.263p3      |
| MPEG-4SP     |
| H.261        |
| MPEG-2       |
| MJPEG        |
| JPEG2000     |
| H.264MP/HP   |



# Base Station Software

## LTE Layer 1 Software

The LTE Layer 1 software includes physical baseband channel processing and radio transport channel functions as defined in the 3GPP standards. Freescale provides a comprehensive set of kernel modules covering the Layer 1 processing for physical downlink shared channel and physical uplink shared channels. The kernels are further combined into uplink and downlink chains, which run in real time using the SmartDSP real-time operating system as a reference. All software is developed as ANSI-C callable and fully documented.

In brief, the physical layer processing functions include:

- Modulation
- Channel coding
- Transmission schemes
- Multiplexing
- MIMO/diversity
- Channel estimation
- Equalization (outside 3GPP scope)

## WCDMA Layer 1 Software

The WCDMA Layer 1 software covers uplink and downlink symbol rate processing as defined in the 3GPP standards. Freescale provides a comprehensive, fully documented set of kernels developed in C and ASM.

### Real-Time Software Subsystem Features

| Category                  | Specifications/Features  |
|---------------------------|--|
| Design approach           | <ul style="list-style-type: none"> <li>• Layered API software approach enables multi-level reuse and ease of integration</li> <li>• Modular C software modules for all subsystems. Includes C wrapper for optimized real-time assembly modules</li> <li>• Algorithm verification with floating- and fixed-point simulation system</li> <li>• Multicore framework allows for efficient inter-core communication and task partitioning</li> </ul>  |
| Features                  | <ul style="list-style-type: none"> <li>• Focus on high-speed shared user physical channels                             <ul style="list-style-type: none"> <li>○ Physical Downlink Shared Channel (PDSCH) (36.211 chapter 5.3)</li> <li>○ Physical Uplink Shared Channel (PUSCH) (36.211 chapter 6.3)</li> <li>○ Random Access Channel (RACH)</li> </ul> </li> <li>• Modular design with well-defined interfaces and module interactions                             <ul style="list-style-type: none"> <li>○ Downlink                                     <ul style="list-style-type: none"> <li>·· IF1Tx: L1/L2 logical interface. Memory mapped over Serial RapidIO</li> <li>·· IF2Tx: Transport to physical channel interface per 3GPP 36.211 and 36.212</li> <li>·· IF3Tx: Transport to OFDMA processing interface. Re-maps IFFT signal generation onto FPGA</li> <li>·· IF4Tx: Baseband I/Q sample interface towards the antenna FPGA</li> </ul> </li> <li>○ Message-based configuration and runtime control</li> <li>○ Includes MIMO processing</li> </ul> </li> </ul> |
| RTOS support              | <ul style="list-style-type: none"> <li>• SmartDSP OS: Integrates real-time kernels and drivers</li> </ul>  |
| API                       | <ul style="list-style-type: none"> <li>• Full software abstraction through well-defined and documented APIs                             <ul style="list-style-type: none"> <li>○ SBL1 API structure for reuse on function level</li> <li>○ Framework API for reuse of higher level, complete processing chains</li> <li>○ Complete subsystem reuse possible for channel types</li> </ul> </li> </ul>   |
| Validation/test           | <ul style="list-style-type: none"> <li>• Software tested on:                             <ul style="list-style-type: none"> <li>○ Unit level (individual modules)</li> <li>○ Integration level (module interaction)</li> <li>○ System level (system operation, performance)</li> </ul> </li> <li>• Software test environment is part of the software delivery package</li> </ul>   |
| Standards reference       | <ol style="list-style-type: none"> <li>[1] 3GPP TS 36.201: LTE physical layer general description (v1.0.0)</li> <li>[2] 3GPP TS 36.211: Physical channels and modulation (v1.0.0)</li> <li>[3] 3GPP TS 36.212: Multiplexing and channel coding (v1.3.2)</li> <li>[4] 3GPP TS 36.213: Physical layer procedures (v1.0.0)</li> <li>[5] 3GPP TS 36.214: Physical layer measurements (v0.1.0)</li> <li>[6] 3GPP TS 36.300: E-UTRA and E-UTRAN overall description; Stage 2 (v8.0.0)</li> <li>[7] 3GPP TS 25.212: UTRA multiplexing and channel coding</li> </ol>   |
| Layer 1 software packages | <ul style="list-style-type: none"> <li>• Signal processing library: Contains LTE Layer 1 signal processing manager and kernel library functions. The signal processing kernels are the basic processing units and the signal processing manager is the chain integration of a set of kernels which includes:                             <ul style="list-style-type: none"> <li>○ DL Transport Channel Package</li> <li>○ DL Physical Channel Package</li> <li>○ UL Transport Channel Package</li> <li>○ UL Physical Channel Package</li> </ul> </li> <li>• Functional integration of uplink/downlink chains (PDSCH/PUSCH) on multicore MSC8156                             <ul style="list-style-type: none"> <li>○ Uses SmartDSP OS real-time operation</li> </ul> </li> </ul>   |

# Base Station Software

| WCDMA Code            |                                 |             |
|-----------------------|---------------------------------|-------------|
| Channel               | Function                        | Source Code |
| DL Symbol Rate R99    | CRC Generation                  | C           |
|                       | Convolutional Coding Rate 2     | C           |
|                       | Coding Rate 3                   | C           |
|                       | Turbo Table Generation          | C           |
|                       | Turbo Coding                    | C           |
|                       | Turbo Puncturing                | C           |
|                       | Convolutional Puncturing        | C           |
|                       | Repeat                          | C           |
|                       | Interleaver 1                   | C           |
|                       | Interleaver 2                   | C           |
| DL Symbol Rate HSDPA  | Full R99 SR DL Integrated Chain | C+ASM       |
|                       | Byte Pack                       | C+ASM       |
|                       | CRC Attachment                  | C           |
|                       | Bit Scrambling                  | C+ASM       |
|                       | Block Segmentation              | C+ASM       |
|                       | Byte Unpack                     | C+ASM       |
|                       | Channel (Turbo) Coding          | C           |
|                       | TurbolL                         | C+ASM       |
|                       | HARQ Manager                    | C+ASM       |
|                       | RM1                             | C+ASM       |
|                       | RM2 - Systematic                | C+ASM       |
|                       | RM2 - P1, P2                    | C+ASM       |
|                       | Bit Collection                  | C+ASM       |
|                       | Physical Channel Seg            | C+ASM       |
| UL Symbol Rate R99    | Interleaving                    | C           |
|                       | MAPLE DEPE Basic Driver         | C           |
|                       | Crc Check                       | C+ASM       |
|                       | Channel Decoding                | C+ASM       |
|                       | Rate De-Matching                | C+ASM       |
|                       | First Deinterleaving            | C+ASM       |
| Second Deinterleaving | C+ASM                           |             |
| Channel Demapping     | C+ASM                           |             |
| Full R99 SR UL Chain  | C+ASM                           |             |

| LTE Code |                      |  |  |                |
|----------|----------------------|--|--|----------------|
| Channel  | Manager              | Kernel                                 | Functions  | Source Code    |
| DL-SCH   | TBP                  |  | Transport Block Processing                           | C              |
|          |                      | TB CRC Gen                             | Transport Block CRC Generation                       | C              |
|          |                      | CodeBlockSegmentation                  | Code Block Segmentation                              | C              |
|          | CBP                  |  | Code Block Processing                                | C              |
|          |                      | CB CRC Gen                             | Code Block CRC Generation                            | C              |
| PDSCH    |                      | Turbo Encoder                          | Turbo Encoding                                       | C              |
|          |                      | RateMatching                           | Rate Matching  | C              |
|          | RBP                  |  | Resource Block Processing                            | C              |
|          |                      | BitScrambling                          | Scrambling   | C              |
|          |                      | ModMapping                             | Modulation Mapping                                   | C              |
|          |                      | LayerMapping                           | Layer Mapping  | C              |
| UL-SCH   |                      | Precoding                              | Precoding  | C              |
|          |                      | PRBMapping                             | Physical Resource Block Mapping                      | C              |
|          | TBP                  |  | Transport Block Processing                           | C              |
|          |                      | TB CRC Detect                          | Transport Block CRC Detection                        | C              |
|          |                      | CodeBlockDesegmentation                | Code Block Desegmentation                            | C              |
|          | CBP                  |  | Code Block Processing                                | C              |
|          |                      | HARQ Combining                         | Hybrid Automatic Repeat Request Combining            | C              |
|          | DCdemux              |  | Data and Control Demultiplexing                      | C              |
| PUSCH    |                      | CodeBlockDeconcatenation               | Code Block Deconcatenation                           | C              |
|          |                      | Dcdemux                                | Data and Control Demultiplexing                      | C              |
|          |                      | Channel Deinterleaving                 | Channel Deinterleaving                               | C              |
|          | VRB                  |  | Virtual Resource Block Processing                    | C              |
|          |                      | Demodmapping                           | Demodulation Mapping                                 | C              |
|          |                      | Descrambling                           | Bit Descrambling                                     | C              |
|          | PRB                  |  | Physical Resource Block Processing                   | C              |
|          |                      | SNR2x2                                 | 2x2 SNR Estimation                                   | C              |
|          |                      | Equalizer2x2                           | 2X2 Equalizer  | C              |
|          |                      | SNR2x4                                 | 2x4 SNR Estimation                                   | C              |
| RSP      |                      | Equalizer 2x4                          | 2x4 Equalizer  | C              |
|          |                      | Equalizer 2x4int                       | 2x4 Interpolation Equalizer                          | C              |
|          |                      | Reference Signal Processing            | Reference Signal Processing                          | C              |
|          |                      | CE2Tx                                  | Channel Estimation MIMO                              | C              |
| NA       |                      | CE1Tx                                  | Channel Estimation for SISO                          | C              |
|          |                      | RMDecoding                             | Reed Muller Decoding                                 | C              |
| PRACH    | FDP                  |  | Frequency Domain Processing                          | C              |
|          |                      | sc_sel                                 | RACH Subcarrier Selection                            | C              |
|          |                      | cor_0p                                 | Correlation and Zero Padding                         | C              |
|          | DPP                  |  | Delay Profile Processing                             | C              |
|          |                      | DP_compute                             | Delay Profile Computation                            | C              |
| PUCCH    | format 1             | TBD                                    | PUCCH Format 1 Demodulation                          |                |
|          | format2              | TBD                                    | PUCCH Format 2 Demodulation                          | Available 1Q11 |
| SRS      |                      | TBD                                    | SRS Metric Calculations                              | Available 1Q11 |
|          | Downlink Integartion | Real-Time Scheduling                   | 1. Real-Time Integration for the DLSCH and the PDSCH | C              |
|          | Uplink Integartion   | Real-Time Scheduling                   | 1. Real-Time Integration for the ULSCH and the PUSCH | C              |
|          |                      |  | 2. Support for Turbo Decoding Using MAPLE TVPE       | C              |
|          |                      |  | 3. Support for FFT Using MAPLE FFTPE                 | C              |
|          |                      |  | 4. Support for DFT Using MAPLE DFTPE                 | C              |
|          | Guard Insertion      | Insertion/Removal of the Guard Carries | MAPLE FFT for the Guard Insertion                    | C              |
|          | Guard Removal        | Removal of the Guard Carries           | System DMA for Guard Removal                         | C              |
|          | iFFT/FFT             | Time <-> Freq Conv                     | MAPLE FFTPE for iFFT and FFT Operation               | C              |
|          | Cyclic Prefix        | Insert and Remove Cyclic Prefix        | System DMA to Manage CP Insert and Remove            | C              |

# MSC8156 Evaluation Module

For evaluation of the MSC815x or MSC825x family of StarCore DSPs

## Overview

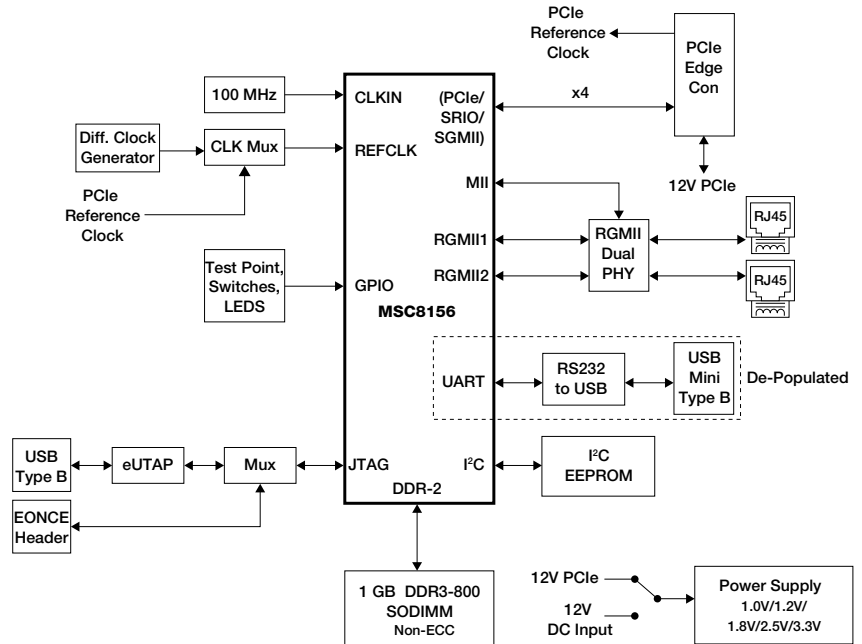
The MSC8156 evaluation module (MSC8156EVM) is a cost-effective (\$459 USD MSRP) tool intended for engineers evaluating the MSC815x and MSC825x family of Freescale DSPs. The MSC815x and MSC825x family of DSPs are highly integrated DSP processors that contain one, two, four or six StarCore SC3850 cores. The family supports raw programmable DSP performance values ranging from eight GMACs to 48 GMACs, with each DSP core running at 1 GHz. These devices target high-bandwidth, highly computational DSP applications, such as 3GPP, TD-SCDMA, 3G-LTE and WiMAX base station applications as well as aerospace and defense, medical imaging, video, voice and test and measurement applications. The MSC8156EVM is intended to serve as a platform for evaluating the capabilities of the MSC815X and MSC825x family of DSPs. On-board resources and the associated CodeWarrior tools help to enable a variety of tasks, including:

- Download and run code
- Set breakpoints
- Display memory and registers

The MSC8156EVM supports two working configurations:

- Stand-alone mode: The MSC8156EVM can run in stand-alone mode with direct connections to a development system for debug, power supply and other external connections.

MSC8156EVM Block Diagram



- PCI Express mode: With the MSC8156EVM plugged into a PCI Express connector as provided, for instance, on Freescale's QorIQ enabled COM single board computer (SBC) environment. The EVM allows testing of PCI Express and Serial RapidIO interconnects and is designed to be compatible with a standard PCI Express interconnect.

## Features

- Supports the MSC815x and MSC825x DSPs at 1 GHz
- A single DDR controller (DDRC2) configured in DDR3 mode: 204-pin SODIMM, 64-bit at 800 Mbps, no ECC, 1 GB of memory
- The DSP RGMII (at ports GE1 and GE2) connects to a Marvell 88E1121 dual GETH PHY for regular board configuration
- Two available debug interfaces, including on-board USB TAP controller (eUTAP) or on-chip emulation 14-pin header for any external TAP controller
- 100 MHz clock oscillator for the DSP clock in
- The EVM can operate in two main supply configurations (configurable via switch S1)
  - Stand-alone mode with external 12V DC
  - PCI Express mode powered from edge connector
- Push buttons: Main power-on-reset (SW8), hard reset (SW7), IRQ0 (SW5), NMI (SW6)



## Development Support

Freescale supplies CodeWarrior IDE, a robust and full-featured set of DSP development tools. The CodeWarrior tool suite is an Eclipse-based integrated development environment supporting the evaluation of many of the features of the Freescale MSC815x and MSC825x family of single- and multicore DSPs. With applications ranging from base stations to medical imaging, aerospace to advanced test and measurement, the development environment gives designers everything they need to exploit the advanced capabilities of the MSC815x and MSC825x architecture.

The CodeWarrior tool suite includes:

- An Eclipse-based integrated development environment

- C and C++ compiler with in-line assembly
- Librarian
- Multicore debugger
- Royalty-free RTOS
- Software simulator
- Profiler
- High-speed run control
- Host platform support

Contact your local sales office or representative for availability.

# MSC8156ADS

## Advanced development system for the MSC815x and MSC825x product families

### Overview

The \$3,900 MSC8156 application development system (MSC8156ADS) is a comprehensive debugging environment intended for engineers developing applications for the MSC8156, MSC8154, MSC8256, MSC8254, MSC8252 and MSC8251 Freescale DSPs. The MSC815x and MSC825x family of DSPs are highly integrated DSP processors that contain one, two, four or six StarCore SC3850 DSP subsystems ranging from eight GMACS to 48 GMACS with each DSP core running up to 1 GHz. These devices target high-bandwidth, highly computational DSP applications, such as 3GPP, TD-SCDMA, 3G-LTE and WiMAX base station applications as well as aerospace and defense, medical imaging, video, voice and

test and measurement applications. The \$3,900 MSC8156ADS is intended to serve as a platform for software and hardware development in processor environments using the MSC815X and MSC825x family of DSPs. On-board resources and the associated debugger enable developers to perform a variety of tasks, including:

- Download and run code
- Set breakpoints
- Display memory and registers
- Connect proprietary hardware via an expansion connector

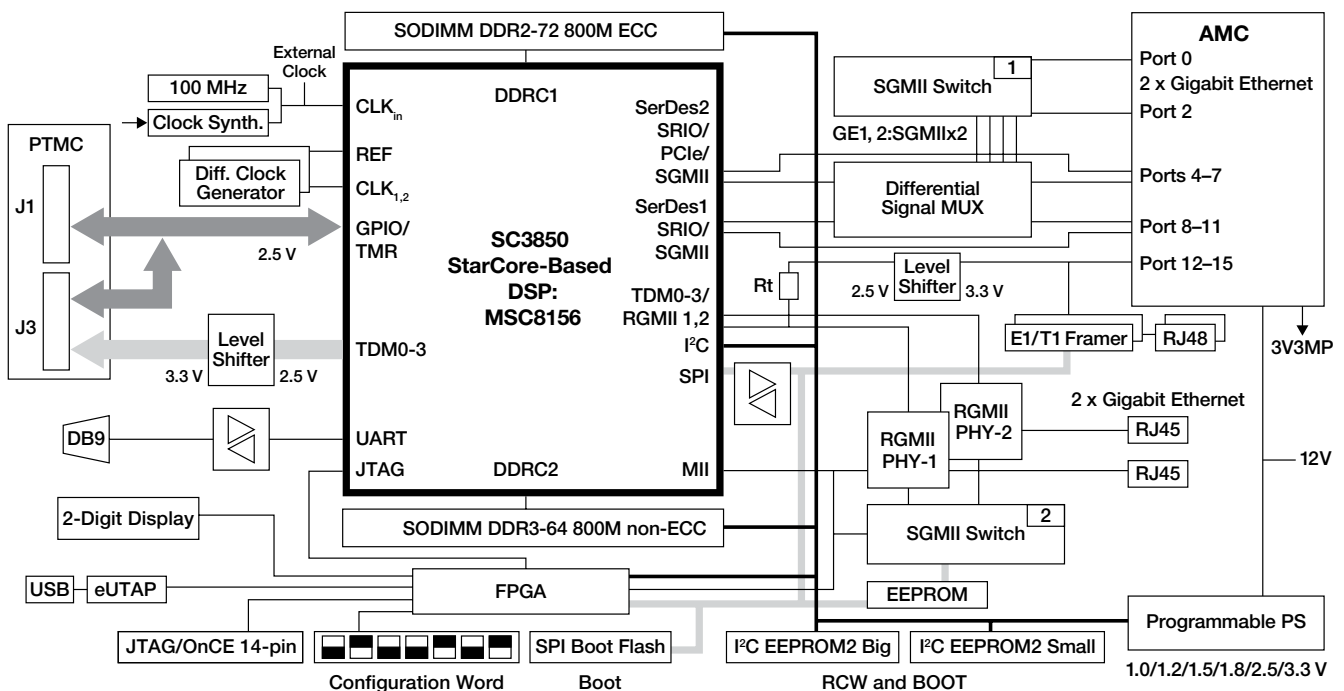
The MSC8156ADS supports two working configurations:

- Stand-alone mode: The MSC8156ADS can run in a stand-alone mode like other

application development systems, with direct connections to debuggers, power supply and other external connections.

- AdvancedMC mode: The MSC8156ADS is inserted in a standard MicroTCA backplane that allows testing of the high-speed Serial RapidIO and PCI Express ports against other platforms. By using a proprietary B2B adaptor card, the AMC-X-Over, the DSP can work with a second DSP device on an additional ADS board. The AMC edge connector carries all high-speed interface signals between the devices. The ADS is compatible with standard MicroTCA chassis, such as a Schroff® or TUNDRA® development platform.

### MSC8156 Application Development System





## Features

- Supports the MSC815x and MSC825x DSPs at 1 GHz with core voltages of 1V
- The first DDR controller (DDRC1) is configured in DDR2 mode: 200-pin SOCDIMM with ECC support, 64-bit at 800 Mbps, 1 GB of memory
- The second DDR controller (DDRC2) is configured in DDR3 mode: 204-pin SODIMM, 64-bit at 800 Mbps, No ECC, 1 GB of memory
- The DSP RGMII (at ports GE1 and GE2) connects to two single Marvell® 88E1111 GETH PHYs for regular board configuration
- A Marvell 10-port SGMII switch 88E6182 links the MSC8156 SGMII lines to 2xRJ-45 copper connectors and to the 1000 Base-X over AMC MicroTCA connector ports 0 and 2
- Pericom® PI2DBS212ZHE Diff Signal Switch parts support programmable SerDes lines multiplexing to AMC edge connector or to the SGMII switch
- Two Dallas E1/T1 framers connect to four DSP TDM ports
- P1 and P3 connectors carry DSP GPIO and TDM signals
- The DSP configuration and boot support includes reset configuration source three-bit set by appropriate DIP switches, parallel load of programmable reset configuration word from FPGA registers sampled previously from DIP switch array, serial configuration and boot from a large (64 KB) or small (1 KB) I<sup>2</sup>C EEPROM, boot from serial 8 MB SPI flash, boot from communications ports (from SerDes Serial RapidIO interface or from Ethernet SGMII or RGMII ports)
- Two available debug interfaces, including on-board USB TAP controller (eUTAP) or OnCE 14-pin header for any external TAP controller
- FPGA logic: Board control and status register (BCSR), JTAG controller allows full board programming, multiplexing of JTAG source signals, I<sup>2</sup>C master and slave controllers, MII controller to program RGMII PHY, SPI controller, boot sequencer configures ADS peripherals for boot over Ethernet, generation of TDM clock and sync, two-digit, 14-segment LED display provides current board settings
- 100 MHz clock oscillator for the DSP clock in
- An external pulse generator may be used as clock source
- Can function in various main supply configurations (configurable via DIP switches or BCSR) in stand-alone mode with an external power 12 VDC at 5A when S1 switch is on, or as an AMC card in the MicroTCA system or interconnection with AMC-X-Over card. If the ADS is fed outside, the S1 power switch should be off
- On-board power system is comprised of two regulator steps:
  - Primary power system is a power-one power manager with 1.0V POL regulator for MSC8156 loads, including cores, MAPLE and M3, 2.5V for I/O and 3.3V for on-board peripherals, DDR switching power supplies for DDRC1 and DDRC2 ports, LDOs for on-board peripherals are fed from 2.5V and 3.3V POLs and 12V input voltage, voltage supervisor monitors all the ADS power supplies. Power good (PG) signal and dedicated LED LD14 indicate power system status. Any failures cause nPRST signal be continuously low
  - Push buttons: Main power-on-reset (SW8), hard reset (SW9), soft reset (SW11), NMI (SW10)



## Development Support

Freescale supplies a comprehensive set of CodeWarrior DSP development tools for the DSP device. The tools provide easier and more robust ways for designers to develop optimized DSP systems. With applications ranging from base stations to medical imaging to aerospace and defense, the development environment gives designers everything they need to exploit the advanced capabilities of the MSC815x and MSC825x architecture. In addition to the ADS board, support tools include:

- Eclipse-based integrated development environment (IDE)
- C and C++ compiler with in-line assembly
- Librarian
- Multicore debugger
- Royalty-free RTOS
- Software simulator
- Profiler
- High-speed run control
- Host platform support

Contact your local sales office or representative for availability.

Visit [freescale.com/DSP](http://freescale.com/DSP) for more information.

# MSC8156AMC

## Advanced mezzanine card system for the MSC815x and MSC825x product families

### Overview

The Freescale MSC8156AMC is a high-density, single-width, full-height AdvancedMC (AMC) DSP platform based around three MSC8156 DSPs. The MSC8156 is a six-core DSP based on Freescale's SC3850 StarCore technology and designed to advance the capabilities of wireless broadband equipment. It delivers industry-leading performance and power savings, leveraging 45 nm process technology in a highly integrated SoC to provide performance equivalent to 6 GHz of a single-core device.

The MSC8156 DSP delivers a high level of performance and integration, combining six fully programmable new and enhanced SC3850 DSP cores, each running at 1 GHz with an architecture highly optimized for wireless

infrastructure applications. Developed by Freescale and integrated on chip, the MAPLE-B supports hardware acceleration for Turbo and Viterbi channel decoding and for discrete Fourier transforms (DFT), inverse discrete Fourier transforms (IDFT) and fast Fourier transforms (FFT) and inverse fast Fourier transforms (IFFT) algorithms. An internal RISC-based QUICC Engine subsystem supports multiple networking protocols to help to ensure reliable data transport over packet networks while significantly offloading processing from the DSP cores.

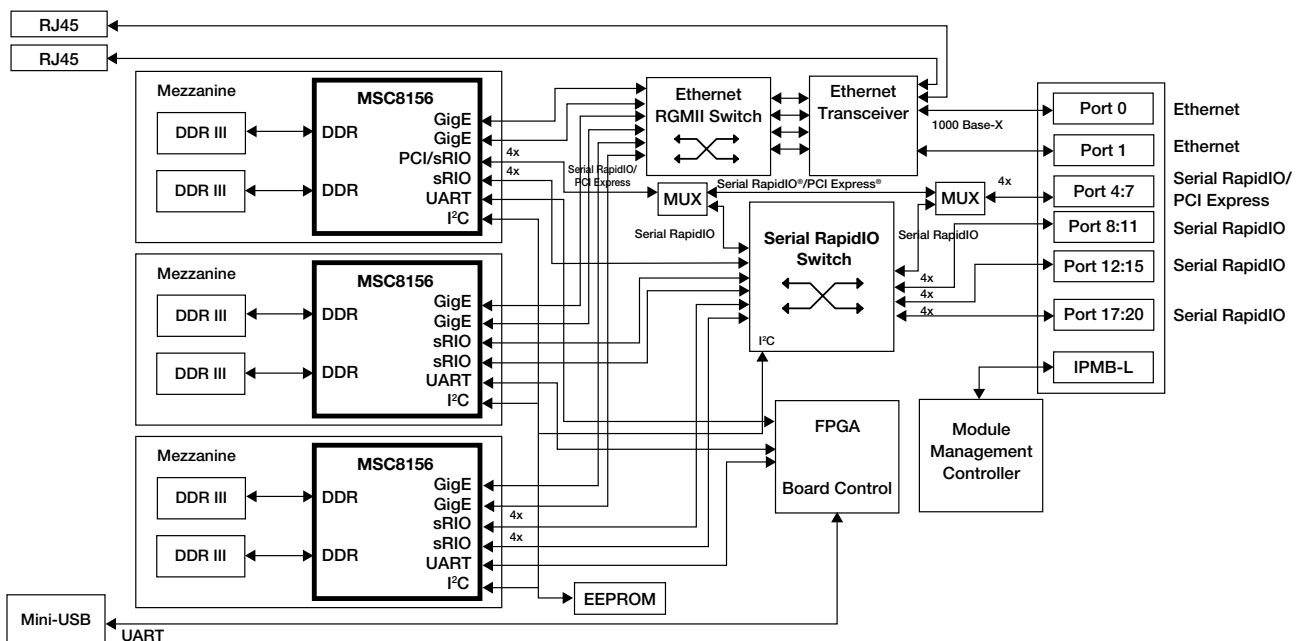
The MSC8156 embeds large internal memory and supports a variety of advanced, high-speed interface types, including two RapidIO interfaces, two Gigabit Ethernet interfaces for network communications, a PCI Express controller

and two DDR controllers for high-speed, industry-standard memory interface.

This 18 GHz of processing power, coupled with an architecture highly optimized for wireless infrastructure applications, make this an ideal platform for developing solutions for the next generation of wireless standards such as 3G\_LTE, WiMAX, HSDPA+ and TDD-LTE.

The AMC has been designed around a mezzanine concept, with three MSC8156 mezzanines providing the system building blocks, enabling rapid prototyping systems to be quickly realized.

**MSC8156 AdvancedMC™ Block Diagram**



Each MSC8156 has 1 GB of associated 64-bit-wide DDR3 memory split into two banks. For data plane applications high throughput 3.125 GHz x4 Serial RapidIO links connect the three MSC8156 DSPs to each other and to the data backplane. The RapidIO interfaces are connected via IDT's high-bandwidth 10 port (x4) CPS10Q Serial RapidIO switch.

Data and control plane applications are handled by the Gigabit Ethernet interface. Two 1000 Base-X Gigabit interfaces connect the backplane to the DSPs via an Ethernet switch. Each DSP has two Gigabit RGMII interfaces connected to the backplane via the Ethernet switch. Two additional Gigabit Ethernet interfaces are provided at the front panel for test and control.

Board control and hot swapping are provided by the Pigeon Point-based module management controller.

## Key Features

- Single-width, full-height AMC form factor
- Three MSC8156 DSPs
  - Powerful and flexible with six SC3850 StarCore cores at 1 GHz and up to 48000 MMACS per device
  - MAPLE-B
  - Two banks of 512 MB 64-bit DDR3-800 per MSC8156 processor

## Connectivity

- Serial RapidIO infrastructure (x4 3.125 GHz) connecting DSPs and backplane via Serial RapidIO switch
- Gigabit Ethernet infrastructure connecting DSPs and backplane via Ethernet switch



## MSC8156 DSP

- Six StarCore DSPs SC3850s operating at 1 GHz/8000 MMACS per core and 48000 MMACS per device
- MAPLE-B
  - Programmable Turbo and Viterbi decoder
- High-speed, high-bandwidth CLASS fabric arbitrates between the DSP cores and other CLASS members to M2 memory, M3 memory, DDR controllers, MAPLE-B and configuration registers
- 32-channel DMA
- Dual RISC core QUICC Engine subsystem operating at 500 MHz providing parallel processing independent of the DSP cores
- 2x 512 MB of 64-bit DDR3-800

## Board I/O

- AMC connector
  - 2x Gigabit Ethernet interfaces (Ports 0 and 1)
  - 3.125 GHz (x4) Serial RapidIO ports [4:7]
  - 3.125 GHz (x4) Serial RapidIO ports [8:11]
  - 3.125 GHz (x4) Serial RapidIO ports [12:15]
  - 3.125 GHz (x4) Serial RapidIO ports [17:20]
- Front Panel
  - 2x Gigabit Ethernet interfaces (RJ45)
  - Mini USB Type B for multiplexed access to DSPs UARTS

## Headers and Debug

- DSP JTAG/EONCE
- Expansion connector provides access to:
  - FPGA JTAG
  - MMC JTAG
  - MMC UART

## Module Management Controller

- Hot swapping
- FRU storage
- Status LEDs

## Application Areas

- 3G-LTE
- TDD-LTE
- WiMAX
- 3GPP-HSPA
- TD-SCDMA



## Key Features

- Single-width, full-height AMC form factor
- QorIQ P2020 processor
  - Dual e500v2 cores at 1.2 GHz
  - 1 GB of DDR2 (SOCDIMM)
  - TCP/IP acceleration
  - eSDHC
  - USB
- MSC8156 DSP
  - Six SC3850 cores built on StarCore technology at 1 GHz each
  - MAPLE-B
  - Two banks of 512 MB 64-bit DDR3-800

## Connectivity

- Serial RapidIO infrastructure (x4 3.125 GHz) connecting processor, DSP and backplane via Serial RapidIO switch
- Gigabit Ethernet infrastructure connecting processor, DSP, backplane and front panel via Ethernet switch
- Module management controller
  - Hot swapping
  - Board control

## QorIQ P2020 Processor

- Dual high-performance e500v2 cores built on Power Architecture technology
- 512 KB L2 cache
- Three RGMII interfaces
  - TCP/IP acceleration
- High-speed SerDes interface (options)
  - One x4 3.125 GHz Serial RapidIO
  - One x4 2.5 GHz PCI Express
  - One x1 2.5 GHz PCI Express and one x1 2.5 GHz Serial RapidIO
- USB interface (USB 2.0)
- Enhanced secure digital host controller (SD/MMC)
- 1 GB 72-bit DDR2-1600 SOCDIMM



## MSC8156 DSP

- Six SC3850 cores built on StarCore technology, operating at 1 GHz/8000 MMACS per core and 48000 MMACS per device
- MAPLE-B
  - Programmable Turbo and Viterbi decoder
- High-speed, high-bandwidth CLASS fabric arbitrates between the DSP cores and other CLASS members to M2 memory, M3 memory, DDR controllers, MAPLE-B and configuration registers
- Dual RISC core QUICC Engine subsystem operating at 500 MHz, providing parallel processing independent of the DSP cores
- 2x 512 MB 64-bit DDR3-800

## Board I/O

- AMC connector
  - 3.125 GHz (x4) Serial RapidIO or 2.5 GHz PCI Express ports [4:7]
  - 3.125 GHz (x4) Serial RapidIO ports [8:11]
  - 3.125 GHz (x4) Serial RapidIO ports [12:15]
  - 3.125 GHz (x4) Serial RapidIO ports [17:20]
  - 2x Gigabit Ethernet Interfaces (Ports 0 and1)

## Front Panel

- 2x Gigabit Ethernet Interfaces (RJ45)
- Mini USB Type B for UART access
- USB Type B connector

## Application Areas

- 3G-LTE
- TDD-LTE
- WiMAX
- 3GPP-HSPA
- TD-SCDMA





# Technical Highlights

A closer look at the DSP56K families  
(Including Symphony)

# DSP56K Family Overview

The DSP56K family is based on the 24-bit 56300 Onyx core and is used in a vast array of different applications ranging from guitar effects processors and audio mixing boards to industrial controllers and complex networking systems. The family includes a multitude of memory, peripheral and operating speed options ranging from single-core 150 MHz devices to 250 MHz dual-core devices.

The family has a set of fully programmable processors (highlighted in white in the roadmap below) targeted at the general

embedded market. The Symphony family of audio software enabled DPS are targeted at the audio market and are labeled in green.

The 24-bit general purpose processing family consists of a single MAC instruction architecture running up to 275 MHz with an enhanced filter coprocessor for math intensive (FFT and DFT) acceleration and peripherals targeted at mixed signal processing connectivity with SPI, HPI and chip memory features.

The 24-bit Symphony DSPs consists of single- and dual-core single MAC instruction architecture and are targeted at audio applications, including stereo headphones, guitar effects processors and echo cancellation headsets. These Symphony DSPs include multiple audio software codecs in the ROM, including fully certified Dolby Digital®, Pro Logic® IIx, WMA and multiple other audio software codecs. All available audio codes are listed on the next page. They also include key audio peripherals, such as SPDIF and audio serial ports.

## DSP56K Roadmap

### Dual Core

#### DSPA56721

- 2x 200 MIPS
- 248 kW RAM
- SPDIF/ASRC
- Dolby Digital +, DTS, PLIiz

#### DSPA56720

- 2x 200 MIPS
- 248 kW RAM
- SPDIF/ASRC
- Ext Bus
- Dolby TrueHD, DTS-MA, Dolby Volume, PLIiz

#### DSPB56721

- 2x 250 MIPS
- 248 kW RAM
- SPDIF/ASRC
- Ext Bus
- 144/80 LQFP

#### DSPB56720

- 2x 200 MIPS
- 248 kW RAM
- SPDIF/ASRC
- Ext Bus
- 144 LQFP

#### DSPB56725

- 2x 250 MIPS
- 112 kW RAM
- SPDIF/ASRC
- 80 LQFP

#### DSPB56724

- 2x 250 MIPS
- 112 kW RAM
- SPDIF/ASRC
- Ext Bus
- 144 LQFP

### Performance Optimized

#### DSP56311

- 150 MIPS
- 128 kW RAM
- 196 MAPBGA

#### DSP56321

- 275 MIPS
- 192 kW RAM
- 196 MAPBGA

### Cost Optimized

#### DSPD56374

- 150 MIPS
- 18 kW RAM
- Dolby Digital, PLIix, Dolby Headphone
- 80/52 LQFP

#### DSPC56371

- 150-180 MIPS
- 88 kW RAM
- Dolby Digital, DTS, AAC, WMA
- 80 LQFP

#### DSPD56371

- 150-180 MIPS
- 88 kW RAM
- Dolby Digital, DTS, Dolby Headphone
- 80 LQFP

#### DSPB56374

- 150 MIPS
- 18 kW RAM
- 80/52 LQFP

#### DSPB56371

- 150-180 MIPS
- 88 kW RAM
- 80 LQFP

- Including audio software in the ROM (Symphony)
- General purpose processor

## DSP56K Features

| Product Name | Cores | SPDIF Rx/Tx | ASRC | EFCOP | SHI | SCI | ESAI | ESSI | MAPBGA196 | 144LQFP | 80LQFP | 52LQFP | 248 kW RAM | 192 kW RAM | 128 kW RAM | 112 kW RAM | 88 kW RAM | 18 kW RAM | External Memory |
|--------------|-------|-------------|------|-------|-----|-----|------|------|-----------|---------|--------|--------|------------|------------|------------|------------|-----------|-----------|-----------------|
| 56374        | 1     |             |      |       | 1   |     | 2    |      |           |         | √      | √      |            |            |            |            |           | √         |                 |
| 56371        | 1     |             |      | 1     | 1   |     | 2    |      |           |         | √      |        |            |            |            |            | √         |           |                 |
| 56311        | 1     |             |      | 1     |     | 1   |      | 2    | √         |         |        |        |            |            | √          |            |           |           | √               |
| 56321        | 1     |             |      | 1     |     | 1   |      | 2    | √         |         |        |        |            | √          |            |            |           |           | √               |
| 56724        | 2     | 1           | 1    |       | 2   |     | 4    |      |           | √       |        |        |            |            |            | √          |           |           | √               |
| 56725        | 2     | 1           | 1    |       | 2   |     | 4    |      |           |         | √      |        |            |            |            | √          |           |           |                 |
| 56720        | 2     | 1           | 1    |       | 2   |     | 4    |      |           | √       |        |        | √          |            |            |            |           |           | √               |
| 56721        | 2     | 1           | 1    |       | 2   |     | 4    |      |           | √       | √      |        | √          |            |            |            |           |           | √               |

# DSP56K Core

The DSP56K family uses a programmable fixed point 24-bit 56300 core, which is a high-performance, single clock cycle per instruction computing engine optimized for DSP audio processing functionality. With the available double precision mode, 48-bit processing is possible with two 56-bit accumulators available to allow for arithmetic overflow. The 5672x devices enhance the family even further by providing a second 56300 core which doubles the MIPS available but at a highly

competitive price. Highly efficient coding is possible via the use of the dual-core architecture coupled with eight channel DMAs on each core to result in one of the most cost-efficient, highest performing audio processing solutions on the market.

The highly configurable memory switching options add to the flexibility of the devices and the addition of on-board audio peripherals, such as the S/PDIF receiver/transmitter and asynchronous sample rate converter (S/PDIF and ASRC on 5672x family only), allow for a highly integrated audio system with minimal bill of materials cost.

- Six- or eight-channel DMA controller
- Reduced power dissipation
  - Very low power CMOS design
  - Wait and Stop low-power standby modes
  - Fully-static logic

## Asynchronous Sample Rate Converter (ASRC)

The ASRC allows audio sample rate conversion between sources with independent clock domains. For example, a source with an 8 kHz sample rate along with a source with a 44.1 kHz sample rate could be input to the ASRC and output at a fixed sample rate of 48 kHz. It also allows for upsampling conversion or downsampling conversion with a range of 1/24 to eight (sampling frequency input to output). Up to 10 channels of conversion can occur with a maximum of three sampling rates at a time.

### Audio Decoders Available in Select Symphony ROMs

|   |
|---|
| PCM   |
| Multi-Channel PCM                           |
| Dolby Digital (2+5.1ch) *                   |
| Dolby Digital Extended Precision *          |
| Dolby Digital Plus *                        |
| Dolby Consumer Encoder *                    |
| Dolby TrueHD *                              |
| DTS *                                       |
| DTS-ES (Discrete/Matrix) *                  |
| DTS 96/24 *                                 |
| DTS-HD (Master Audio and High Resolution) * |
| MPEG-2 (5.1-ch.) *                          |
| MPEG-2 AAC (5.1-ch.) *                      |
| WMA Pro *                                   |

\*Dolby or DTS license required

## Key Elements of the 56300 Core

- 1 MIPS per MHz of operating speed
- Highly parallel instruction set
- Data arithmetic logic unit (Data ALU)
- Address generation unit (AGU)
- Program control unit (PCU)
- Phase locked loop (PLL)
- Hardware debugging support (JTAG TAP, OnCE module and address trace mode)

### Software Architecture Post Process Phases

| Freescal Developed PPPs        | Freescal Developed PPPs | Third-Party Developed PPPs*       |
|--------------------------------|-------------------------|-----------------------------------|
| Bass Manager                   | Parametric EQ           | Dolby Headphone                   |
| Bass Boost                     | Graphic EQ              | Dolby Virtual Speaker             |
| Fade/Balance                   | Pause Detection         | Dolby Pro Logic IIx/Pro Logic IIz |
| Compression                    | Spectrum Analyzer       | DTS Neo6                          |
| De-Emphasis                    | Tone Control            | DTS-ES (matrix)                   |
| DC-Cut                         | Prescaler               | Microsoft HDCD                    |
| Delay Manager                  | Beep                    | Neural Surround                   |
| Dynamic Range Compression      | Chime                   | SRS TruSurroundXT                 |
| Karaoke                        |                         | SRS Circle Surround               |
| Level Meter                    |                         | SRS Circle Surround II            |
| Loudness                       |                         | Waves MaxxBass                    |
| Noise Generator                |                         | QSurround                         |
| Reverb                         |                         | Dolby Volume                      |
| Soundfield/Concert Hall Effect |                         | Dolby Auto Entertainment          |
| Speaker Compensation           |                         |                                   |
| Volume Manager                 |                         |                                   |
| Gain Manager                   |                         |                                   |

\*Dolby, DTS or other license required

## SPDIF Receiver/Transmitter

The Sony/Philips Digital Interface (SPDIF) RX/TX is an easy way to get stereo or multi-channel into or out of the DSP without the need for an external transceiver chip. It allows the handling of both SPDIF channel status (CD) and user (U) data and includes a frequency measurement block that allows the precise measurement of an incoming sampling frequency.

## Enhanced Filter Coprocessor (EFCOP)

The EFCOP module functions as a general purpose, fully programmable filter. It has optimized modes of operation to perform real and complex finite impulse response (FIR) filtering, infinite impulse response (IIR) filtering, adaptive FIR filtering and multi-channel FIR filtering. The EFCOP operations work in parallel with the 56300 core operations with minimal CPU intervention required. It has a dedicated filter multiplier accumulator (FMAC) and so offers dual MAC capabilities when the 56300 core and EFCOP are used at the same time.

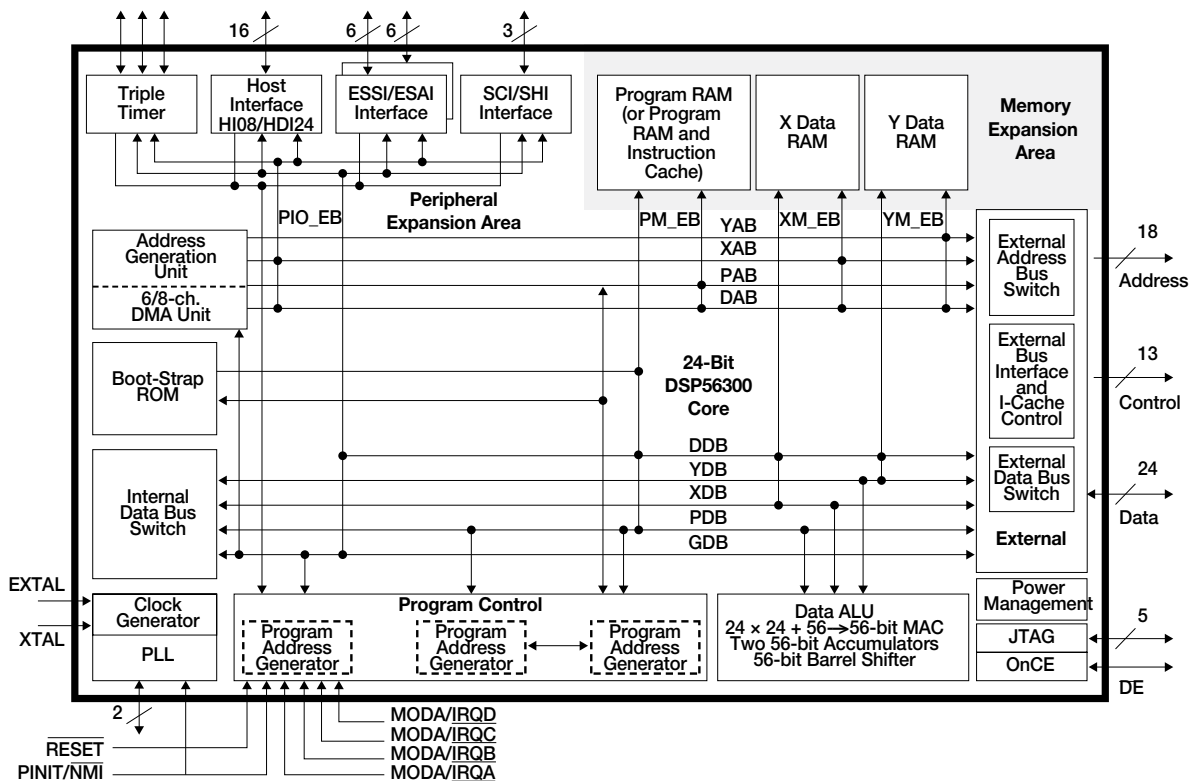
## Enhanced Serial Audio Interface (ESAI) and Enhanced Synchronous Serial Interface (ESSI)

Both of these peripherals provide very useful high-speed serial interfaces, ideally suited for communication and data transfer between the DSP and external ADCs, DACs and other codecs. The main difference between the two peripherals is the number of receiver and transmitters available. The ESSI provides one receiver and up to three transmitters whereas the ESAI provides six ports in total, two of which are dedicated transmitters with the other four configurable as transmitters or receivers. Note that the number of ESAI/ESSI peripherals available varies per DSP with up to four (24 total RX/TX pins) available on the 5672x series. Both the ESAI and ESSI support TDM and non-TDM modes and can be operated in synchronous (receiver and transmitter have the same bit clock and frame synch) or asynchronous (one set of clocks is generated internally and the other set is supplied externally) modes.

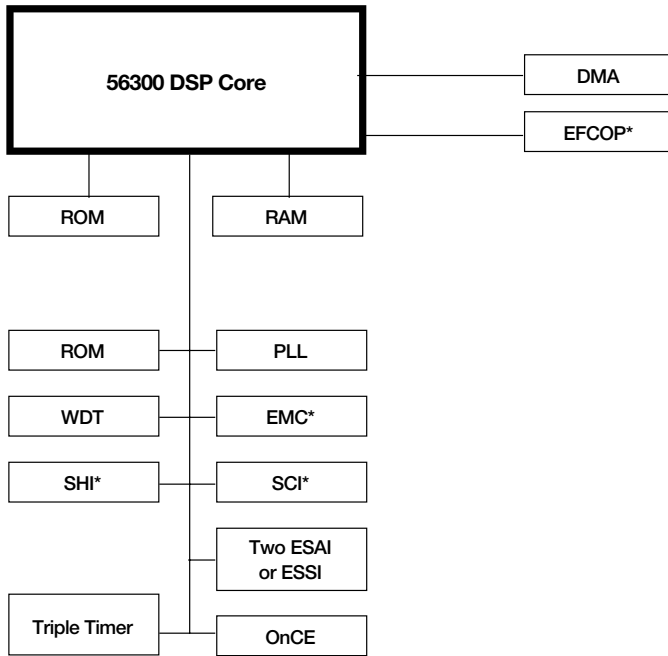
## Serial Host Interface (SHI) and Serial Communication Interface (SCI)

The SHI is a serial I/O interface that allows communication and data transfers between the DSP and an external host processor such as a microcontroller, microprocessor or serial EEPROM/flash. Both serial peripheral interface (SPI) and inter-integrated circuit (I<sup>2</sup>C) control modes are supported. The SHI can either be configured as a slave or single-master device depending on the system requirements and supports 8-bit, 16-bit and 24-bit data transfers. The SCI provides a full-duplex port for serial communication with other DSPs, microprocessor and other peripherals such as modems. The main difference between the SHI and the SCI is that the SCI can support asynchronous serial communication (e.g. RS232) whereas the SHI cannot. The SCI includes its own baud rate generator which can be used as a general purpose timer when not being used by the SCI.

56300 Core Diagram with Available Peripherals

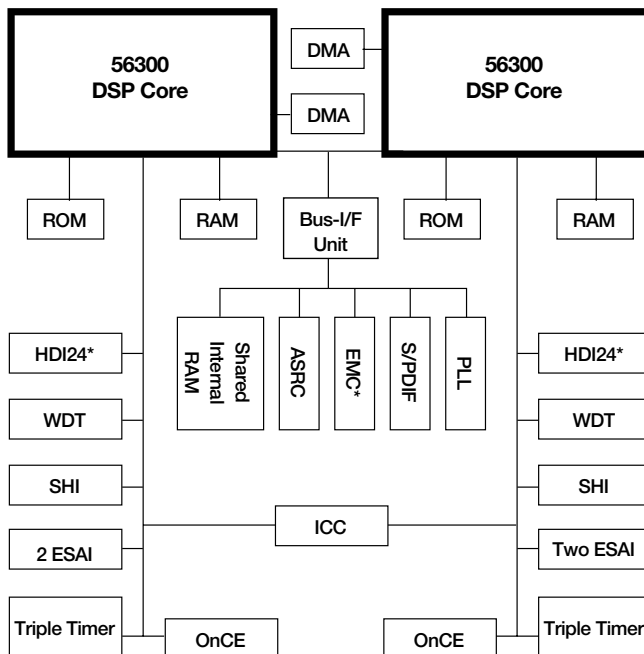


External addressing and HI08/HDI24 is only available on select 56K DSPs

**DSP563xx Single-Core Architecture**


\* Not on all devices

- Single 56300 DSP Core
- 6-ch. DMA
- Switchable memory configurations
- External memory available (56311/321)
- SCI (56311/321)
- SHI (56371/374)
- Complete audio software library (56371/374)
- Triple timer
- Two ESAI (56374/371)
- Two ESSI (56311/321)
- Watchdog timer (56374)
- Enhanced filter coprocessor (56371/311/321)

**DSP5672x Dual-Core Architecture**


\* Not on all devices

- Dual 56300 DSP cores
- 8-ch. DMA/per core
- Switchable memory configurations
- Complete audio software library (on specific devices)
- ASRC
- S/PDIF transmitter and receiver
- Serial host interface
- Four enhanced serial audio interfaces
- Two watchdog timers
- Host data interface (56721)



# Application Solutions

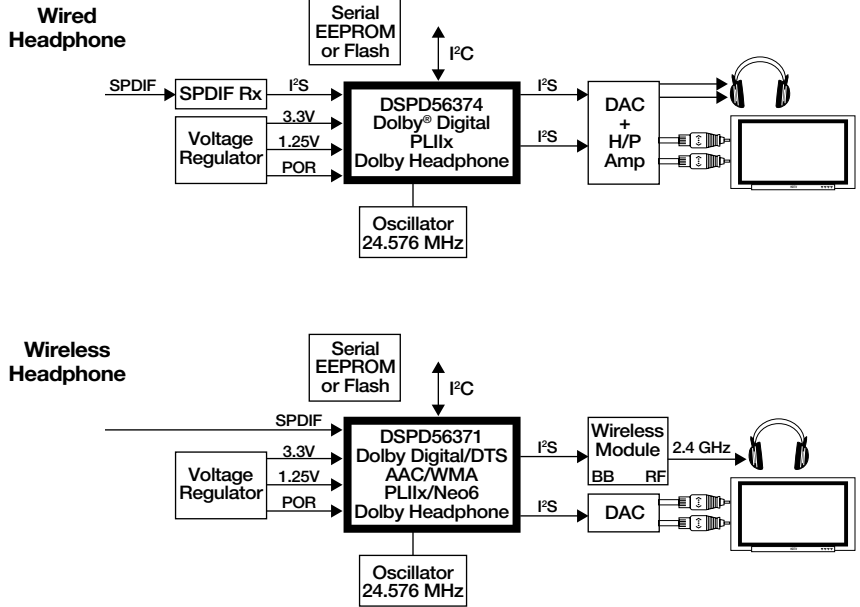
## Virtual Multi-Channel Headphone

The DSP56374 and DSP56371 devices are ideal for use in a virtual multi-channel headphone solution as they offer all the necessary decoding on one chip without the need for mass downloading of data to on-chip RAM. In fact, the system can even forgo a host microcontroller altogether and use the DSP for GPIO tasks such as LED lighting and mode selection. The DSP56374 offers fully certified Dolby Digital, Pro Logic IIx and Dolby Headphone capabilities on its custom ROM as does the DSP56371, which also adds DTS decoding as well as WMA and AAC if required. This part also includes an integrated S/PDIF receiver so an external device does not need to be used, reducing overall system costs. Boot-up can be done from a simple serial EEPROM or flash memory, which also helps to reduce cost.

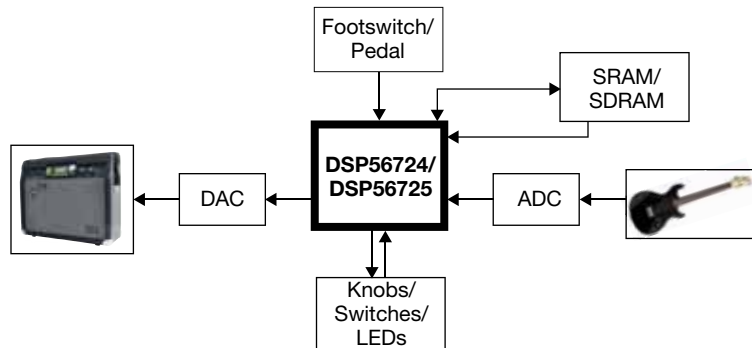
## Guitar Effects Pedal

The DSP56724 and DSP56725 devices are perfect for cost-effective audio instrument effects units such as guitar footswitches or “stomp” pedals. These DSPs offer a very cost-effective solution with substantial internal memory available (112K x 24-bit words of RAM) or an external memory bus (DSP56724 only) if needed. Coupled with the dual-core architecture, this allows customers to build an entire suite of effects, including delay, chorus, distortion, sustain, flange and reverb, into a compact module. These devices include many standard DSP tables in the ROM (e.g. sine, asine, atan, dB to linear, linear to dB, log to the base 2, log to the base 10, log to the base E) which may be useful for creating audio effects.

### Virtual Surround Headphone



### Guitar Effects Pedal





# **DSP56K Family Development Software, Tools and Reference Designs**

# Development Software

A wide range of development software is available to support the 56K DSP family, depending on the evaluation board used and the needs of the application.

## Suite56 (For use with all DSP56K devices)

Suite56 is the standard toolset compatible with all 56K DSP members, includes a basic compiler, linker and assembler and is recommended where basic debugging is required and assembly language is used for code development.

## Serial Debugger Interface (For use with Symphony software-enabled DSP56K devices)

The serial debugger interface is a serially based tool (using either I<sup>2</sup>C or SPI) used to emulate a host microcontroller in a system. It should be used with the DSPAUDIOEVM development tool with DSPs enabled with Symphony software (a special class of DSP with audio decoders embedded in the ROM). It offers a real-time interface which can be used to download and install post process phases (PPPs) and run the Symphony software architecture.

## Symphony Studio (For use with all DSP56K devices)

The Symphony Studio is a more advanced Eclipse-based tool which is based on the Suite56 toolset but comes with a more user friendly graphical interface. It can be used with more advanced applications where multiple files are used and dual-core debugging may be required. It includes a basic compiler, assembler and linker and can be used with assembly or C language programs. It is recommended that for more complex C programs, a third-party compiler should be used such as the one offered by Tasking .

### Development Tools Quick Reference Table

| EVM Board          | 56374 | 56371 | 56311 | 56321 | 56724 | 56725 | 56720 | 56721 | Cost           |
|--------------------|-------|-------|-------|-------|-------|-------|-------|-------|----------------|
| DSPAUDIOEVM        | yes   | yes   | no    | no    | yes   | yes   | yes   | yes   | \$1000/\$1150* |
| DSP563xxEVME       | no    | no    | yes   | yes   | no    | no    | no    | no    | \$400          |
| Symphony Soundbite | no    | yes   | no    | no    | no    | no    | no    | no    | \$150          |

| Software                  | 56374 | 56371 | 56311 | 56321 | 56724 | 56725 | 56720 | 56721 | Cost |
|---------------------------|-------|-------|-------|-------|-------|-------|-------|-------|------|
| Suite56                   | yes   | yes   | yes   | yes   | yes   | yes   | yes   | yes   | free |
| Serial Debugger Interface | yes** | yes** | no    | no    | yes** | yes** | yes** | yes** | free |
| Symphony Studio           | yes   | yes   | yes   | yes   | yes   | yes   | yes   | yes   | free |

\* Cost is quoted for motherboard and daughterboard:

Motherboard is \$750, 37x daughterboard is \$250, 72x daughterboard is \$400

\*\* Only used with Symphony-enabled members of the DSP56K

# DSPAUDIOEVM Evaluation Module

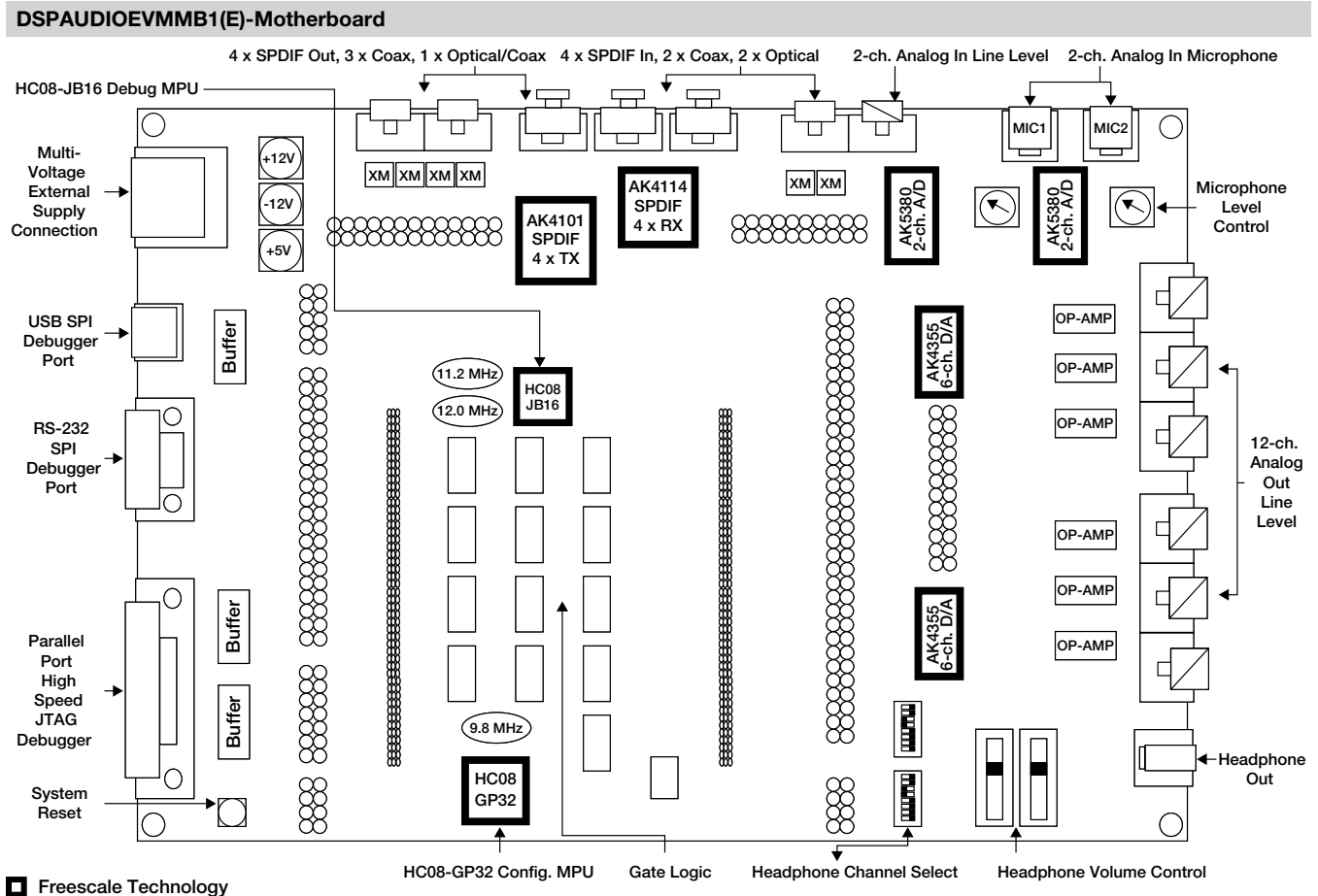
The \$750.00 USD DSPAUDIOEVM evaluation module provides a hardware tool to allow development of applications on the DSP5637x and DSP5672x devices. It consists of a generic motherboard (DSPAUDIOEVMMB1E) and a specific daughterboard corresponding to your DSP needs.

The \$750.00 USD DSPAUDIOEVM is designed for the following purposes:

- To allow new users to familiarize themselves with the features of the DSP5637x/5672x family architecture by exercising the product feature set.
- To serve as a platform for real-time software development, software download to on-chip or on-board RAM, software running and debug with

full speed operation and breakpoint capability and the ability to modify all user-accessible registers, memory and peripherals through the JTAG/OnCE port.

- To allow users to test and evaluate any audio decoders which may be contained in specific ROMs in the Symphony DSP family.



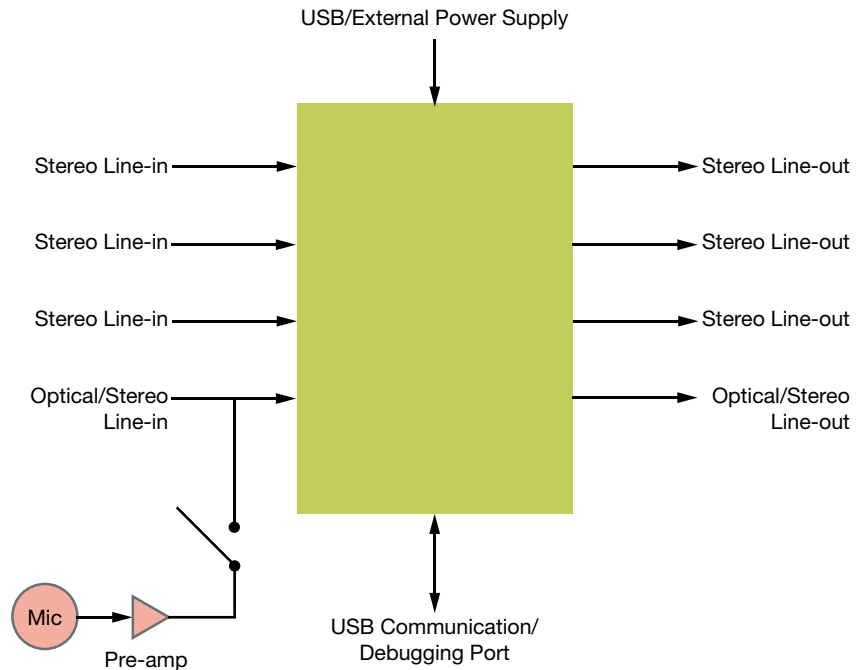
# Symphony SoundBite Development Kit

Freescale's \$150 USD MSRP Symphony SoundBite development kit is designed for cost-sensitive applications and college laboratories, providing a cost-efficient entry point into high-end DSP solutions.

The Symphony SoundBite development kit brings much of the performance of Freescale's full-featured evaluation module (DSPAUDIOEVMMB1E motherboard and DSPB371DB1 daughtercard) for the Symphony DSP56371 DSP to a more compact and user-friendly design at a very manageable price point. The Symphony SoundBite is capable of simultaneously processing eight independent channels of line-level audio via four pairs of 3.5 mm stereo jacks. One input/output pair of jacks is shared with the AKM S/PDIF receiver and transmitter, enabling optical digital audio input and output. The analog processing is handled by four AKM 24-bit stereo codecs at sampling rates up to 192 kHz. Multiple banks of DIP switches and multi-colored LEDs connected to the DSP's GPIO pins allow for user interaction with the DSP application.

The Symphony SoundBite development kit includes the Symphony SoundBite evaluation board, a mini USB cable and a CD-ROM with all the software and documentation needed to get started. An external power supply is recommended for optimum audio performance. The Symphony Studio software is now available for download at no charge. Go to [freescale.com/SymphonyStudio](http://freescale.com/SymphonyStudio) and click on the Download tab. The Symphony SoundBite evaluation board includes the Symphony DSP56371 processor on a small form-factor PCB, 256 KB serial (I<sup>2</sup>C) EEPROM memory, mini USB interface and a DIP switches for user inputs.

## High-Level Symphony SoundBite Overview



## Documentation

- Symphony SoundBite hardware reference guide and schematic
- Symphony DSP56300 family manual
- Symphony DSP56371 user's guide and data sheet
- Symphony SoundBite application examples

## Package

- 4 x 5 inch double sided PCB

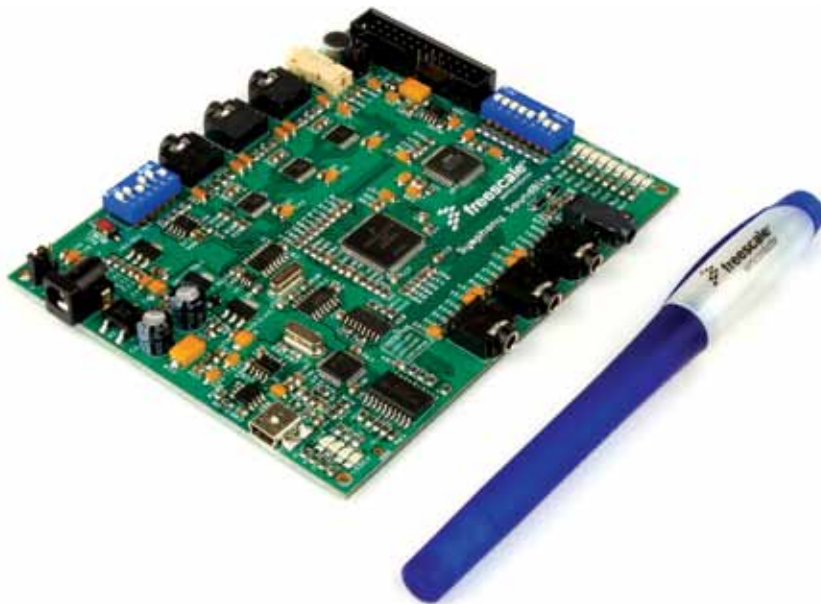


### Key Processor Features

- 24-bit Symphony DSPB56371 DSP, 180 (MIPS) at 180 MHz core clock
  - Dual-Harvard architecture core (two data memory spaces in addition to program space)
- On-chip memories:
- 4–44K x 24-bit words of PRAM
  - 28–36K x 24-bit words of XRAM
  - 16–48K x 24-bit words of YRAM
- Two ESAs provide up to eight channels of digital audio input and output
  - SHI allows for I<sup>2</sup>C or SPI communication

### Key Board Features

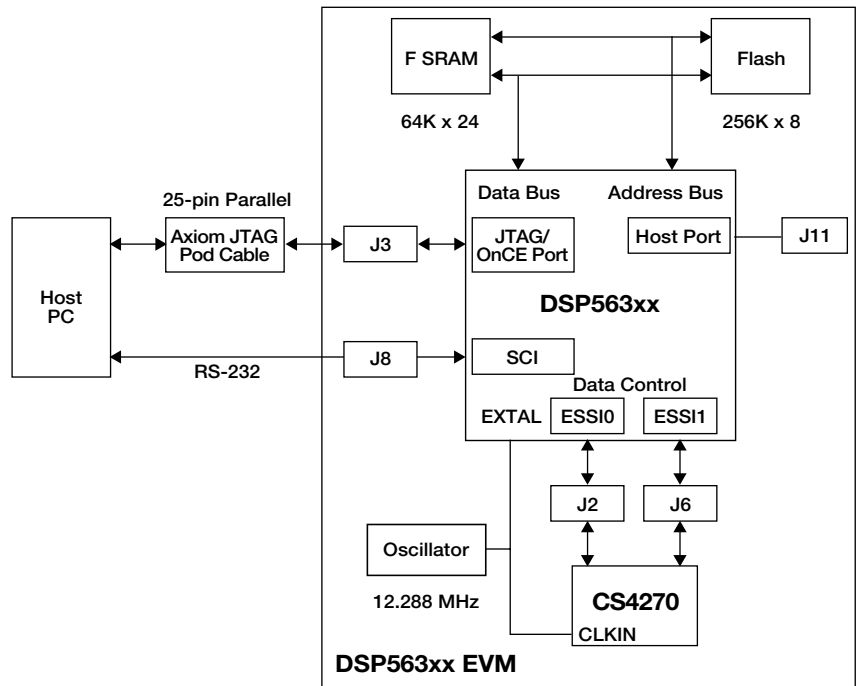
- Powered by USB bus voltage or external power adaptor
- On-board USB interface that provides JTAG debug, I<sup>2</sup>C and SPI serial communication with the DSP
- 1x AK4584 24-bit 192 kHz stereo codec with integrated S/PDIF transceiver
- 3x AK4556 24-bit 192 kHz stereo codecs
- On-board microphone and pre-amplifier
- Expansion header for off-board GPIO interfacing
- 8-position DIP input switch
- Nine LED indicators



# DSP563xx Evaluation Module (DSP563xxEVME)

The DSP563xx evaluation module is a cost-effective platform for developing real-time software and hardware products to support wireless, telecommunications, multimedia and other applications. It comes supplied with a socket and samples of the DSP56311 and DSP56321 DSPs.

## DSP563xx Evaluation Module





# Additional Resources

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For additional details on the products in this brochure, including technical documentation, application notes, software downloads and training, visit [freescale.com/DSP](http://freescale.com/DSP).

Support is available on the Freescale Forums page at [forums.freescale.com](http://forums.freescale.com).

To order samples or tools, contact your local Freescale Sales representative or your local authorized Freescale distributor.

# Ecosystem Partners

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## **ENE A—[enea.com](http://enea.com)**

OSEck RTOS, LINX message layer, network protocols. System level virtualization and debugging environments for system development on the MSC815x and MSC825x

## **Adaptive Digital—[adaptivedigital.com](http://adaptivedigital.com)**

G.PAK framework, G.168 echo cancellation, conferencing and transcoding software

## **GDA Technologies—[gdatech.com](http://gdatech.com)**

Hardware design services, evaluation module (AMC board)

## **Tata—[tataelxsi.com](http://tataelxsi.com)**

Media software development services

## **e2v—[e2v.com](http://e2v.com)**

Extended temperature testing, ruggedized packaging for extreme environments

## **Nuvation—[nuvation.com](http://nuvation.com)**

Embedded system design

## **Altium—[tasking.com/products/dsp56xxx/](http://tasking.com/products/dsp56xxx/)**

Tasking compiler for DSP56xxx devices. For applications where C programming is used extensively

## **Domain Technologies—[domaintec.com/FreescaleTools.html](http://domaintec.com/FreescaleTools.html)**

DSP56xxx debugging solutions

## **Quadros—[quadros.com/supported-processors/other-processors](http://quadros.com/supported-processors/other-processors)**

Real-time OS software is available for the DSP56311 and DSP56321

## **Micrium—[micrium.com/page/downloads/ports/freescale/dsp](http://micrium.com/page/downloads/ports/freescale/dsp)**

Real-time OS software is available for the DSP56311 and DSP56321

## **Rislin—[rislin.com](http://rislin.com)**

Media software and development services





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