EB00921

Time-Frequency Domain Thresholding (TFDT) Library Function

Rev. 1 — 11 January 2024 Engineering bulletin

1 Introduction

This Engineering bulletin describes updates for the following default configuration:

- Voltage detectors
- Clock dividers update for the startup self-test
- Utest flash content
- ADC threshold register value

2 Voltage detector

2.1 Description of the update

The core Cold voltage detector is disabled on the new device by updating the internal PMC_REE DCF Record.

Table 1. Voltage detector registers reset value update

Register name	Old value	New value
Reset Event Enable 0 (PMC_REE_0)	0000_7C98h	0000_7C90h
Reset Event Selection 0 (PMC_RES_0)	0000_0000h	0000_0008h

2.2 Reason

The reason for this update was because of the issue described in Errata ERR050129: PMC: VDD_LV_CORE is close to the Cold LVD threshold during the device startup.

Errata description:

When the internal regulator is used the VDD_LV_CORE may be up to 50 mV lower than nominal value when device leave the reset. This is caused by the oscillation on the reference voltage of the Power Management Controller (PMC) which is originated by internal coupling. When there is high current transient on IDD_LV during application start, VDD_LV_CORE drop can occur. Together with lower value of VDD_LV_CORE the Cold Low voltage detector (LVD) can be triggered and generates Destructive reset.

2.3 On which devices this change is implemented

This change is implemented on all the devices WW45 (144LQFP) and WW47 (257MAPBGA) 2022 onwards. If you are not sure the datecode (week) of your product, this change was implemented on all devices which have different value than 0xFFFF_FFFF at address 0x0040_00F0 in utest flash.

3 Clock dividers update for the startup self-test

3.1 Description of the update

The clock dividers which were programmed to divide by 2 for the startup self-test were changed to divide by 3.

3.2 Reason

The reason for this update was because of the issue described in the Errata ERR010639: MC_CGM: Auxiliary clock dividers get stuck if programmed to divide by 2 and a reset occurs during operation.

Errata Description:

When any functional reset or destructive reset (besides EXT_POR_B and power on/off) occurs during operation, any auxiliary clock divider in the Clock Generation Module (CGM) that is programmed to divide by 2 and is not sourced by the Internal RC Oscillator (IRCOSC) may get stuck and cannot subsequently be reprogrammed. **AUX0_DIV2, AUX1_DIV0, AUX1_DIV1 and AUX11_DIV0 dividers can also stuck during Startup self-test where they are programmed to divide by 2 by internal DCF record which cause LBIST2/3 fail.**

3.3 On which devices this change is implemented

This change is implemented on all the devices WW45 (144LQFP) and WW47 (257MAPBGA) 2022 onwards. If you are not sure the datecode (week) of your product, this change was implemented on all devices which have different value than 0xFFFF_FFFF at address 0x0040_00F0 in utest flash.

4 Utest flash content

4.1 Description of the update

Storing the LVD trimming values into the utest flash memory on the address range 0x0040_00F0 – 0x0040_00FB.

4.2 Reason

The reason for this update is the possible usage of the PMC_LVD_MISC DCF record for configuration the temperature sensor reaction because this record configure together with the temperature sensor reaction also the LVD trimming values.

Table 2. utest flash memory content update

utest flash memory range	Old value	New value
0x0040_00F0 – 0x0040_00F3	0xFFFF_FFFF	direct values of the LVDs trimming
0x0040_00F4 – 0x0040_00F7	0xFFFF_FFFF	inverted values of the LVDs trimming
0x0040_00F8 – 0x0040_00FB	0xFFFF_FFFF	1 bit right rotated LVDs trimming

4.3 On which devices this change is implemented

This change is implemented on all the devices WW45 (144LQFP) and WW47 (257MAPBGA) 2022 onwards. If you are not sure the datecode (week) of your product, this change was implemented on all devices which have different value than 0xFFFF_FFFF at address 0x0040_00F0 in utest flash.

4.4 How the temperature sensor DCF record should be programmed

The PMC_LVD_MISC DCF record which programs the temperature sensor reset reaction and LVD trimming values are triple voting DCF record. It means that it is programmed by three record where the first content is the direct data, second is the inverted data and the third one is the rotated data. This is the reason why LVD trimming values are stored in this format in the utest flash. By default the temperature sensor reset reaction are disabled.

Table 3. PMC_LVD_MISC DCF record description

PMC_LVD_MISC DCF record	DCF data	DCF control word
Direct	0bRRRT_TTRR_LLLL_LLLL_LLLL_LLLL_LLLL_LLLL*[1][1]	0x0040_0144
Negative	0brrr_ttrr_llll_llll_llll_llll_llll_llll*[1]	0x0040_0148
Rotate	0bLRRR_TTTR_RLLL_LLLL_LLLL_LLLL_LLLL_LLLL*[1]	0x0040_0150

[1] R – Reserved, T – Temperature sensors configuration, L – LVD trimming value; the small letters mean negation bits of the capital ones.

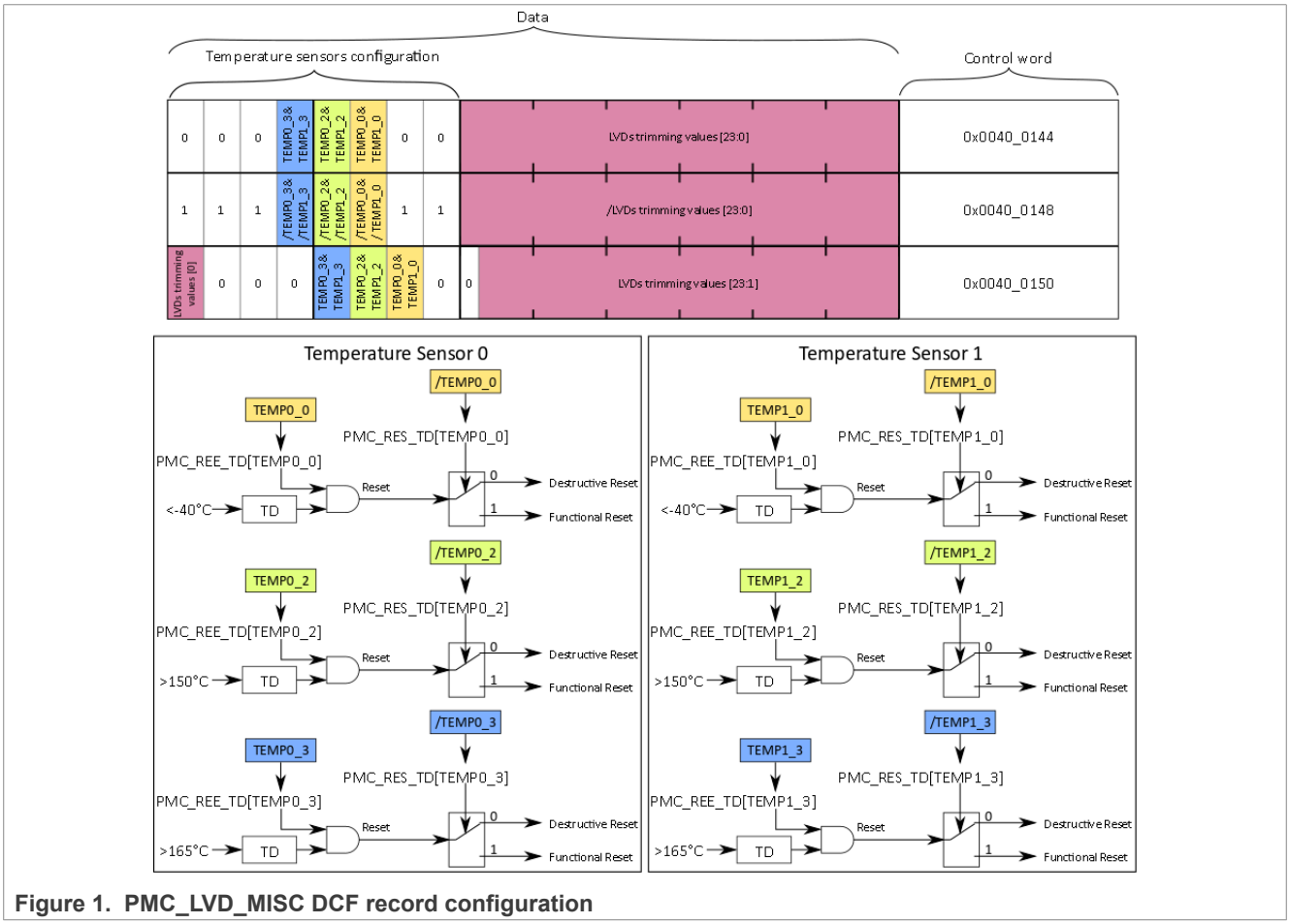

Figure 1. PMC_LVD_MISC DCF record configuration

4.5 Example of the PMC_LVD_MISC DCF record configuration

The following example will enable the destructive reset reaction for both temperature sensors for cold (-40 deg) and hot (150 deg) detectors.

1. Create direct DCF record:

Table 4. Example of the DCF configuration

PMC_LVD_MISC DCF record	Temperature sensors configuration[1]	LVD trimming values[2]	DCF record data[3]
direct	0x0C	0x23_4567	0x0C23_4567

[1] Temperature sensors configuration = 0x0C for destructive reset reaction for both temperature sensors for cold (-40 deg) and hot (150 deg) detectors.

[2] Read direct LVD trimming values [23:0] from utest flash memory 0x0040_00F1 – 0x0040_00F3.
[3] Direct DCF record = (Temperature sensors configuration << 24)| LVD trimming values = (0x0C << 24) | 0x23_4567 = 0x0C23_4567

2. Negative DCF record = NOT (direct DCF record) = NOT (0x0C23_4567) = 0xF3DC_BA98
3. Rotate DCF record = ROTATE_RIGHT_ONE_BIT (direct DCF record) = ROTATE_RIGHT_ONE_BIT (0x0C23_4567) = 0x8611_A2B3
4. Program following DCF records into the utest flash memory DCF records area: 0x0C23_4567_0040_0144, 0xF3DC_BA98_0040_0148, 0x8611_A2B3_0040_0150.

5 ADC threshold register value

5.1 Description of the update

The default threshold values for capacitive self test (algorithm C step 0) stored in the Self Test Analog Watchdog Register 4 (STAW4R) was changed by updating the ADC self test threshold values in the utest flash.

Table 5. STAW4R register value update

Update staff	Old value	New value
Address 0x0040_00E4	0xF010_FFF0	0xF034_FFCC
Register ADC_STAW4R	0x0010_0FF0	0x0034_0FCC

5.2 Reason

The original thresholds values (+/- 16) were derived from the measurement in clean environment. However, in the real application there is noise caused by board, power supply and other factors. Therefore, the thresholds values were changed to +/-52 to pass the ADC self test in real application where the MCU is used.

The test are carried for both the thresholds +/-16 and +/-52, so the devices with the new DCF record (ADC STAW4R default value) will be tested same as in the past. It also passes the self test in the noisy (real) environment.

5.3 On which devices this change is implemented

This change is implemented on all the devices WW45 (144LQFP) and WW47 (257MAPBGA) 2022 onwards. If you are not sure the datecode (week) of your product, this new threshold values were implemented there when ADC_STAW4R register reset value is 0x0034_0FCC.

6 Revision history

Table 6. Revision history

Revision Number	Release Date	Changes
1	11 January 2024	Updated the text in the following sections: • On which devices this change is implemented • On which devices this change is implemented • On which devices this change is implemented • On which devices this change is implemented
0	06/2021	Initial release

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