Functional Differences Between the DSP56311 and DSP56321

The DSP56311 and DSP56321, two members of the Freescale DSP56300 family of programmable digital signal processors (DSPs), support network applications with general filtering operations. Like other DSP56300 family members, these devices preserve code compatibility. Unique to each of these devices is an on-chip enhanced filter coprocessor (EFCOP) that executes filter algorithms in parallel with core operations to provide enhanced signal quality without affecting channel throughput or total number of channels supported, resulting in increased performance overall.

Although the DSP56311 and DSP56321 have similar features, they differ in several ways. This document describes these functional differences.

CONTENTS

1 Migration Considerations

The DSP56311 uses the Freescale HiP4 process. The DSP56321 uses the latest Freescale process technology: HiP7. The migration from the HiP4 to the HiP7 process decreases the core voltage; increases the maximum operating frequency; and changes specific pin definitions, the chip thermal characteristics, the JTAG and Device Identification register contents, internal memory size, memory mapping, shared EFCOP/core memory size, SRAM and DRAM access, Operating Mode Register (OMR) bit definitions, clock/phase-lock loop (PLL) module to a DPLL circuit with different

configuration registers, and packaging. The following sections address the hardware and software implications for migrating DSP56311 designs to DSP56321 designs.

Note: Minor changes are required for correct system operation if a DSP56321 is substituted for a DSP56311 in a design. Freescale does not guarantee correct operation if you do not implement the required design changes described in this document.

2 Summary of Differences

Table 1 summarizes the differences between the DSP56311 and the DSP56321 and references the sections of this document that describe the differences in detail.

Table 1. Differences Between DSP56311 and DSP56321

Feature	See Section	DSP56311	DSP56321
Voltage	**3**	1.8 V ± 0.1 V (separate core and PLL)	1.6 V ± 0.1 V (shared core and DPLL)
Target operating frequency	**4**	150 MHz	275 MHz
Pin definition differences	**5**	V_{CCP}, V_{CCP1}, and GND_P are power and ground dedicated for PLL use. PCAP connects to special PLL capacitor. $\overline{CAS}$, $\overline{RAS}$, $\overline{BCLK}$, BLCK, and CLKOUT used to support DRAM and Address Trace Mode (≤100 MHz only).	Core and DPLL use the same power and ground supplies. The old V_{CCP} pin is used as a V_{CCQL} connection. The old GND_P and GND_{P1} pins are used as GND_Q connections, but are simply designated as GND for the chip pinout because all GND connections must be connected together. PCAP is not connected (NC). $\overline{CAS}$, $\overline{RAS}$, $\overline{BCLK}$, BCLK, and CLKOUT functions are not supported.
Thermal characteristics	**6**	θ_{JA} = 49 °C/W θ_{JC} = 10 °C/W	$R_{\theta JA}$ = 44 °C/W $R_{\theta JC}$ = 7 °C/W The data sheet also specifies new values: $R_{\theta JMA}$: 2s2p, Natural = 25 °C/W 1s, 200 ft/min air flow = 35 °C/W 2s2p, 200 ft/min air flow = 22 °C/W $R_{\theta JB}$ = 13 °C/W
ID registers	**7**	Device ID (IDR) = $000311 JTAG ID = $0180B01D	Device ID (IDR) = $000321 JTAG ID = $0181501D
Internal memory	**8**	128 K × 24-bit on-chip SRAM	192 K × 24-bit on-chip SRAM
Memory maps	**9**	Memory map includes five switch options (including default)	Memory map includes eight switch options (including default)
EFCOP/Core shared memory	**10**	10 K × 24-bit	12 K × 24-bit
SRAM access wait states	**11**	Accesses at 100 MHz or less require at least 1 wait state. Accesses above 100 MHz to 150 MHz require at least 2 wait states. Programming the Bus Control Register for 2–7 wait states adds 1 trailing wait state. Selecting 8 or more wait states adds 2 trailing wait states.	Accesses at 275 MHz require a minimum of 3 wait states. Programming the Bus Control Register for 3–7 wait states adds 1 trailing wait state. Selecting 8 or more wait states adds 2 trailing wait states.
DRAM support	**12**	DRAM is supported to 100 MHz	DRAM is not supported.
Operating Mode Register (OMR)	**13**	Bits 22 and 21 are MSW[1–0], bit 7 is MS	Bits 22,21,7 are MSW[2–0] to increase the number of switch options; bit 15 (Address Trace Enable) is undefined.

Table 1. Differences Between DSP56311 and DSP56321 (Continued)

Feature	See Section	DSP56311	DSP56321
Clock/PLL	**14**, **15**	Standard DSP56300 PLL and non-synthesized clock block	DPLL (without PCAP) and a new synthesized, scannable, clock block.
Peripheral timing	**16**	Based on 150 MHz. Timing expressions use HiP4 delay constants.	Based on 275 MHz. Timing expressions use HiP7 delay constants.
Package	**17**	15 mm × 15 mm 196-pin Molded Array Process-Ball Grid Array (MAP-BGA)	15 mm × 15 mm 196-pin Flip Chip-Plastic Ball Grid Array (FC-PBGA)

3 Voltage

The DSP56311 and DSP56321 are dual-voltage devices. The DSP56311 core operates from a 1.8 ± 0.1 V supply, while the DSP56321 core and DPLL operate from a 1.6 ± 0.1 V supply. The input/output pins on each device operate from an independent 3.3 V supply. Using a variable supply for the core voltage allows designers to use the same board design for either device.

4 Operating Frequency

The maximum operating frequency for the DSP56311 is 150 MHz compared to 275 MHz for the DSP56321.

5 Pin Definitions

Due to the change from the standard DSP56300 phase-lock loop (PLL) design to the new digital phase-lock loop (DPLL) and clock block on the DSP56321, the PCAP pin is no longer necessary and the DSP56321 does not require a separate PLL power source. The PCAP connection is changed to *NC*. V_{CCP} connects to the core power V_{CCQL} and GND_P and GND_{P1}connect to system GND. Since DRAM support and Address Trace Mode are not included in the DSP56321, the $\overline{CAS}$, $\overline{BCLK}$, BCLK, and CLKOUT signals are not supported. $\overline{CAS}$ and $\overline{BCLK}$ are disconnected internally (*NC*). BCLK and CLKOUT are *Reserved*. The RAS[0–3] functions are also not supported. The *DSP56321 Technical Data* sheet provides details on the chip pin-out.

Table 2. Pin Differences Between the DSP56311 and DSP56321

Signal Package Reference Number	DSP56311	DSP56321
M6	V_{CCP}	V_{CCQL}
M9	CLKOUT	Reserved[1]
M10	BCLK	NC[2]
N6	GND_P	GND
N7	AA3/$\overline{RAS3}$	AA3
N8	CAS	NC[2]
N10	BCLK	Reserved[1]
N13	AA0/$\overline{RAS0}$	AA0
P5	PCAP	NC[2]
P6	GND_{P1}	GND
P7	AA2/$\overline{RAS2}$	AA2
P12	AA1/$\overline{RAS1}$	AA1

Table 2. Pin Differences Between the DSP56311 and DSP56321 (Continued)

Signal Package Reference Number	DSP56311	DSP56321

Notes: 1. These pins are connected internally and are reserved. Legacy designs with connections for CLKOUT or BCLK can remain unchanged, but support for CLKOUT and BCLK is not guaranteed at any frequency.

2. These pins are not connected internally. No connection modifications to legacy designs are required for correct operation.

6 Thermal Characteristics

Table 3. Summary of Differences Between the 196-Pin MAP-BGA and FC-PBGA Packages

Characteristic	DSP56311	DSP56321
Θ_{JA} (°C/W)	49 (no airflow)	50 (no airflow)—simulated. Actual data TBD.
Θ_{Jc} (°C/W)	10	0.1—simulated. Actual data TBD.

7 ID Registers

The DSP56300 core provides a dedicated user-accessible test access port (TAP) based on the *IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture*. With the IDCODE instruction, a user can determine from the TAP ID Register information about the manufacturer, part number, and version of a board component. The ID register is updated to reflect information specific to the DSP56321. **Figure 1** shows the specified register contents for the DSP56311 and DSP56321.

	31–28	27–22	21–12	11–1	0
Device	**Version Information**	**Design Center Number**	**Sequence Number**	**Manufacturer Identity**	**1**
DSP56311	0000	000110	0000001011	00000001110	1
DSP56321	0000	000110	0000010101	00000001110	1

Figure 1. JTAG Identification Register Contents for DSP56311 and DSP56321

The device Identification Register (IDR) is a 24-bit, read-only factory-programmed register that identifies DSP56300 family members. It specifies the derivative number and revision number of the device. This information is used in testing or by software. The IDR is updated to reflect information specific to the DSP56321. **Figure 2** shows the specified register contents for the DSP56311 and DSP56321.

	23–16	15–12	11–0
Device	**Reserved**	**Revision Number**	**Derivative Number**
DSP56311	$00	$0	$311
DSP56321	$00	$0	$321

Figure 2. Identification Register Contents for DSP56311 and DSP56321

8 Internal Memory Size

The DSP56311 has a total of 128 K × 24-bit on-chip SRAM compared to a total of 192 K × 24-bit on-chip SRAM in the DSP56321. In both devices, SRAM is partitioned into program memory space (P), and two data memory spaces (X and Y). The program memory space (P) includes internal Program RAM, an optional internal Instruction Cache[1], a boot program ROM, and an optional off-chip memory expansion. The data memory space is divided into

X- and Y-data memory in order to work with the two address arithmetic logic units (ALUs) and to feed two operands simultaneously to the data ALU. Each data memory space includes internal RAM and an optional off-chip memory expansion. The X- and Y-data memory share a 10 K word memory block with the EFCOP in the DSP56311 (20 K words total) and a 12 K word memory block in the DSP56321 (24 K words total).

Figure 3 shows the default memory block diagram for the DSP56311. **Figure 4** shows the default memory block diagram for the DSP56321

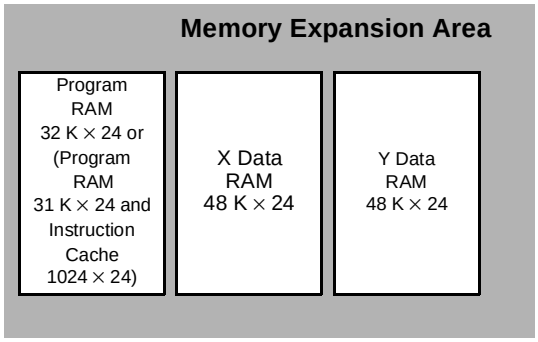


Figure 3. DSP56311 Default Memory Block Diagram

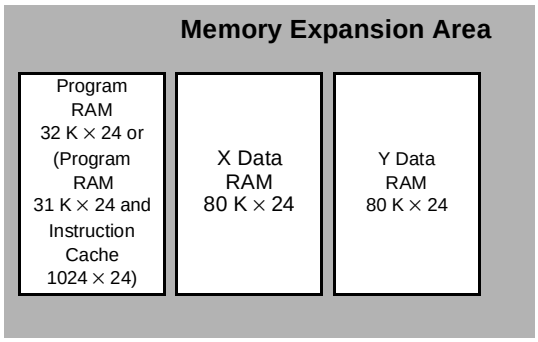


Figure 4. DSP56321 Default Memory Block Diagram

The amount of internal RAM partitioned between program and data RAM depends on the values written to four bits:

- *Cache Enable bit (CE) in the Status Register*. When the CE bit is set, the Instruction Cache is enabled and the lowest 1K of internal Program RAM is reserved as Instruction Cache. When the cache is enabled, the address range is switched to address external memory and the internal memory area becomes inaccessible.
- *Memory Switch Mode bits (MSW[2–0]—OMR[22, 21, and 7]).*The DSP56311 uses the MS bit (OMR[7]) to select Memory Switch Mode and the MSW[1–0] bits (OMR[22–21) to select the alternate memory maps when the mode is selected; this results in five selections: one default setting and four alternate settings. In the DSP56321, the Operating Mode Register (OMR) is redefined so that the same three bits (OMR[22, 21, 7]) make up a 3-bit Memory Switch Mode register. If all three bits

1. When the cache is disabled, the memory space used for the Instruction Cache becomes available as internal program RAM. When the cache is enabled, the on-chip cache memory space is inaccessible and the address range for this space is assigned to external program memory.

are zero, the default mode is selected. When any MSW bit is set, the Memory Switch Mode is enabled, and portions of the internal X and Y data memory become part of the on-chip internal Program RAM. The amount of X and Y data memory that becomes part of Program RAM depends on the MSW bits, the Memory Switch Configuration bits (MSW[2–0], bits 22,21, and 7 in the Operating Mode Register). The MSW bits define eight different X and Y data memory and internal Program RAM configurations, including the default configuration.

Table 4 (DSP56311) and **Table 5** (DSP56321) show partitioning of on-chip RAM in the DSP56311 and DSP56321 relative to these bit settings.

Table 4. DSP56311 Switch Memory Configuration

Program RAM Size	Instruction Cache Size	X Data RAM Size*	Y Data RAM Size*	Instruction Cache (CE)	Switch Mode (MS)	MSW1	MSW0
32 K × 24-bit	0	48 K × 24-bit	48 K × 24-bit	disabled	disabled	0/1	0/1
31 K × 24-bit	1024 × 24-bit	48 K × 24-bit	48 K × 24-bit	enabled	disabled	0/1	0/1
96 K × 24-bit	0	16 K × 24-bit	16 K × 24-bit	disabled	enabled	0	0
95 K × 24-bit	1024 × 24-bit	16 K × 24-bit	16 K × 24-bit	enabled	enabled	0	0
80 K × 24-bit	0	24 K × 24-bit	24 K × 24-bit	disabled	enabled	0	1
79 K × 24-bit	1024 × 24-bit	24 K × 24-bit	24 K × 24-bit	enabled	enabled	0	1
64 K × 24-bit	0	32 K × 24-bit	32 K × 24-bit	disabled	enabled	1	0
63 K × 24-bit	1024 × 24-bit	32 K × 24-bit	32 K × 24-bit	enabled	enabled	1	0
48 K × 24-bit	0	40 K × 24-bit	40 K × 24-bit	disabled	enabled	1	1
47 K × 24-bit	1024 × 24-bit	40 K × 24-bit	40 K × 24-bit	enabled	enabled	1	1
*Includes 10 K × 24-bit shared memory (that is, memory shared by the DSP56300 core and the EFCOP)							

Table 5. DSP56321 Switch Memory Configuration

Program RAM Size	Instruction Cache Size	X Data RAM Size*	Y Data RAM Size*	Instruction Cache (CE)	MSW2	MSW1	MSW0
32 K × 24-bit	0	80 K × 24-bit	80 K × 24-bit	disabled	0	0	0
31 K × 24-bit	1024 × 24-bit	80 K × 24-bit	80 K × 24-bit	enabled	0	0	0
40 K × 24-bit	0	76 K × 24-bit	76 K × 24-bit	disabled	0	0	1
39 K × 24-bit	1024 × 24-bit	76 K × 24-bit	76 K × 24-bit	enabled	0	0	1
48 K × 24-bit	0	72 K × 24-bit	72 K × 24-bit	disabled	0	1	0
47 K × 24-bit	1024 × 24-bit	72 K × 24-bit	72 K × 24-bit	enabled	0	1	0
64 K × 24-bit	0	64 K × 24-bit	64 K × 24-bit	disabled	0	1	1
63 K × 24-bit	1024 × 24-bit	64 K × 24-bit	64 K × 24-bit	enabled	0	1	1
72 K × 24-bit	0	60 K × 24-bit	60 K × 24-bit	disabled	1	0	0
71 K × 24-bit	1024 × 24-bit	60 K × 24-bit	60 K × 24-bit	enabled	1	0	0
80 K × 24-bit	0	56 K × 24-bit	56 K × 24-bit	disabled	1	0	1
79 K × 24-bit	1024 × 24-bit	56 K × 24-bit	56 K × 24-bit	enabled	1	0	1
96 K × 24-bit	0	48 K × 24-bit	48 K × 24-bit	disabled	1	1	0
95 K × 24-bit	1024 × 24-bit	48 K × 24-bit	48 K × 24-bit	enabled	1	1	0
112 K × 24-bit	0	40 K × 24-bit	40 K × 24-bit	disabled	1	1	1
111 K × 24-bit	1024 × 24-bit	40 K × 24-bit	40 K × 24-bit	enabled	1	1	1
*Includes 12 K × 24-bit shared memory (that is, memory shared by the DSP56300 core and the EFCOP)							

9 Memory Mapping

Figure 5 shows a memory map configuration of program memory switching for the DSP56311. **Figure 6** shows a memory map configuration of program memory switching for the DSP56321.

Figure 5. DSP56311 Program Memory Switching Configuration

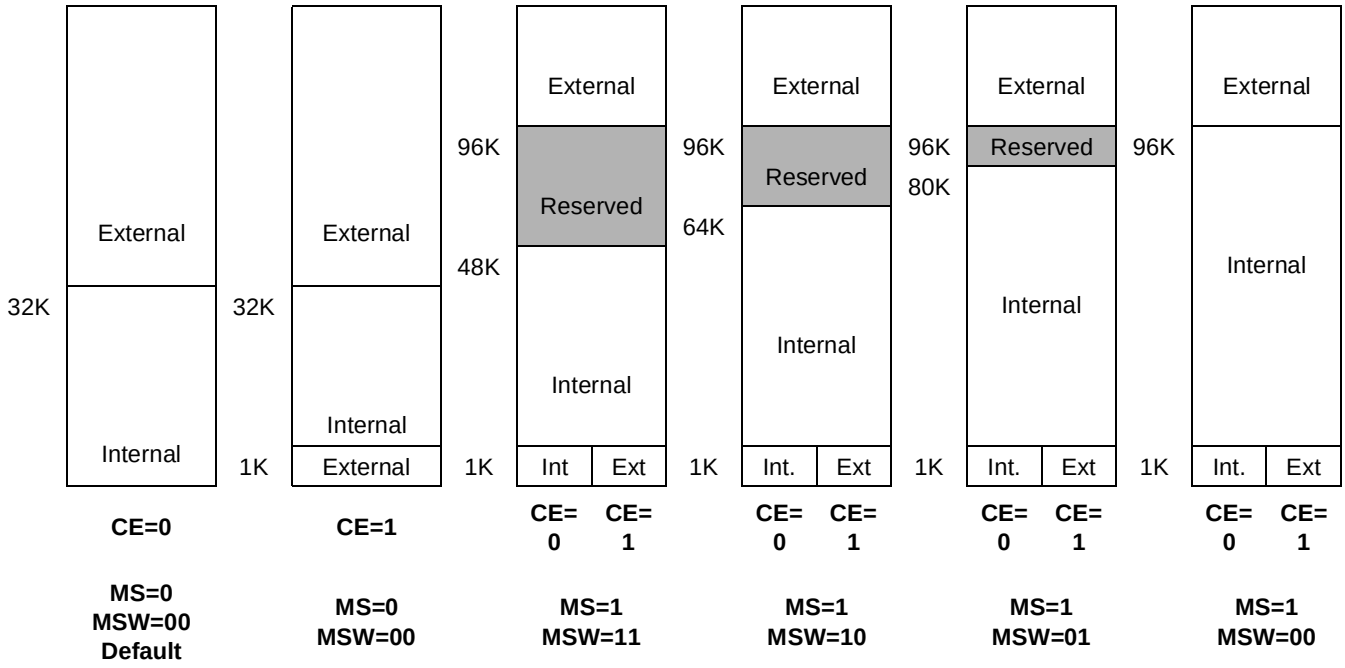


Figure 6. DSP56321 Program Memory Switching Configuration

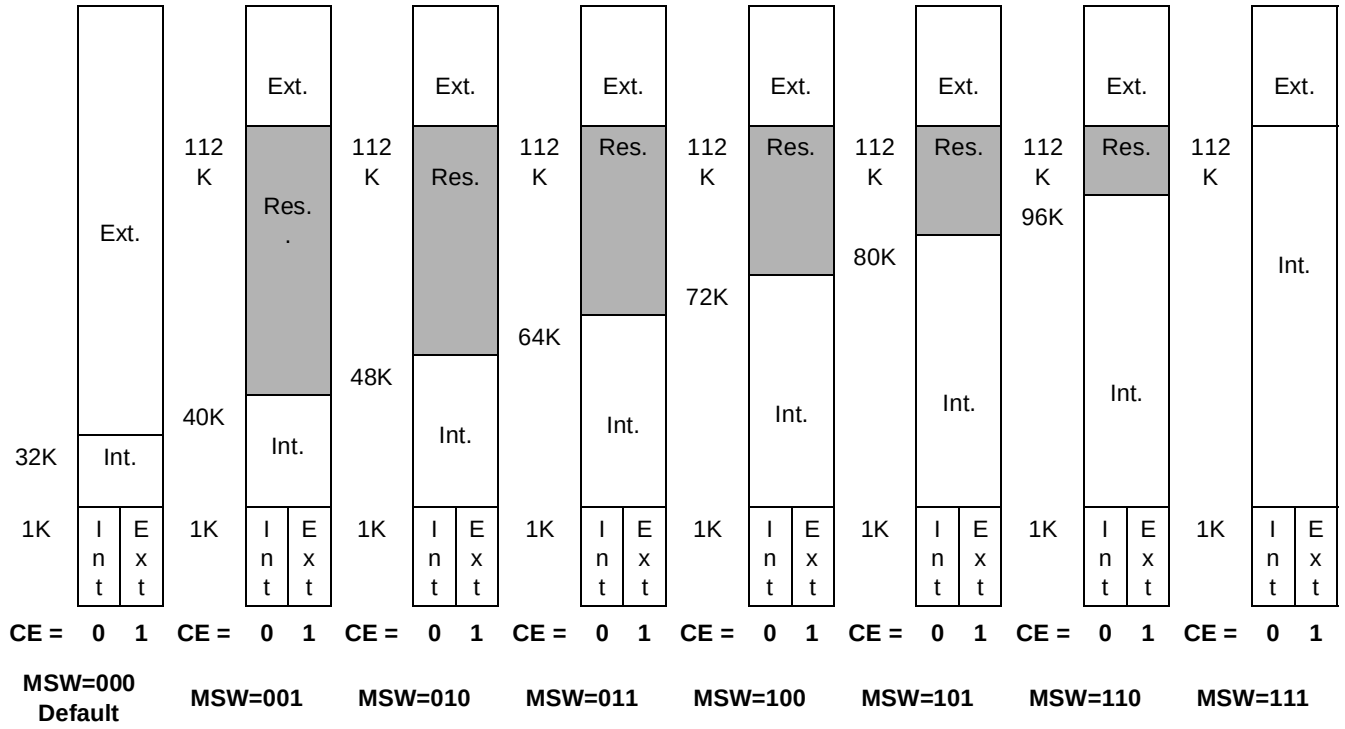


Figure 7 shows a memory map configuration of X and Y data memory switching for the DSP56311. **Figure 8** shows a memory map configuration of X and Y data memory switching for the DSP56321.

Figure 7. DSP56311 X and Y Data Memory Switching Configuration

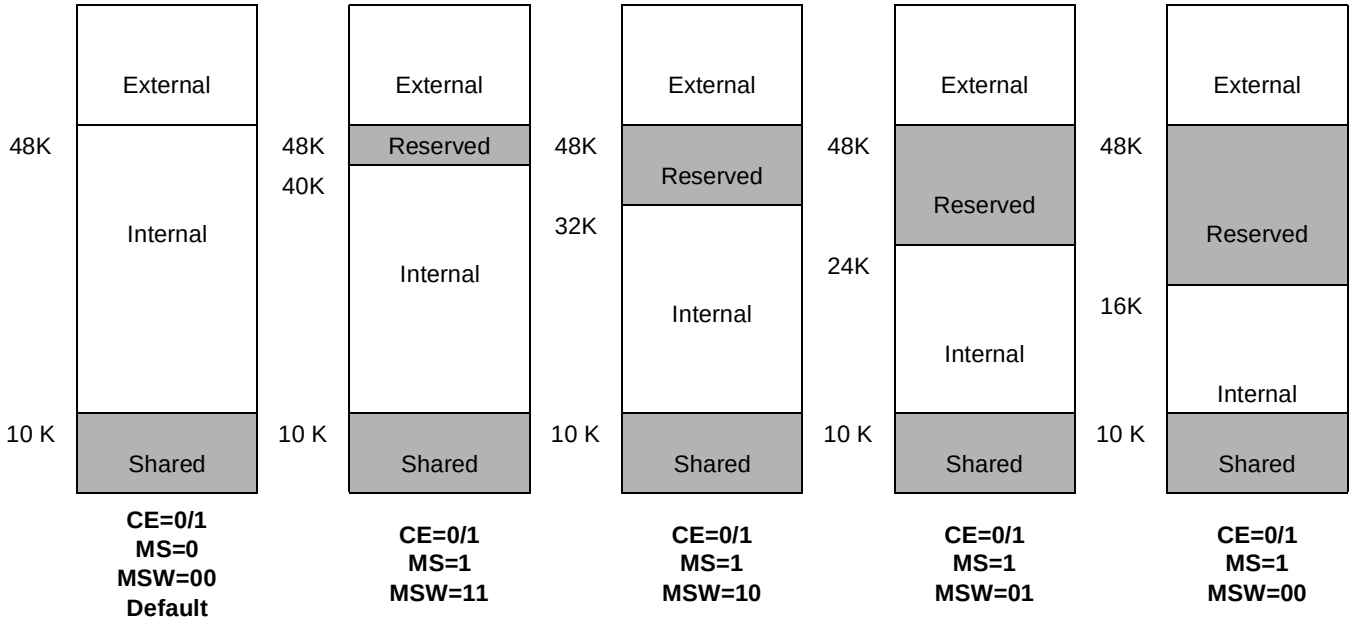
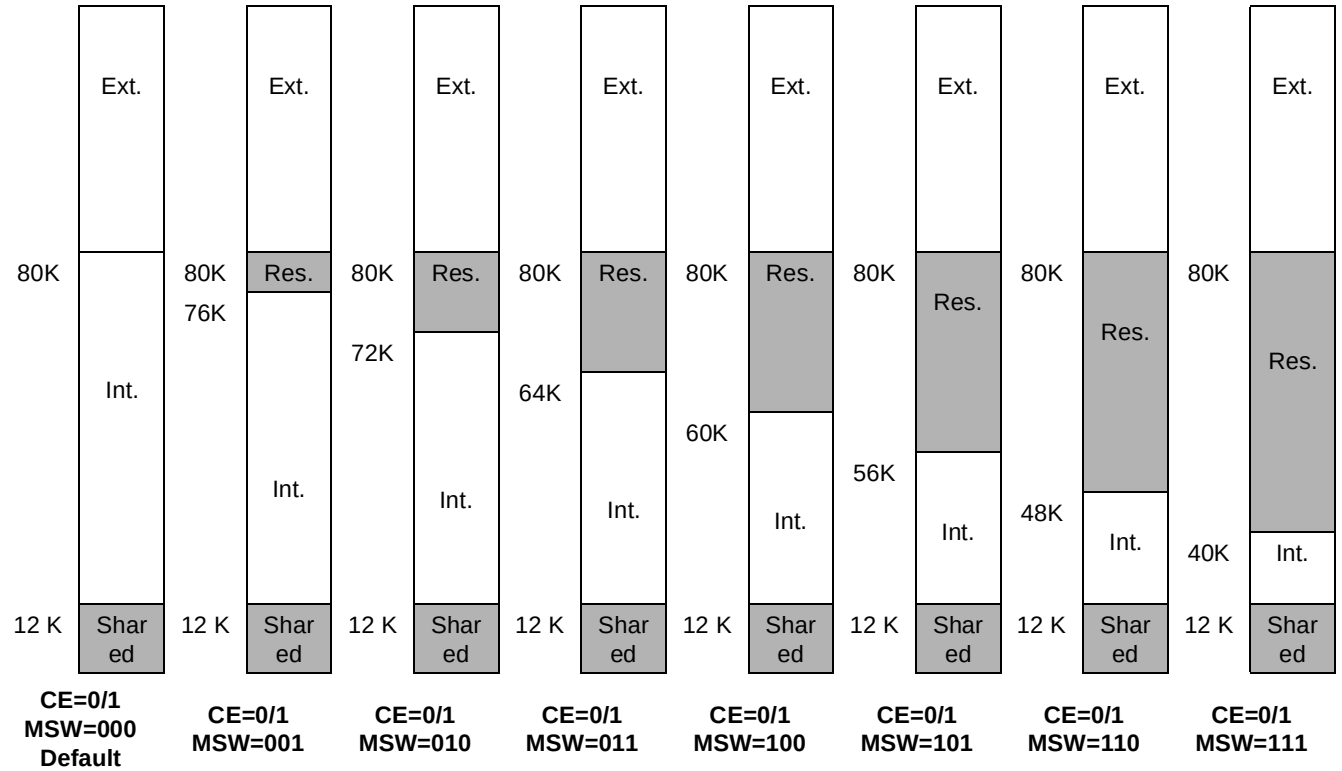


Figure 8. DSP56321 X and Y Memory Switching Configuration



Sixteen-bit Compatibility mode also affects the memory configuration for these devices. **Figure 9** and **Figure 10** show the effect of Sixteen-bit Compatibility mode on the memory map.

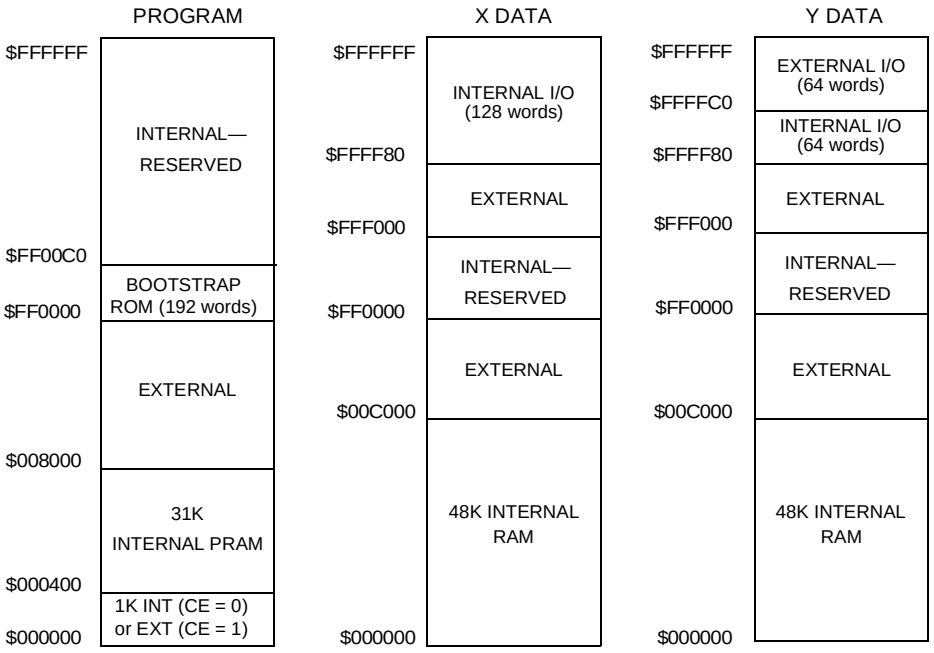


Figure 9. DSP56311 Memory Map—MS = 0 and SC = 0
Memory Switch Mode Disabled, Sixteen-bit Compatibility Mode Disabled

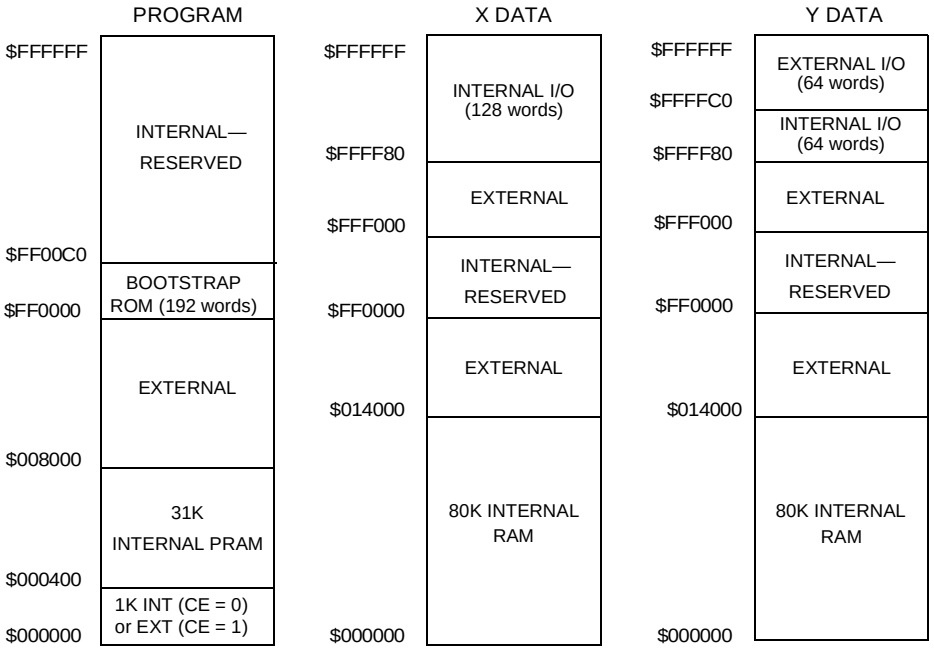


Figure 10. DSP56321 Memory Map—MSW= 000 and SC = 0
Memory Switch Mode Disabled, Sixteen-bit Compatibility Mode Disabled

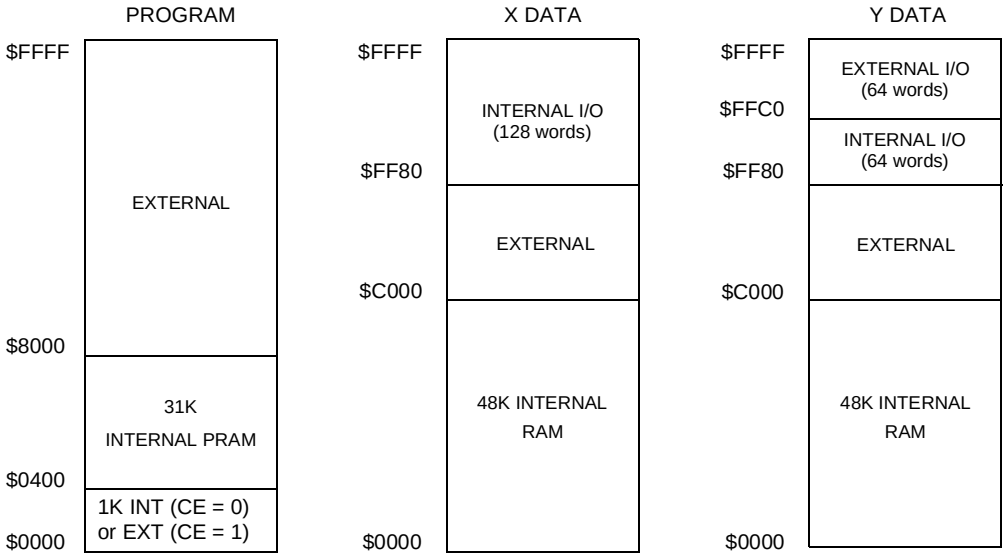


Figure 11. DSP56311 Memory Map—MS = 0 and SC = 1
Memory Switch Mode Disabled, Sixteen-bit Compatibility Mode Enabled

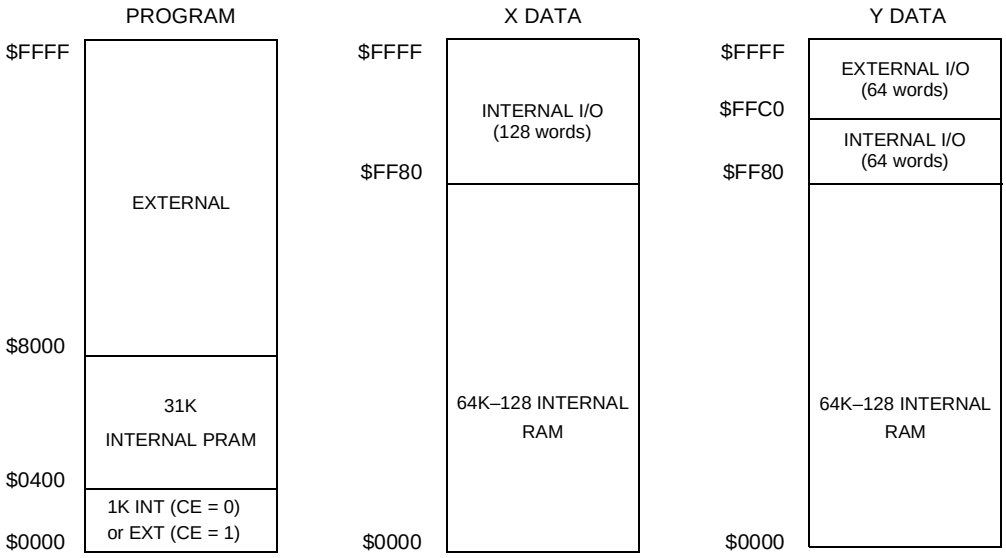


Figure 12. DSP56321 Memory Map—MSW = 000 and SC = 1
Memory Switch Mode Disabled, Sixteen-bit Compatibility Mode Enabled

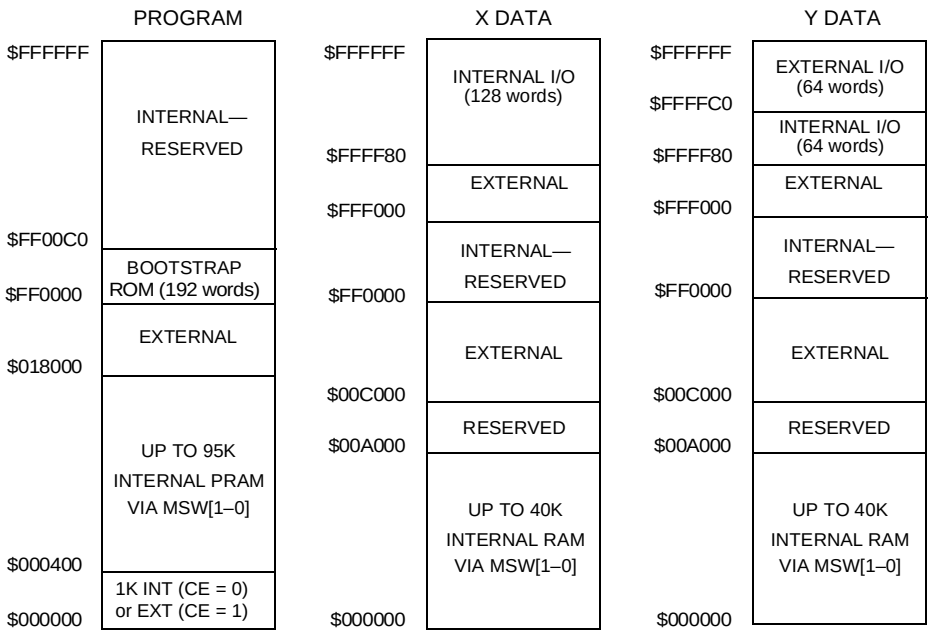


Figure 13. DSP56311 Memory Map—MS = 1 and SC = 0
Memory Switch Mode Enabled, Sixteen-bit Compatibility Mode Disabled

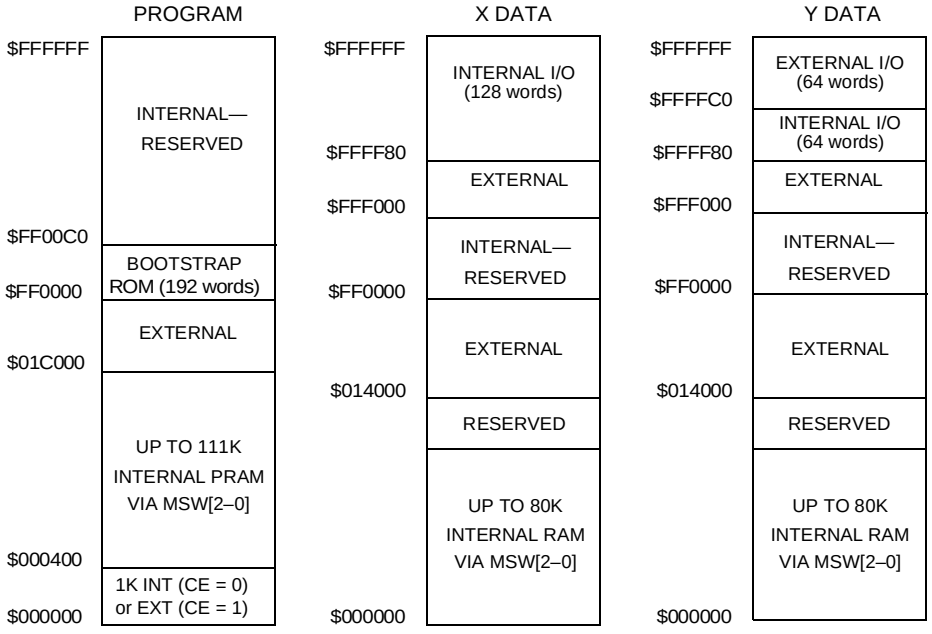


Figure 14. DSP56321 Memory Map—MSW ≠ 000 and SC = 0
Memory Switch Mode Enabled, Sixteen-bit Compatibility Mode Disabled

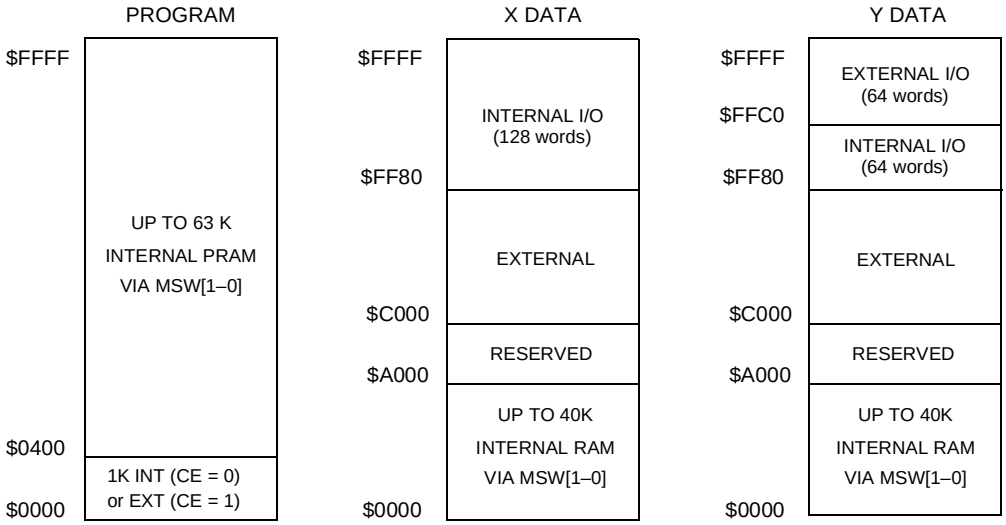


Figure 15. DSP56311 Memory Map—MS = 1 and SC = 1
Memory Switch Enabled, Sixteen-bit Compatibility Mode Enabled

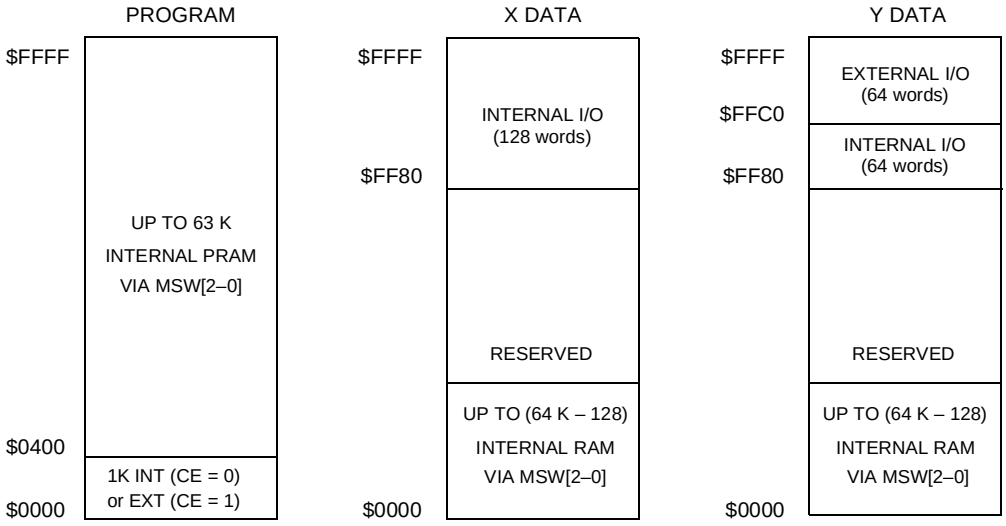


Figure 16. DSP56321 Memory Map—MSW ≠ 000 and SC = 1
Memory Switch Enabled, Sixteen-bit Compatibility Mode Enabled

10 EFCOP/Core Shared Memory

In the DSP56311, the EFCOP shares 20 K 24-bit words of memory with the DSP core: 10 K words in the X-data memory and 10 K words in the Y-data memory. In the DSP56321, the EFCOP shares 24 K words of memory with the DSP core: 12 K words in the X-data memory and 12 K words in the Y-data memory.

11 SRAM Access Wait States

The DSP56311 requires two wait states for operation at 150 MHz. The data sheet for the DSP56321 SRAM states that accesses require a minimum of three wait states for operation at 275 MHz. In addition, if the Bus Control Register is configured for more than one wait state, the DSP adds one or two trailing wait states. **Table 6** shows the number of trailing wait states associated with the number of wait states configured in the Bus Control Register for the DSP56311 or DSP56321.

Table 6. Additional Trailing Wait States for DSP56311 or DSP56321

Wait States in the Bus Control Register	Additional Trailing Wait States for DSP56311 or DSP56321
2–7 (DSP56311) or 3–7 (DSP56321)	1
≥ 8	2

12 DRAM Support

The DSP56311 supports DRAM access up to 100 MHz.

The DSP56321 does not support DRAM access. CLKOUT, $\overline{\text{BCLK}}$, BCLK, $\overline{\text{CAS}}$, and $\overline{\text{RAS}}$[0–3] signals are not supported.

13 Operating Mode Register

In the DSP56311, bits 22, 21, and 7 in the OMR are MSW[1–0] and MS. In the DSP56321, these bits are MSW[2–0]. This enables more switch modes in the DSP56321. The default mode represented by MS = 0 in the DSP56311 is represented by MSW[2–0] = 000 in the DSP56321. In addition, because $\overline{\text{BCLK}}$ and BCLK support is removed, OMR bit 15 is undefined in the DSP56321, since Address Trace Mode is not supported. **Figure 17** and **Figure 18** show the OMR layouts for the DSP56311 and DSP56321, respectively.

SCS								EOM								COM							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSW[1–0]		SEN	WRP	EOV	EUN	XYS	ATE	APD	ABE	BRT	TAS	BE	CDP1–0		MS	SD		EBD	MD	MC	MB	MA

- Reserved bit; read zero; write zero for future compatibility

Figure 17. DSP56311 Operating Mode Register (OMR) Format

SCS								EOM								COM							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSW[2–1]		SEN	WRP	EOV	EUN	XYS		APD	ABE	BRT	TAS	BE	CDP1–0		MSW0	SD		EBD	MD	MC	MB	MA

- Reserved bit; read zero; write zero for future compatibility

Figure 18. DSP56321 Operating Mode Register (OMR) Format

14 Clock/PLL

The DSP56311 uses an internal clock circuitry that includes the standard DSP56300 Phase Lock Loop (PLL) circuit and clock generator block. The DSP56321 uses a new internal clock circuit design that includes a DPLL and a new clock generator circuit. **Table 7** lists the differences between the clock/PLL and the clock/DPLL circuits.

Table 7. DSP56311 Clock/PLL and DSP56321 Clock/DPLL Differences

Characteristic	DSP56311 Clock and PLL	DSP56321 Clock and DPLL
Input frequency (EXTAL) with PLL disabled	0–150 MHz	0–275 MHz
Input frequency (EXTAL) with PLL enabled	7.324 KHz to 150 MHz	16 MHz to 275 MHz
Predivider Range (PDF)	1 to 16	1 to 16[1]
Multiplier Range (MF)	1 to 4096	5 to 15[2]
Core frequency maximum	150 MHz	275 MHz
Core frequency in bypass mode	EXTAL/2	EXTAL/2

Notes: **1.** The output frequency from the predivider must be between 16–32 MHz. The minimum input frequency with the PLL enabled must be 16 MHz with PDF = 1. The default PDF value at reset is 1.

2. MF = MFI + MFN/MFD, where MFI = 5 to 15; MFN = 0 to 127; MFD = 1 to 128; and MFN < MFD. Because the MF value is limited to a maximum of 15, if MFI = 15, MFN must equal 0. See **Section 15**for detailed information.

15 PLL/DPLL Control Registers

The DSP56311 uses one PLL Control Register (see **Figure 19** and **Table 8**) which is X-I/O-mapped at address $FFFFFD (24-bit mode) or $FFFD (16-bit mode). This read/write register directs the operation of the on-chip PLL.

23	22	21	20	19	18	17	16	15	14	13	12
PD3	PD2	PD1	PD0	COD	PEN	PSTP	XTLD	XTLR	DF2	DF1	DF0
11	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MF11	MF10	MF9	MF8	MF7	MF6	MF5	MF4	MF3	MF2	MF1	MF0

Figure 19. PLL Control Register (PCTL)

Table 8 defines the DSP56311 PCTL bits.

Table 8. DSP56311 PLL Control Register (PCTL) Bit Definitions

Bit Number	Bit Name	Reset Value	Description
23–20	PD[3–0]	0	**Predivider Factor Bits—**Define the predivision factor (PDF) to be applied to the PLL input frequency. The PD[3–0] bits are cleared during DSP56311 hardware reset, which corresponds to a PDF of one.
19	COD	0	**Clock Output Disable—**Controls the output buffer of the clock at the CLKOUT pin. When COD is set, the CLKOUT output is pulled high. When COD is cleared, the CLKOUT pin provides a 50 percent duty cycle clock.
18	PEN	PINIT	**PLL Enable—**Enables PLL operation. The reset value is taken from the PINIT input.
17	PSTP	0	**PLL Stop State—**Controls PLL and on-chip crystal oscillator behavior during the stop processing state.
16	XTLD	0	**XTAL Disable—**Controls the on-chip crystal oscillator XTAL output. The XTLD bit is cleared during DSP56311 hardware reset, so the XTAL output signal is active, permitting normal operation of the crystal oscillator.

Table 8. DSP56311 PLL Control Register (PCTL) Bit Definitions (Continued)

Bit Number	Bit Name	Reset Value	Description
15	XTLR	0	**Crystal Range—**Controls the on-chip crystal oscillator transconductance. The XTLR bit is set to a predetermined value during hardware reset. In the DSP56311, this value is zero.
14–12	DF[2–0]	0	**Division Factor—**Define the DF of the low-power divider. These bits specify the DF as a power of two in the range from 2^0 to 2^7.
11–0	MF[11–0]	0	**PLL Multiplication Factor—**Define the multiplication factor that is applied to the PLL input frequency. The MF bits are cleared during DSP56311 hardware reset and thus correspond to an MF of one.

The DSP56321 uses two control registers: DPLL Static Control Register (DSCR) at X:$FFFFD0 or X:FFD0 (16-bit mode) (see **Figure 20** and **Table 9**) and the DPLL Clock Control Register (PCTL) at X:$FFFFD1 or X:FFD1 (16-bit mode) (see **Figure 21** and **Table 10**).

23	22	21	20	19	18	17	16	15	14	13	12
BRMO	PLM	PDF3	PDF2	PDF1	PDF0	MFD6	MFD5	MFD4	MFD3	MFD2	MFD1
11	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
MFD0	MFN6	MFN5	MFN4	MFN3	MFN2	MFN1	MFN0	MFI3	MFI2	MFI1	MFI0

Figure 20. DPLL Static Control Register (DSCR)—X:$FFFFD0

Table 9. DPLL Static Control Register (DSCR) Bit Definitions

Bit Number	Bit Name	Reset Value	Description
23	BRMO	1	**Binary Rate Modulation Order**—The value of BRMO determines the output order used by the Binary Rate Modulator (BRM). If BRMO is cleared (0), the BRM uses a first order output. If BRMO is set (1), the BRM uses a second order output. If the DPLL Multiplication Factor Denominator (MFD) is < 8, then use a first order output (that is, BRMO = 0). If MFD $\geq$ 8, use a second order output (that is, BRMO = 1). If the DPLL Multiplication Factor Numerator (MFN) is 0, this bit is ignored. **Notes:** The DPLL does not operate correctly if this bit is not configured appropriately.
22	PLM	1	**Phase Lock Mode**—When this bit is cleared (0), the DPLL operates in Frequency Only Lock (FOL) mode. When this bit is set (1), the DPLL operates in Frequency and Phase Lock (FPL) mode. FPL mode can be used for both an integer and fractional multiplication factor, but phase skew reduction is accomplished only for the integer MF.

Table 9. DPLL Static Control Register (DSCR) Bit Definitions (Continued)

Bit Number	Bit Name	Reset Value	Description
21–18	PDF[3–0]	0	**Predivision Factor (PDF)**—Defines the DPLL Predivision Factor value. This value is in the range 1–16. **Notes:** The value of PDF bits written into DSCR must be the factor value minus 1.
			PDF[3–0] / **PDF Value** 0000 / 1 0001 / 2 0010 / 3 . . . / . . . 1111 / 16
17–11	MFD[6–0]	0	**Multiplication Factor Denominator (MFD)**—Defines the denominator of the fractional part of the Multiplication Factor (MF). The MFD can be any integer from 1 to 128. **Notes:** The value of MFD bits written into DSCR must be the denominator value minus 1. The MFD value must be higher than the MFN value.
			MFD[6–0] / **MFD Value** $00 / 1 $01 / 2 $02 / 3 . . . / $7E / 127 $7F / 128
10–4	MFN[6–0]	0	**Multiplication Factor Numerator (MFN)**—Defines the numerator of the fractional part of the MF. The MFN can be any integer from 0 to 127. **Notes:** The total MF is limited to a maximum of 15. Therefore, if the MFI is programmed as 15 (that is, MFI[3–0] = 1111), MFN must equal 0.
			MFN[6–0] / **MFN Value** $00 / 0 $01 / 1 $02 / 2 . . . / $7E / 126 $7F / 127

Table 9. DPLL Static Control Register (DSCR) Bit Definitions (Continued)

<table>
<tr><th>Bit Number</th><th>Bit Name</th><th>Reset Value</th><th>Description</th></tr>
<tr><td>3–0</td><td>MFI[3–0]</td><td>1000</td><td>Multiplication Factor Integer (MFI)—Defines the integer part of the MF. The MFI can be any integer from 5 to 15.

Notes: The total MF is limited to a maximum of 15. Therefore, if the MFI is programmed as 15 (that is, MFI[3–0] = 1111), MFN must equal 0.
<table>
<tr><th>MFI[3–0]</th><th>MFI Value</th></tr>
<tr><td>0000</td><td>5</td></tr>
<tr><td>0001</td><td>5</td></tr>
<tr><td>0010</td><td>5</td></tr>
<tr><td>0011</td><td>5</td></tr>
<tr><td>0100</td><td>5</td></tr>
<tr><td>0101</td><td>5</td></tr>
<tr><td>0110</td><td>6</td></tr>
<tr><td>0111</td><td>7</td></tr>
<tr><td>1000</td><td>8</td></tr>
<tr><td>.
.
.</td><td></td></tr>
<tr><td>1110</td><td>14</td></tr>
<tr><td>1111</td><td>15</td></tr>
</table>
</td></tr>
</table>

23	22	21	20	19	18	17	16	15	14	13	12
11	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
					DF2	DF1	DF0	PEN	XTLD	PSTP	

Reserved, write as zeros to maintain future compatibility.

Figure 21. DPLL Clock Control Register (PCTL)

Table 10. DPLL Clock Control Register (PCTL)

Bit Number	Bit Name	Reset Value	Description
23–7	reserved	0	These bits are reserved for future purposes.

Table 10. DPLL Clock Control Register (PCTL) (Continued)

<table>
<tr><th>Bit Number</th><th>Bit Name</th><th>Reset Value</th><th>Description</th></tr>
<tr><td>6–4</td><td>DF[2–0]</td><td>011</td><td>Division Factor (DF)—Defines the low-power divider specified as a power of two in the range from 2^0 to 2^7. Changing the value of the DF[2–0] bits does not cause a loss of lock condition.
<table>
<tr><th>DF[2–0]</th><th>DF value</th></tr>
<tr><td>000</td><td>2^0</td></tr>
<tr><td>001</td><td>2^1</td></tr>
<tr><td>010</td><td>2^2</td></tr>
<tr><td>011</td><td>2^3</td></tr>
<tr><td>100</td><td>2^4</td></tr>
<tr><td>101</td><td>2^5</td></tr>
<tr><td>110</td><td>2^6</td></tr>
<tr><td>111</td><td>2^7</td></tr>
</table></td></tr>
<tr><td>3</td><td>PEN</td><td>PINIT</td><td>DPLL Enable—When PEN is set, the DPLL is enabled; when the DPLL locks, the internal clocks are derived from the DPLL output. When PEN is cleared, the internal clocks are derived directly from the EXTAL signal. Disabling the DPLL minimizes power consumption. Software can set or clear the PEN bit at any time during the device operation. During hardware reset, this bit is set or cleared based on the value of the DPLL PINIT input.</td></tr>
<tr><td>2</td><td>XTLD</td><td>0</td><td>XTAL Disable—Controls the XTAL output from the crystal oscillator on-chip driver. When XTLD is cleared, the XTAL output pin is active, permitting normal operation of the crystal oscillator. When XTLD is set, the XTAL output pin is pulled high, disabling the on-chip oscillator driver. If the on-chip crystal oscillator driver is not used (that is, EXTAL is driven from an external clock source), set XTLD (disabling XTAL) to minimize RFI noise and power dissipation.</td></tr>
<tr><td>1</td><td>PSTP</td><td>0</td><td>DPLL Stop State Control—Determines DPLL and on-chip crystal oscillator behavior during the Stop processing state. When PSTP is set, the DPLL and the on-chip crystal oscillator remain operating when the chip is in the Stop state. When PSTP is cleared and the device enters the Stop state, the DPLL and the on-chip crystal oscillator are disabled to reduce power consumption; however, this results in longer recovery time upon exit from the Stop state. To enable rapid recovery when exiting the Stop state (but at the cost of higher power consumption during the Stop state), PSTP should be set.

Notes: PSTP and PEN are related. When PSTP is set and PEN is cleared, the on-chip crystal oscillator remains operating in the Stop state, but the DPLL is disabled. This power saving feature enables rapid recovery from the Stop state when you operate the device with an on-chip oscillator and with the DPLL disabled.
<table>
<tr><th rowspan="2">PSTP</th><th rowspan="2">PEN</th><th colspan="2">Operation during Stop State</th><th rowspan="2">Recovery Time from Stop State</th><th rowspan="2">Power Consumption during Stop State</th></tr>
<tr><th>DPLL</th><th>Oscillator (XTLD=0)</th></tr>
<tr><td>0</td><td>X</td><td>Disabled</td><td>Disabled</td><td>Long</td><td>Minimal</td></tr>
<tr><td>1</td><td>0</td><td>Disabled</td><td>Enabled</td><td>Short</td><td>Low</td></tr>
<tr><td>1</td><td>1</td><td>Enabled</td><td>Enabled</td><td>Short</td><td>High</td></tr>
</table></td></tr>
</table>

Table 10. DPLL Clock Control Register (PCTL) (Continued)

Bit Number	Bit Name	Reset Value	Description
0	reserved	0	This bit is reserved. **Notes:** Although this bit is cleared after reset, it enables the output of a reserved signal that Freescale uses for development purposes. To prevent possible noise generation, Freescale recommends writing a 1 to this bit after reset to disable the reserved signal output.

16 Peripheral Timing

The timing for the on-chip peripherals is based primarily on the operating frequency used by the specified device (DSP56311 or DSP56321). An example of the effect due to the frequency difference is the ratio of the peripheral clock frequency to the core clock frequency. In addition, internal signal delay values are inherently different for the HiP4 process (DSP56311) versus the HiP7 process (DSP56321), resulting in different constant values used in timing expressions. Refer to Section 2 in the DSP56311 Technical Data sheet or the DSP56321 Technical Data sheet for detailed timing information.

17 Package

The DSP56311 and DSP56321 are signal pin-compatible, but the DSP56311 uses a 15 mm × 15 mm 196-pin Molded Array Process-Ball Grid Array (MAP-BGA) package, whereas the DSP56321 uses Freescale's 15 mm × 15 mm 196-pin Flip Chip-Ball Grid Array (FC-PBGA) package. **Table 11** summarizes the differences between these two packages.

Table 11. Differences Between the 196-Pin MAP-BGA and FC-PBGA Packages

Characteristic	MAP-BGA (DSP56311)	FC-PBGA (DSP56321)
X/Y Dimensions	15 × 15 mm	15 × 15 mm
Ball Pitch	1.0 mm	1.0 mm
Pinout	196-pin	196-pin
Interconnection Method	Wirebond—MAP-BGA is attached to the substrate face-up, connected using gold wires.	C4 Bump—FC-PBGA uses an evaporated 97% Lead/3% Tin (97Pb3Sn) bump joined to the substrate face-down.
Package Height	1.60 mm maximum	2.43 mm maximum
Θ_{JA} (°C/W)	49 (no airflow)	50 (no airflow)—simulated. Actual data TBD.
Θ_{Jc} (°C/W)	10	10—simulated. Actual data TBD.
Moisture Sensitivity	Moisture Sensitivity Level 3 (MSL3) capable	MSL5 capable. Actual performance TBD.
Coplanarity Specification	0.10 mm	0.15 mm
Package Sealing Against Moisture	Overmolded with a dense silica epoxy	Epoxy underfill seals the cavity between die and substrate and increases the reliability of the bump interconnection
Singulation	Saw cutting	Flip chip substrates are delivered singulated from the substrate supplier
Package Identifier	VF	FC
Solder Balls	0.5 mm 62Sn36Pb2Ag	0.5 mm 62Sn36Pb2Ag
Package Solder Pad	Soldermask Defined (SMD)	Soldermask Defined (SMD)

For dimensional reference, **Figure 22** shows the MAP-BGA package drawing, and **Figure 23** shows the FC-PBGA package drawing.

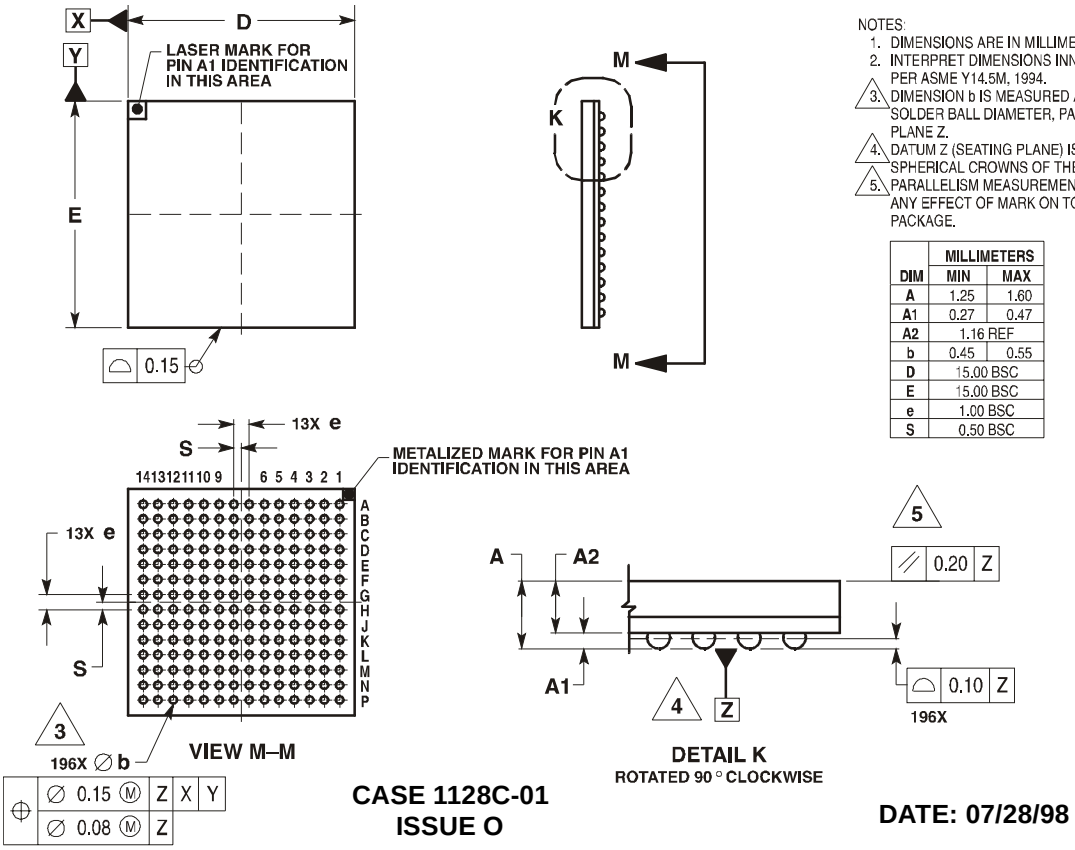
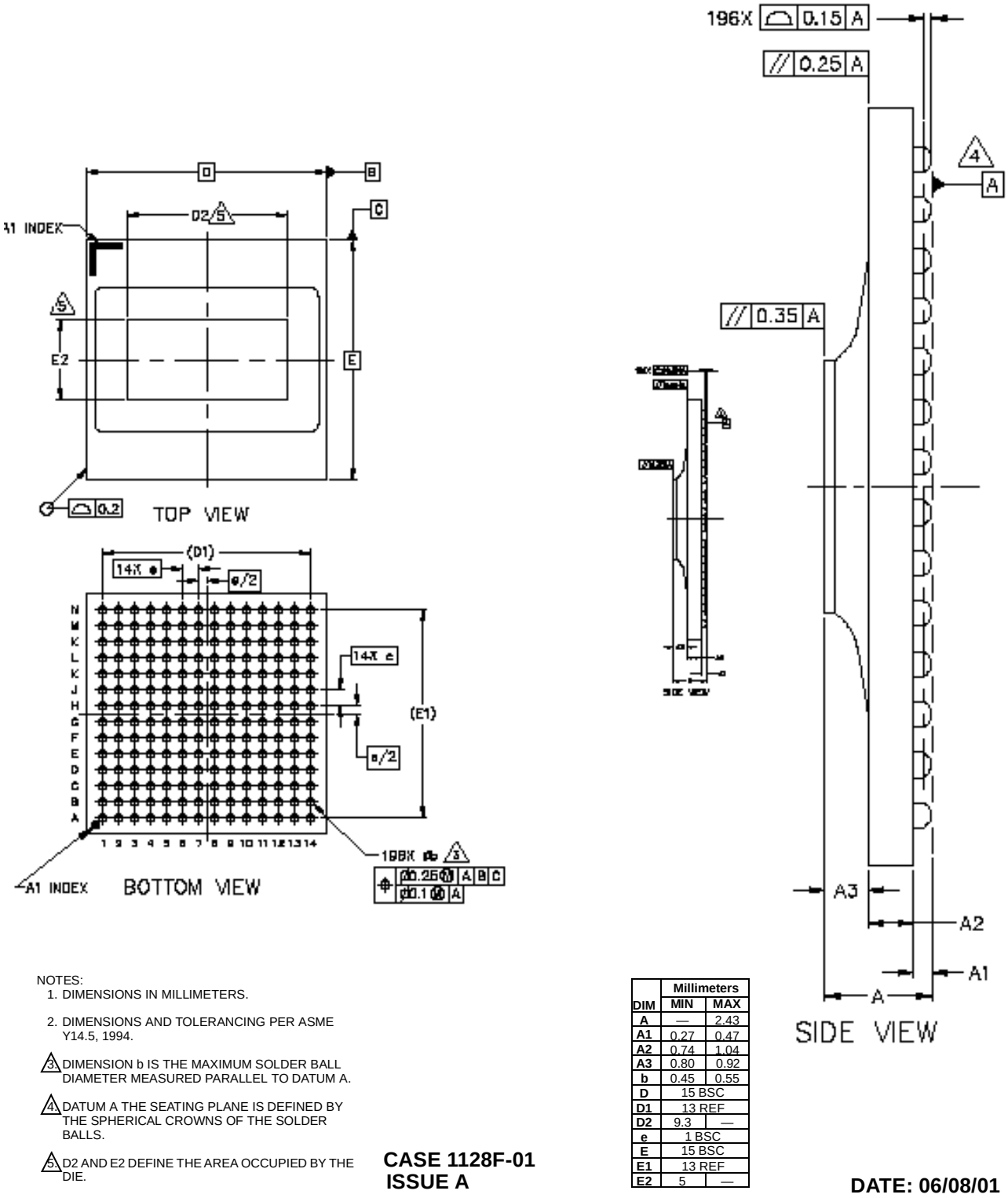


Figure 22. Mechanical Information for 196-pin MAP-BGA Package



NOTES:
1. DIMENSIONS IN MILLIMETERS.
2. DIMENSIONS AND TOLERANCING PER ASME Y14.5, 1994.
3. DIMENSION b IS THE MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A THE SEATING PLANE IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. D2 AND E2 DEFINE THE AREA OCCUPIED BY THE DIE.

DIM	Millimeters MIN	MAX
A	—	2.43
A1	0.27	0.47
A2	0.74	1.04
A3	0.80	0.92
b	0.45	0.55
D	15 BSC	
D1	13 REF	
D2	9.3	—
e	1 BSC	
E	15 BSC	
E1	13 REF	
E2	5	—

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DATE: 06/08/01

Figure 23. Mechanical Information for 196-pin FC-PBGA Package

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