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Engineering Bulletin

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Using Predividers on the MPC5500 FMPLL

Including the MPC553x, MPC555x, and MPC556x Devices

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1 Introduction

The MPC5500 devices based on the e200z3 and e200z6 Power Architecture® cores use a low frequency, or relatively low frequency, crystal. This crystal is used as a reference to the on-chip frequency modulated phase-lock loop (FMPLL) that generates the system clock. Crystals in the range of 8 MHz to 20 MHz — or greater than 20 MHz, up to 40 MHz — can be used, depending on the configuration of the FMPLL (see the PLLCFG2 pin on devices that support the 40 MHz crystal option). However, the reference frequency to the FMPLL can be as low as 4 MHz, and must be less than one-half of the maximum operating frequency of the device.

The crystal circuitry drives a predivider that allows the crystal reference to be divided by a value from one to five. A limitation was found in the design of the prescaler to the FMPLL (from the crystal circuitry) that requires proper divider initialization if using a predivider greater than one (using a predivider of two to five). This

Contents

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engineering bulletin describes the proper method of initializing the FMPLL to avoid anomalous operation when using predividers greater than one.

NOTE

This engineering bulletin does not apply to the MPC5510 family or to any of the MPC56xx devices.

Table 1. MPC5500 Family FMPLL Support

Device	Maximum PLL Frequency	Is a 40 MHz Crystal Supported?
MPC5533	82 MHz	No
MPC5534	82 MHz	No
MPC5553	132 MHz	No
MPC5554	132 MHz	No
MPC5561	135 MHz	Yes
MPC5565	135 MHz	No[1]
MPC5566	147 MHz	No
MPC5567	135 MHz	Yes

1 The MPC5565 has a PLLCFG2 pin that would allow selection between the 8 to 20 MHz crystal and the >20 to 40 MHz crystal. However, the device only allows PLLCFG2 to be set low for 8 to 20 MHz crystal operation. [meaning that only one option is actually available?]

2 Clock and FMPLL Overview

The clock and FMPLL section of the device is made up of several blocks. The key blocks are the oscillator, the predivider, the FMPLL itself, and the FMPLL reduced-frequency divider. All of these blocks control the final system frequency at which the device operates. They are all controlled in the FMPLL Synthesizer Control Register (FMPLL_SYNCR) by the predivider control bits (PREDIV), the multiplication factor divider (MFD), and the reduced frequency divider (RFD). The formula for defining the system frequency is shown in Figure 1.

$$F_{sys} = F_{ref\_crystal} \times \frac{MFD + 4}{(PREDIV + 1) \times 2^{RFD}}$$

Figure 1. System Frequency Formula

Figure 2 shows a block diagram of the clock generation section of the MPC5500 devices. This block diagram is slightly modified from the block diagram included in the device's reference manuals. The PREDIV and the RFD are shown outside of the FMPLL (the reference manuals group these all together inside the FMPLL block). This is a more accurate representation, considering the specifications of the device (FMPLL input frequency [after predivider] and the current-controlled oscillator output).

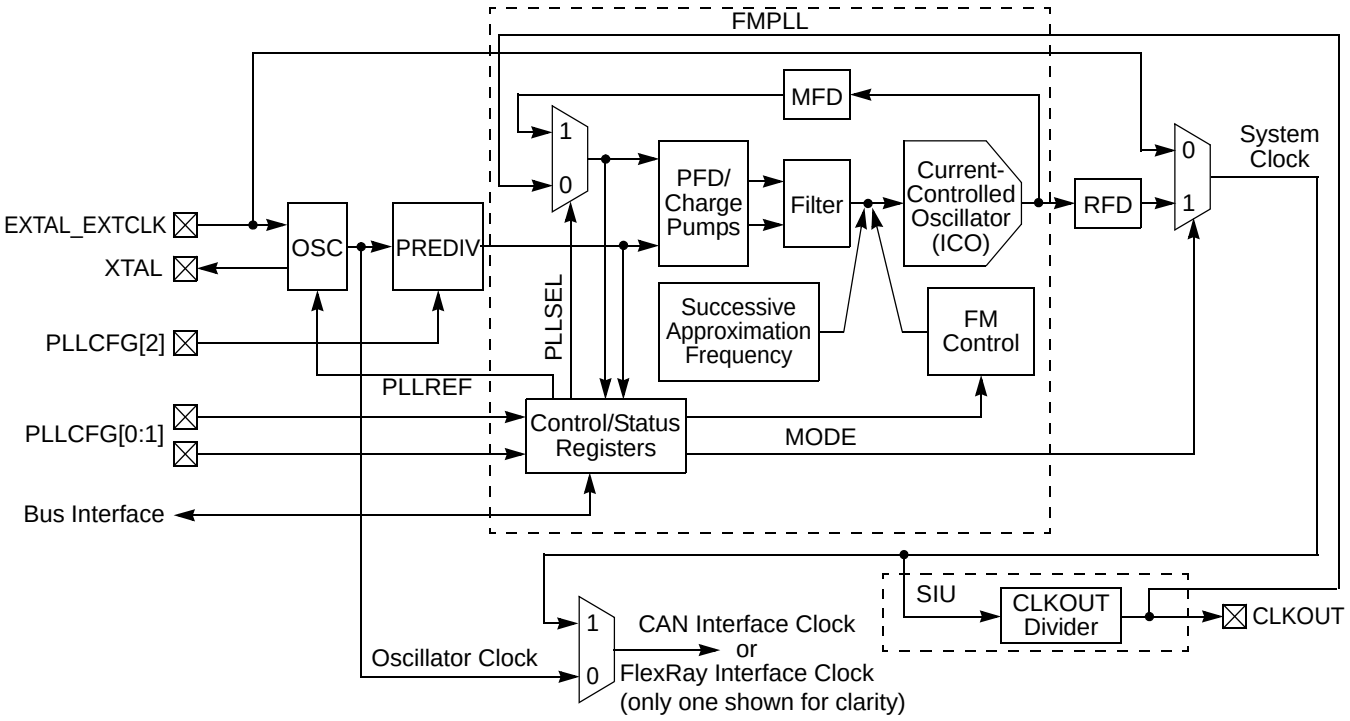

Figure 2. FMPLL Block Diagram

Regardless of the predivider, the FMPLL has several restrictions. These include the range of the reference frequency to the FMPLL, as well as the fact that the maximum frequency of the FMPLL output, prior to the postdivider (RFD), must be within the operating frequency of the device. See the oscillator and FMPLL electrical specifications[1] section of the device's data sheet to find the minimum and maximum frequencies that each device supports. Keep in mind that the minimum frequency into the FMPLL from the predivider is 4.0 MHz.

Making changes to either the PREDIV or the MFD will cause the FMPLL to relock. Changes to the RFD do not cause the FMPLL to relock. Therefore, for quick changes in frequency, the RFD can be changed to reduce the system frequency. This will reduce power (for a lower power option), but will also allow software to quickly restore the previous system frequency.

2.1 Predivider (PREDIV)

The predivider to the FMPLL allows the input reference clock to be divided by a value from one to five, to add additional system frequency resolution. For example, a system frequency of 132 MHz cannot be derived with a straight multiplier from an 8 MHz crystal (or clock reference). Using a predivider of two gives the FMPLL a reference clock of 4 MHz that can be multiplied to achieve a system frequency of 132 MHz.

1. In particular, see the FMPLL reference frequency range specification, system frequency specifications (plus the *Orderable Part Numbers* table), and the predivider output frequency in the datasheet.

2.2 Multiplication Factor Divider (MFD)

The multiplication factor divider controls the output frequency of the FMPLL by taking the FMPLL output, dividing it by the multiplication factor, and comparing the resulting frequency to the input reference frequency. The FMPLL then adjusts the output frequency up or down to match the input frequency after the MFD circuit. The minimum multiplier (with an MFD setting of 0b0_0000) is four. The MFD allows for a maximum multiplier of $(2^5 – 1) + 4$, or 35.

2.3 Reduced Frequency Divider (RFD)

The reduced frequency divider (RFD) is a postdivider that is used to generate lower frequencies for the system clock than the actual FMPLL output clock can provide. The RFD is restricted to dividers that are multiples of two — see Table 2.

Table 2. Reduced Frequency Divider Settings

RFD	Divider
0b000	Divide by 1
0b001	Divide by 2
0b010	Divide by 4
0b011	Divide by 8
0b100	Divide by 16
0b101	Divide by 32
0b110	Divide by 64
0b111	Divide by 128

2.4 Recommended MCU Initialization of the FMPLL

It is recommended that the following sequence be used to initialize the FMPLL and cache (if available) on the MPC55xx devices. Cache initialization is included because the cache draws a significant amount of current. It is best to enable the cache while the system is at a low system frequency, because enabling the cache when running at the final system frequency will cause a larger instantaneous jump in the operational current required from the power supply than when the enabling is done at a lower frequency.

1. While the device is running at the default system frequency after reset, enable the cache. However, the region of memory where the FMPLL frequency-setting code resides (usually the internal flash) must be set to noncacheable in the MMU.[1]
2. Set the FMPLL frequency to one-half of the desired system frequency (with RFD = 0b001). This may take several steps to maintain the minimum and maximum frequencies for the FMPLL input frequency and FMPLL output frequency. Anytime either the PREDIV or the MFD values are changed, software must wait for the FMPLL to lock prior to continuing to the next step.
3. The MMU region containing the initialization code can then be made cacheable.
4. Set the RFD to 0b000 to reach the final system frequency.

NOTE

The MPC55xx family does not disable the clock to peripherals when the FMPLL is locking or relocking. For this reason, it is recommended that the FMPLL be locked at one-half of the final system frequency using the reduced frequency divider to avoid operating above the maximum rating of the device. As the final step of the clock frequency change, the RFD can be set to divide by one.

For customers familiar with the MPC5xx family, this operation is different. On the MPC5xx family, the system clock is disabled while the FMPLL is locking.

2.5 Pre-Divider Issues

The predivider between the crystal and the FMPLL generates a nearly 50% duty-cycle signal to the FMPLL input, regardless of the divider ratio (even or odd). If the predivider to the FMPLL is set to a divider value greater than one, the PLL may fail to lock if the end system frequency is greater than one-half crystal frequency during the PLL lock sequence at the time of the write to the SYNCR register. If a failing condition occurs, when an odd predivider (three or five) is programmed, the FMPLL will continuously operate in the digital successive approximation stage of the FMPLL lock operation. The clock out signal (CLKOUT) will step through five different frequencies. In the case of even predividers (two or four), the FMPLL will essentially bypass the digital SAR stage of the lock operation, setting the current-controlled oscillator to a higher frequency than the analog portion of the FMPLL can tolerate, and it will fail to lock.

1. Cached code that only reads the FMPLL synthesizer status register (FMPLL_SYNSR) can cause an undesirable increase in the system current by executing a very tight loop at the maximum core clock instruction rate.

NOTE

Initiating the FMPLL lock with a maximum system frequency of one-half of the crystal frequency is a requirement only if the predivider is set to divide by two or more.

3 Proper Predivider Programming

Any time a predivider of two or more is required, the final system frequency must be less than one-half of the crystal frequency at the time either the predivider or the multiplication factors are being changed.

In other words, the system frequency must be less than one-half of the crystal frequency when the write is performed to the FMPLL_SYNCR and either of these two conditions is true:

- The PREDIV is set to a value of 0b001 or more (divide by two or greater) and there is a change to the MFD.
- The PREDIV alone is being changed to a value greater than zero.

In most cases, a predivider greater than one (divide by two or more) is only needed when a 4 MHz reference is required for the input to the PLL (8, 12, 16, or 20 MHz crystals) or when using a 40 MHz crystal with devices that support FlexRay. A 4 MHz reference to the PLL is generally required to obtain a 132 MHz system frequency (8, 16, and 20 MHz crystal references cannot be multiplied directly to obtain a 132 MHz system clock). A 40 MHz crystal can be used to obtain an 8 MHz reference to the FMPLL with an 8 MHz system frequency resolution and to provide the 40 MHz reference for FlexRay.

3.1 132 MHz System Frequency with an 8 MHz Crystal (Divide-by-Two Predivider)

Dividing the 8 MHz crystal by two gives a 4 MHz clock frequency that can then be multiplied up to a 132 MHz system frequency. To avoid any issues, Table 3 shows a sequence of steps that can be taken to meet the maximum frequency specifications for the FMPLL and maintain the system frequency.

Table 3. Recommended FMPLL Settings for 132 MHz System Frequency and 8 MHz Crystal

Step	Predivider		Multiplication Factor		Reduced Frequency Divider		FMPLL Output Frequency [1]	System Frequency
	Divide Value	PREDIV	Multiplication Value	MFD	Postdivider Value	RFD		
0	÷1	0b000	×6	0b0_0010	÷4	0b010	48 MHz	12 MHz
1	System Initialization — Enable cache, but keep internal flash not cacheable							
2	÷1	0b000	×6	0b0_0010	÷16	0b100	48 MHz	3 MHz[2]
3	÷2	0b001	×33[3]	0b1_1101	÷16	0b100	132 MHz[4]	8.25 MHz
4	Wait for FMPLL to lock							
5	System Initialization — Enable cache of internal flash							
6	÷2	0b001	×33[3]	0b1_1101	÷8[5]	0b011	132 MHz[4]	16.5 MHz

Table 3. Recommended FMPLL Settings for 132 MHz System Frequency and 8 MHz Crystal

Step	Predivider		Multiplication Factor		Reduced Frequency Divider		FMPLL Output Frequency [1]	System Frequency
	Divide Value	PREDIV	Multiplication Value	MFD	Postdivider Value	RFD		
7	÷2	0b001	×33[3]	0b1_1101	÷4[5]	0b010	132 MHz[4]	33 MHz
8	÷2	0b001	×33[3]	0b1_1101	÷2[5]	0b001	132 MHz[4]	66 MHz
9	÷2	0b001	×33[3]	0b1_1101	÷1[5]	0b000	132 MHz[4]	132 MHz

1 FMPLL output frequency (prior to the RFD divider) must be between 48 MHz and the maximum FMPLL frequency (as specified in the device datasheet).

2 The system clock frequency must be less than one-half of the crystal frequency when changing the predivider or the MFD.

3 Change this to × 32 (0b1_1100 or 0x1C) for 128 MHz system frequency.

4 Or 128 MHz if a multiplication factor of 32 is used.

5 Intermediate steps may not be required if the power supply can manage the change in current load from changing the clock frequency.

3.2 132 MHz System Frequency with a 16 MHz Crystal (Divide-by-Four Predivider)

Dividing the 16 MHz crystal by 4 gives a 4 MHz clock frequency that can then be multiplied up to a 132 MHz system frequency. To avoid any issues, Table 4 shows a sequence of steps that can be taken to meet the maximum frequency specifications for the FMPLL and maintain the system frequency.

Table 4. Recommended FMPLL Settings for 132 MHz System Frequency with a 16 MHz Crystal

Step	Predivider		Multiplication Factor		Reduced Frequency Divider		FMPLL Output Frequency[1]	System Frequency
	Divide Value	PREDIV	Multiplication Value	MFD	Postdivider Value	RFD		
0	÷1	0b000	×6	0b0_0010	÷4	0b010	96 MHz	24 MHz
1	System Initialization — Enable cache, but keep internal flash not cacheable							
2	÷1	0b000	×6	0b0_0010	÷16	0b101	96 MHz	6 MHz[2]
3	÷4	0b011	×33[3]	0b1_1101	÷16	0b101	132 MHz[4]	8.25 MHz
4	Wait for FMPLL to lock							
5	System Initialization — Enable cache of internal flash							
6	÷4	0b011	×33[3]	0b1_1101	÷8[5]	0b011	132 MHz[4]	16.5 MHz
7	÷4	0b011	×33[3]	0b1_1101	÷4[5]	0b010	132 MHz[4]	33 MHz
8	÷4	0b011	×33[3]	0b1_1101	÷2[5]	0b001	132 MHz[4]	66 MHz
9	÷4	0b011	×33[3]	0b1_1101	÷1[5]	0b000	132 MHz[4]	132 MHz

1 FMPLL output frequency (prior to the RFD divider) must be between 48 MHz and the maximum FMPLL frequency (as specified in the device datasheet).

2 The system clock frequency must be less than one-half of the crystal frequency when changing the predivider or the MFD.

3 Change this to × 32 (0b1_1100 or 0x1C) for 128 MHz system frequency.

4 Or 128 MHz if a multiplication factor of 32 is used.

5 Intermediate steps may not be required if the power supply can manage the change in current load from changing the clock frequency.

3.3 128 MHz System Frequency with a 20 MHz Crystal (Divide-by-Five Predivider)

Dividing the 20 MHz crystal by five gives a 4 MHz clock frequency that can then be multiplied up to either a 128 MHz system frequency or a 132 MHz system frequency. Table 5 shows a sequence of steps that can be taken that meets the maximum frequency specifications for the FMPLL and maintains the system frequency, to avoid any issues with a predivider of five.

Table 5. Recommended FMPLL Settings for 132 MHz System Frequency and 20 MHz Crystal (Divide-by-Five Predivider)

Step	Predivider		Multiplication Factor		Reduced Frequency Divider		FMPLL Output Frequency[1]	System Frequency
	Divide Value	PREDIV	Multiplication Value	MFD	Postdivider Value	RFD		
0	÷1	0b000	×6	0b0_0010	÷4	0b010	120 MHz	30 MHz
1	System Initialization — Enable cache, but keep internal flash not cacheable							
2	÷1	0b000	×6	0b0_0010	÷16	0b100	120 MHz	7.5 MHz[2]
3	÷5	0b100	×32[3]	0b1_1100	÷16	0b100	128 MHz[5]	8 MHz
4	Wait for FMPLL to lock							
5	System Initialization — Enable cache of internal flash							
6	÷5	0b100	×32[3]	0b1_1100	÷8[4]	0b011	128 MHz[5]	16 MHz
7	÷5	0b100	×32[3]	0b1_1100	÷4[4]	0b010	128 MHz[5]	32 MHz
8	÷5	0b100	×32[3]	0b1_1100	÷2[4]	0b001	128 MHz[5]	64 MHz
9	÷5	0b100	×32[3]	0b1_1100	÷1[4]	0b000	128 MHz[5]	128 MHz

1 FMPLL output frequency (prior to the RFD divider) must be between 48 MHz and the maximum FMPLL frequency (as specified in the device datasheet).

2 The system clock frequency must be less than one-half of the crystal frequency when changing to divide-by-three or divide-by-five on the predivider.

3 Change this to × 33 (0b1_1101 or 0x1C) for 132 MHz system frequency.

4 Intermediate steps may not be required if the power supply can manage the change in current load from changing the clock frequency.

5 Or 132 MHz if a multiplication factor of 33 is used.

3.4 128 MHz System Frequency with a 40 MHz Crystal (Divide-by-Five Predivider)

Dividing the 40 MHz crystal by five gives an 8 MHz clock frequency that can then be multiplied to generate a 128 MHz system frequency. Table 6 shows a sequence of steps that can be taken that meets the maximum frequency specifications for the FMPLL and maintains the system frequency. Doing so will avoid problems when using a predivider of five.

Table 6. Recommended FMPLL settings for 128 MHz System Frequency and 40 MHz Crystal (Divide-by-Five Predivider)

Step	Predivider		Multiplication Factor		Reduced Frequency Divider		FMPLL Output Frequency[1]	System Frequency
	Divide Value	PREDIV	Multiplication Value	MFD	Postdivider Value	RFD		
0	÷2	0b001	×6	0b0_0010	÷4	0b010	120 MHz	30 MHz
1	System Initialization — Enable cache, but keep internal flash not cacheable							
2	÷2	0b001	×6	0b0_0010	÷8	0b011	120 MHz	15 MHz[2]
3	÷5	0b100	×16	0b0_1100	÷8	0b011	128 MHz	16 MHz
4	Wait for FMPLL to lock							
5	System Initialization — Enable cache of internal flash							
6	÷5	0b100	×16	0b0_1100	÷4[3]	0b010	128 MHz	32 MHz
7	÷5	0b100	×16	0b0_1100	÷2[3]	0b001	128 MHz	64 MHz
8	÷5	0b100	×16	0b0_1100	÷1	0b000	128 MHz	128 MHz

1 FMPLL output frequency (prior to the RFD divider) must be between 48 MHz and the maximum FMPLL frequency (as specified in the device datasheet).

2 The system clock frequency must be less than one-half of the crystal frequency when changing to divide-by-three or divide-by-five on the predivider.

3 Intermediate steps may not be required if the power supply can manage the change in current load from changing the clock frequency.

3.5 132 MHz System Frequency with a 12 MHz Crystal (Divide-by-Three Predivider)

Dividing the 12 MHz crystal by three gives a 4 MHz clock frequency that can then be multiplied to generate either a 128 MHz system frequency or a 132 MHz system frequency. Table 7 shows a sequence of steps that can be taken that meets the maximum frequency specifications for the FMPLL and maintains the system frequency. Doing so will avoid problems with a predivider of three.

Table 7. 12 MHz FMPLL Settings with Divide-by-Three

Step	Predivider		Multiplication Factor		Reduced Frequency Divider		FMPLL Output Frequency[1]	System Frequency
	Divide Value	PREDIV	Multiplication Value	MFD	Postdivider Value	RFD		
0	÷1	0b000	×6	0b0_0010	÷4	0b010	72 MHz	18 MHz
1	System Initialization — Enable cache, but keep internal flash not cacheable							
2	÷1	0b000	×6	0b0_0010	÷16	0b100	72 MHz	4.5 MHz[2]
3	÷3	0b100	×33	0b1_1101	÷16	0b100	132 MHz	8.25 MHz
4	Wait for FMPLL to lock							
5	System Initialization — Enable cache of internal flash							
6	÷5	0b100	×33	0b1_1101	÷8[3]	0b011	132 MHz	16.5 MHz
7	÷3	0b100	×33	0b1_1101	÷4[3]	0b010	132 MHz	33 MHz
8	÷3	0b100	×33	0b1_1101	÷2[3]	0b001	132 MHz	66 MHz
9	÷3	0b100	×33	0b1_1101	÷1[3]	0b000	132 MHz	132 MHz

1 FMPLL output frequency (prior to the RFD divider) must be between 48 MHz and the maximum FMPLL frequency (as specified in the device datasheet).

2 The system clock frequency must be less than one-half of the crystal frequency when changing to divide-by-three or divide-by-five on the predivider.

3 Intermediate steps may not be required if the power supply can manage the change in current load from changing the clock frequency.

4 Summary

For devices that require the use of a predivider greater than one to the FMPLL to obtain the final system frequency, care must be taken to insure that the FMPLL is initialized in the proper steps so as to avoid erroneous situations.

Appendix A Errata Wording

The current wording of the errata for the MPC5500 family devices is shown below. (The number is IPG8014, but this number could change in the future. Always refer to the latest revision of the device errata sheet available on the Freescale website, at www.freescale.com/MPC55xx.)

- Errata Title

  FMPLL: Non-zero pre-divider values can cause PLL lock failure

- Errata Description

  When configuring the MPC55xx Frequency Modulated Phase Lock Loop (FMPLL) in crystal or external reference clock mode, the system clock frequency (SYSCLK) is determined by the values programmed into the Pre-Divider (PREDIV), Multiplication Factor Divider (MFD), and Reduced Frequency Divider (RFD) fields in the FMPLL Synthesizer Control Register (FMPLL_SYNCR). If the pre-divider is set to divide by 2, 3, 4, or 5 (FMPLL_SYNCR[PREDIV] = 1, 2, 3, or 4), a condition may occur in which the FMPLL will fail to lock. Odd predividers may result in the PLL stuck in a lock routine where it can not escape. Even predividers may result in the PLL VCO frequency not being able to reach target frequencies below 110MHz. To clear this condition when it occurs, the part must be powered down.

- Errata Work Around

  If a pre-divider of 2, 3, 4, or 5 must be used in order to achieve the desired system clock frequency, any write that causes a relock of the FMPLL (changing either the PREDIV or MFD) with a FMPLL_SYNCR[PREDIV] = 1, 2, 3, or 4 must occur with the current system frequency set to one-half of the crystal frequency or less through setting of the PLL RFD prior to writing the MFD or PREDIV.

  NOTE: When programming the FMPLL, care must also be taken not to violate the maximum system clock frequency of the device, or the maximum and minimum frequency specifications of the FMPLL.

Appendix B FMPLL Settings When Using a Predivider of One—Examples

Although there is no special requirement for the FMPLL locking with the system frequency of less than one-half of the crystal frequency when a predivider is set to one (PREDIV=0b000), this appendix shows some examples of FMPLL settings using a divide-by-one predivider.

B.1 80 MHz System Frequency with 8 MHz Crystal and Divide-by-One Predivider

An 8 MHz crystal can be multiplied up directly to an 80 MHz system frequency. To avoid any issues, Table 8 shows a sequence of steps that can be taken to meet the maximum frequency specifications for the FMPLL and maintain the system frequency.

Table 8. Recommended FMPLL Settings for 80 MHz System Frequency and 8 MHz Crystal

Step	Predivider		Multiplication Factor		Reduced Frequency Divider		FMPLL Output Frequency[1]	System Frequency
	Divide Value	PREDIV	Multiplication Value	MFD	Postdivider Value	RFD		
0	÷1	0b000	×6	0b0_0010	÷4	0b010	48 MHz	12 MHz
1	System Initialization — Enable cache, but keep internal flash not cacheable							
2	÷1	0b000	×10	0b0_0110	÷2	0b001	80 MHz	40 MHz
3	Wait for FMPLL to lock							
4	System Initialization — Enable cache of internal flash							
5	÷1	0b000	×10	0b0_0110	÷1	0b000	80 MHz	80 MHz

1 FMPLL output frequency (prior to the RFD divider) must be between 48 MHz and the maximum FMPLL frequency (as specified in the device datasheet).

B.2 80 MHz System Frequency with 20 MHz Crystal and Divide-by-One Predivider

A 20 MHz crystal can then be multiplied up directly to an 80 MHz system frequency. To avoid any issues, Table 9 shows a sequence of steps that can be taken to meet the maximum frequency specifications for the FMPLL and maintain the system frequency.

Table 9. Recommended FMPLL Settings for 80 MHz System Frequency and 20 MHz Crystal

Step	Predivider		Multiplication Factor		Reduced Frequency Divider		FMPLL Output Frequency[1]	System Frequency
	Divide Value	PREDIV	Multiplication Value	MFD	Postdivider Value	RFD		
0	÷1	0b000	×6	0b0_0010	÷4	0b010	120 MHz	30 MHz
1	System Initialization — Enable cache, but keep internal flash not cacheable							
2	÷1	0b000	×4	0b0_0000	÷2	0b100	80 MHz	40 MHz
3	Wait for FMPLL to lock							
4	System Initialization — Enable cache of internal flash							
5	÷1	0b000	×4	0b0_0000	÷1	0b000	80 MHz	80 MHz

1 FMPLL output frequency (prior to the RFD divider) must be between 48 MHz and the maximum FMPLL frequency (as specified in the device datasheet).

Appendix C Revision History

Table 10 provides a revision history for this document.

Table 10. Revision History

Revision Number	Substantive Changes	Date of Release
0	Initial Release.	July 2008
1	• Changed title from “Using Odd Predividers on the MPC5500 FMPLL” to “Using Predividers on the MPC5500 FMPLL.” • Section 2.5 updated to include even predividers and describe the failure conditions in more detail. • Added sections for 132 MHz system frequency with an 8 MHz crystal, and 132 MHz system frequency with a 16 MHz crystal. • Updated the headings for what are now sections 3.3, 3.4, and 3.5. • Added the current errata wording in Appendix A. • Added predivider-of-one examples as Appendix B. • Added revision history as Appendix C. • Clean up throughout.	May 2009
2	• Removed reference to unavailable application note.	12/2012
3	• Removed section “128 MHz System Frequency with 8 MHz Crystal and Divide-by-One Predivider”	February 2015

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