

Electrical Connection Recommendations for the Exposed Pad on QFN and DFN Packages

1 Introduction

The exposed pad (EP) on Freescale microcontroller Dual Flat Pack No-lead (DFN) and Quad Flat Pack No-lead (QFN) packages is intended to improve the thermal performance of this leadless near Chip Scale Package (CSP) when it is mounted on a printed circuit board. There are no firm rules in the semiconductor industry for soldering or biasing the exposed pad. Instead, system designers are left to exercise their engineering judgment on how to connect the EP to the PCB. This engineering bulletin gives connection recommendations specifically for microcontrollers in DFN and QFN packages.

Freescale application note AN4530, QFN (Quad Flat Pack No-Lead), contains specific guidelines for PCB design and soldering when using QFN and DFN packages. Those guidelines will not be duplicated here.

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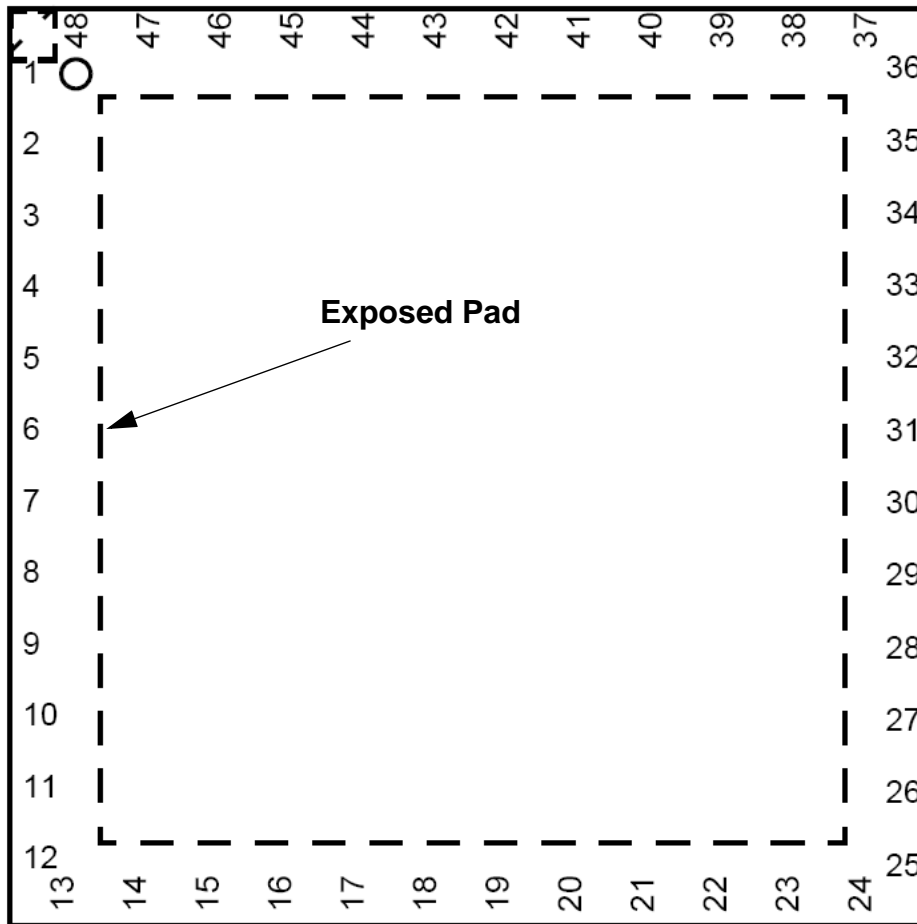


Figure 1. 48 QFN Pinout — Top View

2 Overview

QFN and DFN packages are just slightly larger than the silicon die that is contained in the package. When compared to traditional leaded surface mount devices, this small package size significantly affects the power (heat) dissipation of the device due to the reduced amount of metal leadframe and volume of plastic surrounding the die. Freescale uses a thermally enhanced pad (also known as an exposed pad) on many of our QFN and DFN packages as the die mounting surface to provide a path to remove heat from the package. See [Figure 1](#), [Figure 2](#), and [Figure 4](#).

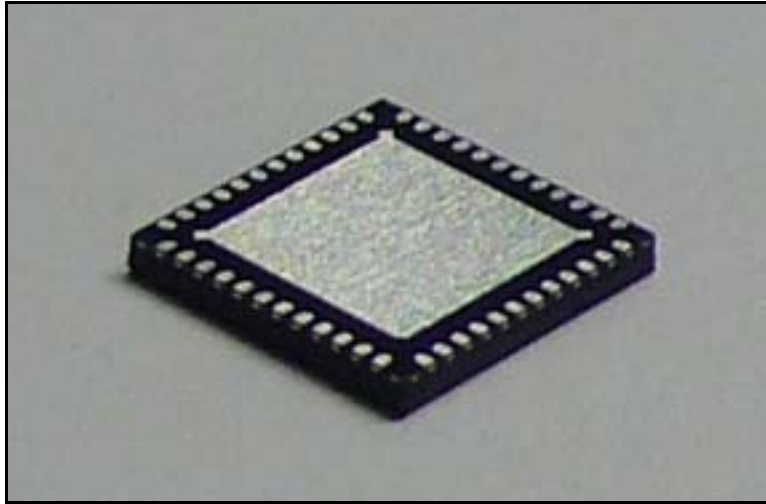


Figure 2. 48 QFN Exposed Pad — Bottom Perspective

Compared to traditional surface mount packages, such as the Leaded Quad Flat Pack (LQFP), the QFN has the same epoxy die attach, wire bonding, and plastic encapsulation methods. Likewise, there is no electrical connection between the die pins or terminals and the flag or exposed pad - the epoxy bonds the die substrate to the flag/EP but provides no external electrical connection for the circuitry on the die. The cross-sections in [Figure 3](#) and [Figure 4](#) show similarities between the assembly of a typical LQFP package and a QFN with an exposed pad.

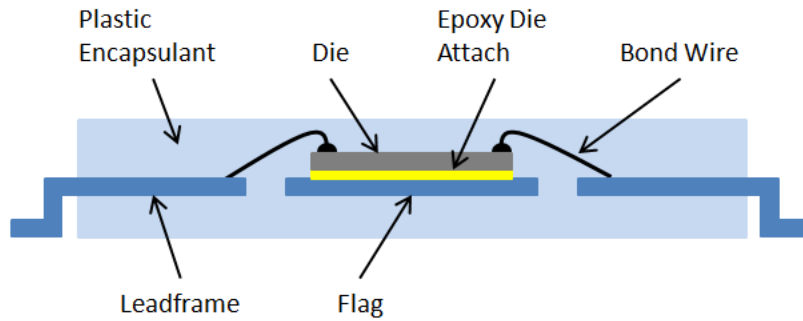


Figure 3. Typical Cross-section of LQFP

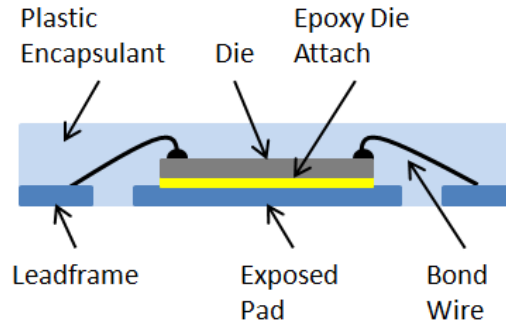


Figure 4. Typical Cross-section of QFN with an Exposed Pad

Many Freescale MCU data sheets contain package dimensional information that shows the exposed pad in the QFN or DFN package drawing, but do not identify the exposed pad in the pin descriptions, mainly because the EP is not a circuit terminal. However, because the exposed pad forms a plane under the die we recommend connecting the EP to MCU ground to improve EMC performance.

Note that some Freescale MCUs are packaged in a special MAPBGA package that is called a laminate QFN. The square pads on the laminate QFN must be connected to MCU ground because these are connected to the MCU VSS pins.

3 Recommendations

Automotive or safety critical applications: solder the exposed pad to the PCB and connect the exposed pad to the MCU ground. This provides reliable mechanical connection for the chip and a reliable ground plane for EMC purposes. The PCB ground layer dimensions and thermal via connections will be factors in removing heat from the package. Refer to AN4530 for configuration of the PCB land or land pattern.

Low-power applications: the exposed pad may not need to be soldered to the PCB if the chip power dissipation is very low (tens of milliwatts) and the application operating temperature range is no higher than about 60°C. A more reliable mechanical connection of the chip to the board would be to solder the EP to a copper land (or land pattern) on the PCB under the chip. If the EP land is connected to a potential, that potential must be MCU ground. EMC performance will be enhanced when the EP is soldered to the PCB and connected to MCU ground.

High-power applications: the exposed pad must be soldered to a PCB land or land pattern that has sufficient connections to heat sinking areas of copper on the PCB. The connections include thermal vias under the exposed pad to bond the land pattern to the heat sinking copper. Freescale recommends that the exposed pad and heat sink should be connected to the MCU ground to enhance EMC robustness.

4 Summary

Freescale recommends electrically connecting the exposed pad of QFN and DFN devices to MCU ground and soldering the exposed pad to a suitable land pattern on the PCB. The exposed pad should never be connected to a potential other than MCU ground.



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