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MPC577xK STCU BIST Configuration

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1. Introduction

This document describes the MPC577xK default Self-Test Control Unit (STCU) configuration for offline Built-In Self-Test (BIST). The default STCU configuration is programmed in the MPC577xK UTEST FLASH section during factory test and enables BIST execution by default. BIST will execute at device startup events, as specified in the MPC577xK Reference Manual. This document provides instructions for disabling BIST execution. Details of the default configuration settings for BIST faults and recommendations on handling BIST faults are also included in this document.

Contents

2. STCU BIST Configuration Summary

- Offline BIST enabled by default
- Overall coverage level (with BIST enabled): ASIL-D
- PLL0: 66 MHz with IRCOSC reference
- LBIST
  - Logic partitions 0-7 (see table 1), tested in parallel and sequentially
  - Coverage/Algorithm: 90% Stuck-at
  - Execution time: 11.78 ms (+/- 8% according to IRC trim tolerance)
- MBIST
  - Memory partitions 0-91, tested in parallel
  - Coverage/Algorithm: Full test (including PMOS)
  - Execution time: 16.98 ms (+/- 8% according to IRC trim tolerance)

3. Disable BIST Execution

The default BIST configuration for MPC577xK enables BIST execution at start-up. To prevent execution of BIST at start-up, the STCU configuration must be adjusted to disable offline BIST.

To disable BIST, a single Device Configuration Format (DCF) record should be written to the UTEST FLASH section in the first available space immediately after the last valid DCF entry in the UTEST. The DCF record area starts at 0x00400200. After the DCF record area, the first address which contains 0xFFFFFFFF_FFFFFFFF is the first open UTEST memory address, as shown in figure 1. For MPC577xK maskset 1N76P, the first open address is 0x00400668.

The following DCF record should be written to the first open UTEST memory address to disable BIST: 0x7F000000, 0x0008000C.

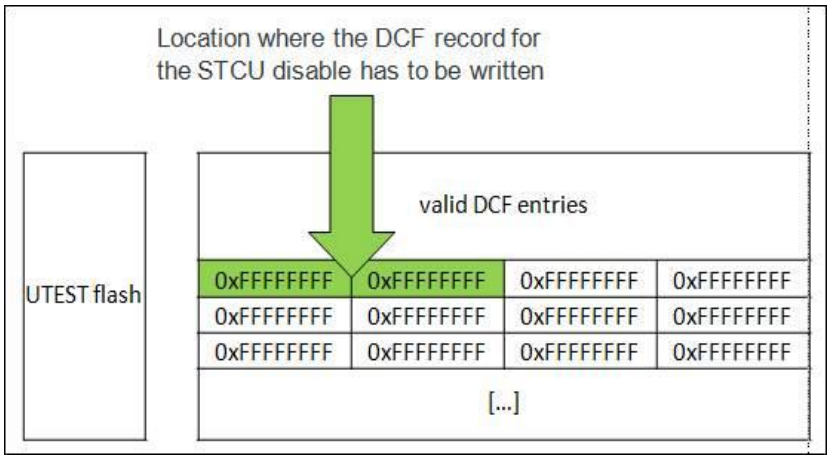

Figure 1. How to identify first open UTEST memory address

4. BIST Execution

When enabled, BIST will execute at the following start-up events:

- Power-on reset (POR)
- External reset with the reset sequence configured in Reset Generation Module to start from PHASE1
- Destructive reset

When offline BIST execution is enabled, MBIST is executed before LBIST.

5. BIST Clock Settings

STCU offline BIST uses the PLL and IRC clock to generate an internal 66 MHz clock. No external clocks are required to run offline self-test.

6. LBIST

LBIST operates on the digital logic of the MPC577xK and uses scan test techniques to provide high coverage defect detection. The digital logic of the MPC577xK is segmented into eight individual LBIST partitions, as shown in table 1.

Table 1. LBIST Module Partitioning

Partition	Logic Partition
0	INTC, ENET
1	AIPS1, PBRIDGE_1 peripherals
2	RCCU, Check core
3	Core0, Core1
4	MEMU, Flash, PRAM_CTRL, PFLASH_CTRL
5	AIPS0, PBRIDGE_0 peripherals
6	SPT, WGM, PDI, CTE
7	MC_ME, JTAG

The default execution order of the LBIST partitions is illustrated in figure 2. Note that LBIST tests are executed both in parallel and sequentially, to provide an optimal balance of execution time and current consumption.

Phase 1	Phase 2	Phase 3	Phase 4
LBIST0	LBIST3	LBIST4	LBIST6
LBIST1		LBIST5	LBIST7
LBIST2			

Figure 2. LBIST execution order

The default LBIST configuration for the MPC577xK provides 90% stuck-at coverage.

7. MBIST

MBIST is executed for each of the memories listed in table 2. The memories are segmented into 92 individual memory partitions, as shown in table 2. The default MBIST configuration tests all MPC577xK memory partitions, 0-91, in parallel.

The default MBIST configuration for the MPC577xK executes Full Test Mode with PMOS test, which provides > 90% coverage.

Table 2. MBIST Memory Partitioning

Partition Number	Memory Association
0	BAM_ROM
1	CAN_0
2	CAN_1
3	FLEXRAY DATA
4	FLEXRAY LUT
5	CAN_2
6	CAN_3
7	ETHERNET
8	CORE0 DCACHE
9	
10	
11	
12	CORE0 DTAG
13	CORE0 DTCM
14	
15	CORE0 ICACHE
16	
17	
18	
19	CORE0 ITAG
20	CORE1 DCACHE
21	
22	CORE1 DTAG
23	CORE1 DTCM
24	
25	CORE1 ICACHE
26	
27	CORE1 ITAG
28	CORE2 DCACHE
29	
30	CORE2 DTAG

Partition Number	Memory Association
31	CORE2 DTCM
32	
33	CORE2 ICACHE
34	
35	CORE2 ITAG
36	DMA
37	PRAM0
38	
39	PRAM1
40	
41	PRAM2
42	
43	PRAM3
44	
45	PRAM4
46	
47	
48	
49	PRAM5
50	
51	
52	
53	PRAM6
54	
55	
56	
57	PRAM7
58	
59	
60	
61	RESERVED
62	
63	SPT
64	
65	
66	
67	
68	
69	
70	

Partition Number	Memory Association
71	
72	
73	
74	
75	
76	
77	
78	
79	SPT TWIDDLE
80	
81	
82	
83	
84	
85	
86	
87	CWG LUT
88	
89	
90	
91	MCAN

8. Fault Handling

The default configuration for the MPC577xK sets all BIST faults as recoverable faults.

After BIST execution, application software should check the following registers to determine whether a fault has occurred:

- STCU2 error register: STCU2_ERR_STAT (will read all zeros if no fault occurred)
  - Recoverable Faults Status Flag: STCU2_ERR_STAT[RFSF]
  - Unrecoverable Faults Status Flag: STCU2_ERR_STAT[UFSF]

If a fault has occurred, the following STCU2 status registers should be read to determine the source of the fault:

Table 3. STCU2 BIST Status Registers

STCU Register Name	Register Description	Expected value if no fault after BIST execution
STCU2_MBSL	Off-Line MIBST Status Low Register	0xFFFF_FFFF
STCU2_MBSM	Off-Line MBIST Status Medium Register	0xFFFF_FFFF
STCU2_MBSH	Off-Line MBIST Status High Register	0x0FFF_FFFF
STCU2_MBEL	Off-Line MBIST End Flag Low Register	0xFFFF_FFFF

STCU Register Name	Register Description	Expected value if no fault after BIST execution
STCU2_MBEM	Off-Line MBIST End Flag Medium Register	0xFFFF_FFFF
STCU2_MBEH	Off-Line MBIST End Flag High Register	0x0FFF_FFFF
STCU2_LBS	Off-Line LBIST Status Register	0X0000_00FF
STCU2_LBE	Off-Line LBIST End Flag Register	0X0000_00FF

The STCU2 communicates fault information to the Fault Control and Collection Unit (FCCU) to indicate the occurrence of an unrecoverable fault and/or a recoverable fault failure during the BIST sequence. If a fault does occur, application software should check the FCCU status registers to see if a multi-bit error has occurred. The FCCU has dedicated fault input mappings for STCU BIST fault indications, as shown in table 4.

Table 4. FCCU Non-Critical Fault Mapping for STCU Module

FCCU Non-Critical Fault Number	Description
NCF[6]	Critical fault indication from STCU
NCF[7]	Non-critical fault indication from STCU
NCF[8]	Critical fault indication from STCU in case LBIST or MBIST control signals go to wrong condition during user application

Refer to the FCCU module chapter in the device reference manual for more information. Consult the MPC577xK Reference Manual and Safety Manual to ensure that fault handling is performed correctly in order to achieve required safety coverage levels.

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