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DSP56721

Silicon Revision: 0M78E

Table 1 defines Severity values for errata described in this document.

Table 1. Definitions of Errata Severity

Severity	Errata Type	Meaning	Workaround
1	Critical	Failure mode that severely inhibits the use of the device for all or a majority of intended applications	Unavailable
2	High	Failure mode that might restrict or limit the use of the device for all or a majority of intended applications	Generally available
3	Moderate	Unexpected behavior that does not cause significant problems for the intended applications of the device	Generally available

Table 3 lists known chip errata affecting the versions of DSP56721 identified in the final column. Table 2 summarizes the errata described in more detail in Table 3.

Table 2. Chip Errata Summary for DSP56721

Severity	Erratum ID	Title	Silicon Revision
3	ES151	Incorrect Chip ID in CIM and JTAG modules on the DSP56721	0M78E
3	ES152	Access to External Memory Space Hangs Device.	0M78E
3	ES153	Clearing Individual ESAI Interrupt Enable Bits	0M78E

Table 3. Chip Errata for DSP56721

Severity	Erratum ID	Summary	Details	Silicon Revision
3	ES151	**Module Affected:** CIM/JTAG **Title:** Incorrect Chip ID in CIM and JTAG modules on the DSP56721 **Release Date:** March 2007	**Description:** In chapter 6 “Core Integration Module (CIM, CIM_1)” of the DSP56720/721 Reference Manual, there are CHIDR registers at address X:$FFFFF5 for both cores. In section 6.2.1, the CHIDR register value for the DSP56721 device is 0x000721 for Core-0 and is 0x010721 for Core-1. But in the actual DSP56721 device, the CHIDR register value for the DSP56721 device is 0x000720 for Core-0 and 0x010720 for Core-1, which is the same value that is in a DSP56720 device. Also note that the JTAG ID for both DSP56720 and DSP56721 devices is the same, and is 32'b0000_0001_1110_1101_0000_0000_0001_1101. **Workaround:** To determine which device it is over the register interface, our customer can check the package ID bits if the Chip ID register (CHIDR) is 720. The package ID is bit 23:22 of register at address Y:FFFFE4. The package ID scheme is: 10-- DSP56721 80-pin LQPF package 01-- DSP56721 144-pin LQFP package 11-- DSP56720 144-pin LQFP package Note that this workaround does not work for the JTAG ID. **Fix Plan/Status:** Not fixed.	0M78E
3	ES152	**Module Affected:** both DSP cores and DMAs **Title:** Access to External Memory Space Hangs Device **Release Date:** March 2007	**Description:** Accessing the external memory space of the DSP56721 by either DSP core (or either DMA) will cause that DSP core (or DMA) to stop. All other modules (including peripherals) will continue operating. A reset is needed to restore the DSP core or DMA to normal operation. Note that there is no External Memory Controller (EMC) on the DSP56721 device. **Workaround:** Do not attempt to access the external memory space on the DSP56721 device. **Fix Plan/Status:** Not fixed.	0M78E

Table 3. Chip Errata for DSP56721 (continued)

Severity	Erratum ID	Summary	Details	Silicon Revision
3	ES153	**Module Affected:** ESAI/ESAI_1/ESAI_2/ ESAI_3 **Title:** Clearing Individual ESAI Interrupt Enable Bits **Release Date:** September 2007	**Description:** If an ESAI transmit interrupt enable bit (TEIE, TEDIE, TIE, TLIE) or an ESAI receive interrupt enable bit (REIE, REDIE, RIE, RLIE) is cleared by software while that same interrupt is asserted then the interrupt vector received by the DSP56300 core may be for the ESAI Receive Data interrupt if no other ESAI interrupts are pending. This only occurs if the interrupt is disabled before the interrupt vector is calculated but after the DSP56300 core has accepted that interrupt as the highest priority pending interrupt. The ESAI Receive Data interrupt does not need to be enabled for this to happen. This errata also applies to ESAI_1, ESAI_2 and ESAI_3. **Workaround:** Mask the ESAI interrupt in the IPRP register while clearing an individual ESAI interrupt enable bit. It is also valid to globally mask all interrupts while the individual ESAI interrupt is disabled, but this is not required. **Fix Plan/Status:** Not fixed.	0M78E

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