

DSP56721

Silicon Revision: 0M78E

[Table 1](#) defines Severity values for errata described in this document.

Table 1. Definitions of Errata Severity

Severity	Errata Type	Meaning	Workaround
1	Critical	Failure mode that severely inhibits the use of the device for all or a majority of intended applications	Unavailable
2	High	Failure mode that might restrict or limit the use of the device for all or a majority of intended applications	Generally available
3	Moderate	Unexpected behavior that does not cause significant problems for the intended applications of the device	Generally available

[Table 3](#) lists known chip errata affecting the versions of DSP56721 identified in the final column. [Table 2](#) summarizes the errata described in more detail in [Table 3](#).

Table 2. Chip Errata Summary for DSP56721

Severity	Erratum ID	Title	Silicon Revision
3	ES151	Incorrect Chip ID in CIM and JTAG modules on the DSP56721	0M78E
3	ES152	Access to External Memory Space Hangs Device.	0M78E
3	ES153	Clearing Individual ESAI Interrupt Enable Bits	0M78E

Table 3. Chip Errata for DSP56721

Severity	Erratum ID	Summary	Details	Silicon Revision
3	ES151	<p>Module Affected: CIM/JTAG</p> <p>Title: Incorrect Chip ID in CIM and JTAG modules on the DSP56721</p> <p>Release Date: March 2007</p>	<p>Description: In chapter 6 “Core Integration Module (CIM, CIM_1)” of the DSP56720/721 Reference Manual, there are CHIDR registers at address X:\$FFFFFF5 for both cores. In section 6.2.1, the CHIDR register value for the DSP56721 device is 0x000721 for Core-0 and is 0x010721 for Core-1.</p> <p>But in the actual DSP56721 device, the CHIDR register value for the DSP56721 device is 0x000720 for Core-0 and 0x010720 for Core-1, which is the same value that is in a DSP56720 device.</p> <p>Also note that the JTAG ID for both DSP56720 and DSP56721 devices is the same, and is 32'b0000_0001_1110_1101_0000_0000_0001_1101.</p> <p>Workaround: To determine which device it is over the register interface, our customer can check the package ID bits if the Chip ID register (CHIDR) is 720. The package ID is bit 23:22 of register at address Y:FFFFE4.</p> <p>The package ID scheme is: 10-- DSP56721 80-pin LQPF package 01-- DSP56721 144-pin LQFP package 11-- DSP56720 144-pin LQFP package</p> <p>Note that this workaround does not work for the JTAG ID.</p> <p>Fix Plan/Status: Not fixed.</p>	0M78E
3	ES152	<p>Module Affected: both DSP cores and DMAs</p> <p>Title: Access to External Memory Space Hangs Device</p> <p>Release Date: March 2007</p>	<p>Description: Accessing the external memory space of the DSP56721 by either DSP core (or either DMA) will cause that DSP core (or DMA) to stop. All other modules (including peripherals) will continue operating. A reset is needed to restore the DSP core or DMA to normal operation. Note that there is no External Memory Controller (EMC) on the DSP56721 device.</p> <p>Workaround: Do not attempt to access the external memory space on the DSP56721 device.</p> <p>Fix Plan/Status: Not fixed.</p>	0M78E

Table 3. Chip Errata for DSP56721 (continued)

Severity	Erratum ID	Summary	Details	Silicon Revision
3	ES153	<p>Module Affected: ESAI/ESAI_1/ESAI_2/ ESAI_3</p> <p>Title: Clearing Individual ESAI Interrupt Enable Bits</p> <p>Release Date: September 2007</p>	<p>Description: If an ESAI transmit interrupt enable bit (TEIE, TEDIE, TIE, TLIE) or an ESAI receive interrupt enable bit (REIE, REDIE, RIE, RLIE) is cleared by software while that same interrupt is asserted then the interrupt vector received by the DSP56300 core may be for the ESAI Receive Data interrupt if no other ESAI interrupts are pending.</p> <p>This only occurs if the interrupt is disabled before the interrupt vector is calculated but after the DSP56300 core has accepted that interrupt as the highest priority pending interrupt. The ESAI Receive Data interrupt does not need to be enabled for this to happen.</p> <p>This errata also applies to ESAI_1, ESAI_2 and ESAI_3.</p> <p>Workaround: Mask the ESAI interrupt in the IPRP register while clearing an individual ESAI interrupt enable bit. It is also valid to globally mask all interrupts while the individual ESAI interrupt is disabled, but this is not required.</p> <p>Fix Plan/Status: Not fixed.</p>	0M78E

How to Reach Us:

Home Page:
www.freescale.com

Web Support:
<http://www.freescale.com/support>

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, EL516
2100 East Elliot Road
Tempe, Arizona 85284
+1-800-521-6274 or +1-480-768-2130
www.freescale.com/support

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
www.freescale.com/support

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

For Literature Requests Only:
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-441-2447 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners.

© Freescale Semiconductor, Inc. 2007. All rights reserved.