ERRATA SHEET

Date: **2008 July 9**
Document Release: **Version 1.0**
Device Affected: **LPC2104/01**

This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document.

Each deviation is assigned a number and its history is tracked in a table at the end of the document.

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NXP
Semiconductors

founded by Philips

Document revision history

Rev	Date	Description
1.0	July 9, 2008	1. First Version

Identification:

The LPC2104/01 devices typically have the following top-side marking:

LPC2104xxx

/01

xxxxxxx

xxYYWWR

The last letter in the last line (field ‘R’) will identify the device revision. This Errata Sheet covers the following revisions of the LPC2104/01:

Revision Identifier (R)	Comment
‘E’	Initial device revision

Field ‘YY’ states the year the device was manufactured. Field ‘WW’ states the week the device was manufactured during that year.

Errata Overview - Functional Problems

Functional Problem	Short Description	Device Revision the problem occurs in
Core.1	Incorrect load of the link register	E

Errata Overview - AC/DC Deviations

AC/DC Deviation	Short Description	Device Revision the deviation occurs in
N/A	N/A	N/A

Errata Notes

Note	Short Description
N/A	N/A

Functional Problems of LPC2104/01

Core.1 Incorrect update of the Abort Link register in Thumb state

Introduction: If the processor is in Thumb state and executing the code sequence STR, STMIA or PUSH followed by a PC relative load, and the STR, STMIA or PUSH is aborted, the PC is saved to the abort link register.

Problem: In this situation the PC is saved to the abort link register in word resolution, instead of half-word resolution.

Conditions:

The processor must be in Thumb state, and the following sequence must occur:

<any instruction>

<STR, STMIA, PUSH> <---- data abort on this instruction

LDR rn, [pc,#offset]

In this case the PC is saved to the link register R14_abt in only word resolution, not half-word resolution. The effect is that the link register holds an address that could be #2 less than it should be, so any abort handler could return to one instruction earlier than intended.

Work around: In a system that does not use Thumb state, there will be no problem.

In a system that uses Thumb state but does not use data aborts, or does not try to use data aborts in a recoverable manner, there will be no problem.

Otherwise the workaround is to ensure that a STR, STMIA or PUSH cannot precede a PC-relative load. One method for this is to add a NOP before any PC-relative load instruction. However this is would have to be done manually.