

# ES\_LPC407x/8x

Errata sheet LPC407x/8x

Rev. 2.1 — 11 January 2022

Errata sheet

## Document information

Info	Content
<b>Keywords</b>	LPC4088FBD208; LPC4088FET208; LPC4088FET180; LPC4088FBD144; LPC4078FBD208; LPC4078FET208; LPC4078FET180; LPC4078FBD144; LPC4078FBD80; LPC4076FET180; LPC4076FBD144; LPC4074FBD144; LPC4074FBD80; LPC4072FBD80, LPC407x, LPC408x, errata
<b>Abstract</b>	<p>This errata sheet describes both the known functional problems and any deviations from the electrical specifications known at the release date of this document.</p> <p>Each deviation is assigned a number and its history is tracked in a table.</p>



## Revision history

Rev	Date	Description
2.1	20220111	<ul style="list-style-type: none"><li>Revised IBAT.1 errata workaround with further details in <a href="#">Section 3.3 “IBAT.1: Typical lots have about 5% parts with higher than normal IBAT current when only V<sub>BAT</sub> power is provided (VDD<sub>REG</sub> is grounded)”</a>.</li></ul>
2	20140603	<ul style="list-style-type: none"><li>Updated ETHERNET.1 work-around</li></ul>
1.3	20131126	<ul style="list-style-type: none"><li>Added IBAT.1</li></ul>
1.2	20130214	<ul style="list-style-type: none"><li>Added I2C.1</li></ul>
1.1	20121207	<ul style="list-style-type: none"><li>Added ETHERNET.1</li></ul>
1	20120924	<ul style="list-style-type: none"><li>Initial version</li></ul>

## Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 1. Product identification

The LPC407x/8x devices typically have the following top-side marking:

LPC40xxXXX

xxxxxxx

xxYYWWR[x]

The last digit in the last line (field 'R') will identify the device revision. Note: pre-production parts are marked differently and this system does not apply. This Errata Sheet covers the following revisions of the LPC407x/8x:

**Table 1. Device revision table**

Revision identifier (R)	Revision description
'-'	Initial device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

## 2. Errata overview

**Table 2. Functional problems table**

Functional problems	Short description	Revision identifier	Detailed description
ETHERNET.1	In Ethernet MII mode, the transmit data TXD3:0 and transmit enable TX_EN incorrectly reference RX_CLK in data transmission.	'-'	<a href="#">Section 3.1</a>
I2C.1	In slave-transmitter mode, the device set in monitor mode must write a dummy value of 0xFF into the DAT register.	'-'	<a href="#">Section 3.2</a>
IBAT.1	Typical lots have about 5 % parts with higher than normal I <sub>BAT</sub> current when only V <sub>BAT</sub> power is provided (VDD <sub>BAT</sub> is grounded).	'-'	<a href="#">Section 3.3</a>

**Table 3. AC/DC deviations table**

AC/DC deviations	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

**Table 4. Errata notes**

Note	Short description	Revision identifier	Detailed description
Note.1	During power-up, an unexpected glitch (low pulse) could occur on the port pins as the V <sub>DD</sub> supply ramps up.	'-'	<a href="#">Section 5.1</a>

### 3. Functional problems detail

---

#### 3.1 ETHERNET.1

**Introduction:**

The Ethernet block contains a full featured 10 Mbps or 100 Mbps Ethernet MAC (Media Access Controller) designed to provide optimized performance through the use of DMA hardware acceleration. The Ethernet block interfaces between an off-chip Ethernet PHY using the MII (Media Independent Interface) or RMI (reduced MII) protocol and the on-chip MIIM (Media Independent Interface Management) serial bus.

**Problem:**

In MII mode, the transmit data TXD3:0 and transmit enable TX\_EN should reference the TX\_CLK from the Ethernet PHY. However, due to a configuration error in the chip, the transmit data TXD3:0 and transmit enable TX\_EN reference RX\_CLK in data transmission. The consequence of this error is that a small percentage of packets cannot be received by the PHY.

**Work-around:**

None.

**Note:** There is no issue in RMI mode operation.

## 3.2 I2C.1

### Introduction:

The I2C monitor mode allows the I2C module to monitor traffic on the I<sup>2</sup>C-bus without actually participating in traffic or interfering with the I<sup>2</sup>C-bus.

### Problem:

In slave-transmitter mode, the device set in the monitor mode must write a dummy value of 0xFF into the DAT register. If this is not done, the received data from the slave device will be corrupted. To allow the monitor mode to have sufficient time to process the data on the I<sup>2</sup>C-bus, the device may need to have the ability to stretch the I2C clock. Under this condition, the I2C monitor mode is not 100% non-intrusive.

### Work-around:

When setting the device in monitor mode, enable the ENA\_SCL bit in the MMCTRL register to allow clock stretching.

Software code example to enable the ENA\_SCL bit:

```
LPC_I2C_MMCTRL |= (1<<1);    //Enable ENA_SCL bit
```

In the I2C ISR routine, for the status code related to slave-transmitter mode, write the value of 0xFF into the DAT register to prevent data corruption. In order to avoid stretching the SCL clock, the data byte can be saved in a buffer and processed in the Main loop. This ensures the SI flag is cleared as fast as possible.

Software code example for slave-transmitter mode:

```
case 0xA8:    // Own SLA + R has been received, ACK returned
case 0xB0:
case 0xB8:    // data byte in DAT transmitted, ACK received
case 0xC0:    // (last) data byte transmitted, NACK received
case 0xC8:    // last data byte in DAT transmitted, ACK received
    DataByte = LPC_I2C->DATA_BUFFER; //Save data. Data can be processed in Main loop
    LPC_I2C->DAT = 0xFF;             // Pretend to shift out 0xFF
    LPC_I2C->CONCLR = 0x08;         // clear flag SI
break;
```

### 3.3 IBAT.1: Typical lots have about 5% parts with higher than normal IBAT current when only $V_{BAT}$ power is provided ( $VDD_{REG}$ is grounded)

#### Introduction:

Two independent power domains ( $VDD_{REG}$  domain and  $V_{BAT}$  domain) are provided that allow the bulk of the device to have power removed while maintaining operation of the Real Time Clock (RTC). The  $V_{BAT}$  pin supplies power only to the RTC domain and is active when  $V_{BAT}$  is greater than  $VDD_{REG}$ . The RTC requires a minimum of power to operate, which can be supplied by an external battery ( $V_{BAT}$ ). Whenever the device core power ( $VDD_{REG}$ ) is greater than  $V_{BAT}$ ,  $VDD_{REG}$  is used to operate the RTC. When  $VDD_{REG}$  is grounded, the IBAT is typically around 1  $\mu$ A.

#### Problem:

Typical lots have about 5 % parts with IBAT current as high as about 10  $\mu$ A when only  $V_{BAT}$  is applied ( $VDD_{REG}$  is grounded). This is due to a leakage current path in a level shifter in the power domain.

#### Work-around:

The problematic leakage path is disabled when the part is entered into Deep power-down mode prior to  $VDD_{REG}$  powering off. The application should put the device into Deep power-down mode and disable the BOD reset (bit 4, PCON register) before the  $VDD_{REG}$  power is grounded. The BOD ISR could potentially be used for this purpose.

## 4. AC/DC deviations detail

---

n/a

## 5. Errata notes

---

### 5.1 Note.1

The General Purpose I/O (GPIO) pins have configurable pull-up/pull-down resistors where the pins are pulled up to the  $V_{DD}$  level by default. During power-up, an unexpected glitch (low pulse) could occur on the port pins as the  $V_{DD}$  supply ramps up.

## 6. Contents

<b>1</b>	<b>Product identification</b> .....	<b>3</b>	<b>3.3</b>	IBAT.1: Typical lots have about 5% parts with higher than normal IBAT current when only $V_{BAT}$ power is provided ( $VDD_{REG}$ is grounded) .....	<b>6</b>
<b>2</b>	<b>Errata overview</b> .....	<b>3</b>			
<b>3</b>	<b>Functional problems detail</b> .....	<b>4</b>	<b>4</b>	<b>AC/DC deviations detail</b> .....	<b>7</b>
3.1	ETHERNET.1 .....	4	<b>5</b>	<b>Errata notes</b> .....	<b>7</b>
3.2	I2C.1 .....	5	5.1	Note.1 .....	7
			<b>6</b>	<b>Contents</b> .....	<b>8</b>



## How To Reach Us

### Home Page:

[nxp.com](http://nxp.com)

### Web Support:

[nxp.com/support](http://nxp.com/support)

**Limited warranty and liability** — Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.

NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address: [nxp.com/SalesTermsandConditions](http://nxp.com/SalesTermsandConditions).

**Right to make changes** - NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Security** — Customer understands that all NXP products may be subject to unidentified or documented vulnerabilities. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately. Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. NXP has a Product Security Incident Response Team (PSIRT) (reachable at [PSIRT@nxp.com](mailto:PSIRT@nxp.com)) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP, the NXP logo, NXP SECURE CONNECTIONS FOR A SMARTER WORLD, COOLFLUX, EMBRACE, GREENCHIP, HITAG, ICODE, JCOP, LIFE, VIBES, MIFARE, MIFARE CLASSIC, MIFARE DESFire, MIFARE PLUS, MIFARE FLEX, MANTIS, MIFARE ULTRALIGHT, MIFARE4MOBILE, MIGLO, NTAG, ROADLINK, SMARTLX, SMARTMX, STARPLUG, TOPFET, TRENCHMOS, UCODE, Freescale, the Freescale logo, Altivec, CodeWarrior, ColdFire, ColdFire+, the Energy Efficient Solutions logo, Kinetis, Layerscape, MagniV, mobileGT, PEG, PowerQUICC, Processor Expert, QorIQ, QorIQ Qonverge, SafeAssure, the SafeAssure logo, StarCore, Symphony, VortiQa, Vybrid, Airfast, BeeKit, BeeStack, CoreNet, Flexis, MXC, Platform in a Package, QUICC Engine, Tower, TurboLink, EdgeScale, EdgeLock, eIQ, and Immersive3D are trademarks of NXP B.V. All other product or service names are the property of their respective owners. AMBA, Arm, Arm7, Arm7TDMI, Arm9, Arm11, Artisan, big.LITTLE, Cordio, CoreLink, CoreSight, Cortex, DesignStart, DynamIQ, Jazelle, Keil, Mali, Mbed, Mbed Enabled, NEON, POP, RealView, SecurCore, Socrates, Thumb, TrustZone, ULINK, ULINK2, ULINK-ME, ULINK-PLUS, ULINKpro, µVision, Versatile are trademarks or registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere. The related technology may be protected by any or all of patents, copyrights, designs and trade secrets. All rights reserved. Oracle and Java are registered trademarks of Oracle and/or its affiliates. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks

*Table continues on the next page...*

and service marks licensed by Power.org. M, M Mobileye and other Mobileye trademarks or logos appearing herein are trademarks of Mobileye Vision Technologies Ltd. in the United States, the EU and/or other jurisdictions.

© NXP B.V. 2012-2021.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 11 January 2022  
Document identifier: ES\_LPC407X\_8X

The logo for ARM, consisting of the lowercase letters 'arm' in a blue, sans-serif font.