ES_LPC5410x

Errata sheet LPC5410x

Rev. 2.4 — 19 January 2024 **Errata**

Document information

Information	Content
Keywords	LPC54102J512UK49; LPC54102J256UK49; LPC54101J512UK49; LPC54101J256UK49; LPC54102J512BD64; LPC54102J256BD64; LPC54101J512BD64; LPC54101J256BD64
Abstract	LPC5410x errata.

1 Product identification

The ES_LPC5410x LQFP64 package has the following top-side marking:

- First line: LPC5410xJyyy
  - x: 2 = dual core (M4, M0+), 1 = single core (M4)
  - yyy: flash size
- Second line: BD64
- Third line: xxxxxxxxxxxx
- Fourth line: xxxyywwx[R]z
  - yyww: Date code with yy = year and ww = week.
  - xR = boot code version and device revision.

The ES_LPC5410x WLCSP49 package has the following top-side marking:

- First line: LPC5410x
  - x: 2 = dual core (M4, M0+), 1 = single core (M4)
- Second line: JxxxUK49
  - xxx: flash size
- Third line: xxxxxxxx
- Fourth line: xxxyyww
  - yyww: Date code with yy = year and ww = week.
- Fifth line: xxxxx
- Sixth line: NXP x[R]z
  - xR = boot code version and device revision.

This Errata Sheet covers the following revisions of the LPC5410x:

Table 1. Device revision table

Revision identifier (R)	Revision description
‘1B’	Initial device revision with boot code version 17.1.
‘1C’	Second device revision with boot code version 17.1.

2 Errata overview

Table 2. Functional problems table

Functional problems	Short description	Revision identifier	Detailed description
RTC.1	The PDEN_32K_OSC bit gets cleared when the MCU wakes up from Deep power-down mode. This causes the RTC oscillator to change from bypass mode to crystal mode.	‘1B’, ‘1C’	Section 3.1
ISP.1	ISP (In-System Programming) command for UID (unique identification number) is not functional.	‘1B’, ‘1C’	Section 3.2
Frequency.1	The maximum operating system clock on the LPC5410x device is limited to 96 MHz.	‘1B’	Section 3.3
POWER_API.1	The set-voltage ROM API call does not configure the internal regulator correctly for the desired operating frequency.	‘1B’, ‘1C’	Section 3.4
CRP.1	Code read protection level 1 is not functional.	‘1B’, ‘1C’	Section 3.5

Table 2. Functional problems table*...continued*

Functional problems	Short description	Revision identifier	Detailed description
IRC.1	Accuracy of the Internal RC Oscillator (IRC) frequency for the LPC5410x Revision B devices in the WLCSP49 package are outside of the IRC specification.	'1B'	Section 3.6
PLL.1	P-divider set to 4 could generate the wrong output frequency from the PLL.	'1B', '1C'	Section 3.7

Table 3. AC/DC deviations table

AC/DC deviations	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

Table 4. Errata notes

Note	Short description	Revision identifier	Detailed description
n/a	n/a	n/a	n/a

3 Functional problems detail

3.1 RTC.1: The RTC oscillator changes from bypass control mode to crystal mode when waking up from Deep power-down mode.

Introduction:

On the LPC5410x, the low power 32 KHz RTC oscillator can be configured to run in crystal oscillation mode or bypass control mode. In crystal oscillation mode, the RTC oscillator is driven by an external 32 KHz crystal and in bypass control mode, the RTC oscillator is driven by an external 32 KHz clock. Bypass control mode can be entered by setting the PDEN_32K_OSC bit in the PDRUNCFG register (bit 24).

Problem:

The PDEN_32K_OSC bit gets cleared when the MCU wakes up from Deep power-down mode. This causes the RTC oscillator to change from bypass mode to crystal mode.

Work-around:

If using deep power-down mode, the crystal oscillation mode should be used instead of the bypass crystal mode. The bypass crystal mode can be used in active, sleep, deep-sleep, and power-down modes.

3.2 ISP.1: ISP (In-System Programming) command for UID (unique identification number) is not functional.

Introduction:

Each LPC5410x device contains a device serial number (four 32-bit words) for unique identification. The ISP call (ReadUID) can be performed via the USART interface to read the unique serial number where the word at the lowest address is sent first.

Problem:

On the LPC5410x, the read UID ISP command is not functional.

Work-around:

The unique serial number (four 32-bit words) can be directly read from address locations 0x01800100 to 0x0180010C.

3.3 Frequency.1: The maximum operating system clock on the LPC5410x device is limited to 96 MHz.

Introduction:

The LPC5410x data sheet specifies that the LPC5410x device can operate at CPU frequencies up to 100 MHz.

Problem:

To guard band for process, voltage, and temperature, the operating frequency is limited to ≤96 MHz.

Work-around:

None. Use CPU frequencies ≤96 MHz.

3.4 POWER_API.1: The set-voltage API ROM call does not configure the internal regulator correctly for the desired operating frequency.

Introduction:

On the LPC5410x device, the following power API ROM calls are provided to configure the system clock, and to manage the power consumption::

- set_pll: Configures the system PLL.
- set_voltage: Controls the device power consumption and the internal regulator for desired operating frequency.
- power_mode_configure: Entry to and wake up from the low power modes.

Problem:

The set-voltage API ROM call does not configure the internal regulator correctly for the desired operating frequency.

Work-around:

The power API library (power_lib) provided in NXP's LPC5410x LPCOpen v3.xx software platform must be used when calling the set_voltage API call. This library correctly configures the internal regulator for the desired operating frequency.

3.5 CRP.1: Code read protection level 1 is not functional

Introduction:

Code Read Protection is a mechanism that allows the user to enable different levels of security in the system so that access to the on-chip flash and use of the ISP can be restricted. When needed, CRP is invoked by programming a specific pattern in the flash image at offset 0x0000 02FC. There are three levels of code read protection available to the user.

For CRP1 level, erase page command can erase pages in sector 0 only when all pages in the user flash are selected for erase.

Problem:

All pages in sector 0 except page 0 can be erased, which results in erasing CRP1 level.

Work-around:

Use CRP2 level or CRP3 level for code read protection.

3.6 IRC.1: Accuracy of the Internal RC Oscillator (IRC) frequency for the LPC5410x revision B devices in the WLCSP49 package are outside of the IRC specification

Introduction:

The LPC5410x device has a 12 MHz internal RC oscillator (IRC) which can be optionally used as the CPU clock source or as the clock that drives the PLL and subsequently the CPU. The IRC frequency specification in Table 5 is in the LPC5410x data sheet:

Table 5. Dynamic characteristic: IRC oscillator

1.62 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	T_{amb} = 25 °C	[2]	12 -1 %	12	12 +1 %	MHz
		-40 °C ≤ T_{amb} ≤ +105 °C	[3]	12 -3.5 %	12	12 +3 %	MHz
		0 °C ≤ T_{amb} ≤ +85 °C	[3]	12 -2 %	12	12 +2.5 %	MHz

[1] Typical ratings are not guaranteed. The value listed is at room temperature (25 °C).
[2] Tested in production.
[3] Guaranteed by characterization, not tested in production.

Problem:

For the LPC5410x revision B devices in the WLCSP49 package, the IRC does not meet the limits specified in the LPC5410x data sheet. For temperature range -40 C to 0 C and +85 C to +105 C, this may affect the auto-baud routine's ability to synchronize with the host via serial port 0 during In-System Programming (ISP) at

higher baud rates. Table 6 shows the IRC specification for the LPC5410x revision B devices in the WLCSP49 package. This does not affect the LPC5410x devices in the LQFP64 package.

Table 6. Dynamic characteristic: IRC oscillator for revision B devices in WLCSP49 package

1.62 V ≤ V_{DD} ≤ 3.6 V.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	T_{amb} = 25 °C	12 -2 %	12	12 +2 %	MHz
		-40 °C ≤ T_{amb} ≤ +105 °C	12 -7 %	-	12 +6%	MHz
		-20 °C ≤ T_{amb} ≤ +85 °C	12 -5.5 %	-	12 +5 %	MHz
		0 °C ≤ T_{amb} ≤ +85 °C	12 -4 %	-	12 +3.5 %	MHz

[1] Typical ratings are not guaranteed. The value listed is at room temperature (25 °C).

Work-around:

This issue will be fixed in the next device revision C.

3.7 PLL.1: P-divider set to 4 could generate the wrong output frequency from the PLL

Introduction:

On the LPC5410x PLL, the Fcco frequency must be either the actual desired output frequency, or the desired output frequency times 2 x P, where P is range from 1 to 32 (2^5). The Fcco frequency must also be a multiple of the PLL reference frequency, which is either the PLL input, or the PLL input divided by N, where N is from 2 to 256.

Problem:

The P-divider when set for divide by 4 mode can erroneously arrive in divide by 2 mode. The high frequency spikes coming from the level shifter during startup of the PLL can cause the P-divider to jump into the wrong division state only when set in divide by 4 mode. This issue affects both the System PLL and Audio PLL.

Work-around:

Use other P values other than 4 to achieve desired output frequency. P = 1 – 32 and P ≠ 4.

4 AC/DC deviations detail

No known errata.

5 Errata notes

No known errata.

6 Revision history

Table 7. Revision history

Document ID	Release date	Description
ES_LPC5410x v. 2.4	19 January 2024	• Added Section 3.7

Table 7. Revision history...*continued*

Document ID	Release date	Description
ES_LPC5410x v. 2.3	21 November 2017	• Added Section 3.6
ES_LPC5410x v. 2.2	21 April 2017	• Added Section 3.5
ES_LPC5410x v. 2.1	16 December 2015	• Power ROM API.1 • Updated Section 1. Added boot code revision.
ES_LPC5410x v. 2.0	1 May 2015	• Added Section 3.1 • Added Section 3.2 • Frequency.1 • Updated product identification information
ES_LPC5410x v. 1	5 November 2014	• Initial version

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