Mask Set Errata for Mask 1N30D-2N30D

Introduction

This report applies to mask 1N30D-2N30D for these products:

- KINETIS

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2776	CRC: May have incorrect CRC result when performing CRC 8-bit or 16-bit writes with transpose enabled.
2547	DAC: 12-bit DAC buffer registers cannot be read.
2579	ENET: No support for IEEE 1588, TS_TIMER, timestamp timer overflow interrupt
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2686	WDOG: A watchdog reset while the system is in STOP or VLPS modes causes an incorrect wakeup sequence

e2550: ADC: ADC abort conversion logic error

Errata type: Errata
Description: The ADC abort conversion logic does not function as specified. Writes to the ADC CV1, CV2, OFS, PG, MG, CLPx, and CLMx registers will not abort a conversion.

Workaround: The abort conversion logic protects against changes to the ADC configuration during a conversion. To avoid this issue, do not change ADC settings during a conversion.

e2776: CRC: May have incorrect CRC result when performing CRC 8-bit or 16-bit writes with transpose enabled.

Errata type: Errata
Description: If performing CRC 8-bit or 16-bit writes with transpose enabled, the final checksum may have an incorrect CRC result.

Workaround: Write accesses to the CRC when transpose is enabled should always be 32-bit.

e2547: DAC: 12-bit DAC buffer registers cannot be read.

Errata type: Errata
Description: The 12-bit DAC buffer registers, DACx_DAT[1:15]L and DACx_DAT[1:15]H, cannot be read. The data that is written to these registers cannot be read. Only DACx_DAT0L and DACx_DAT0H can be read correctly.

Workaround: Treat the DACx_DAT[1:15]L and DACx_DAT[1:15]H registers as write-only registers because reads may return invalid data. The DAC buffer can still be used since the values written to these registers are valid.

e2579: ENET: No support for IEEE 1588, TS_TIMER, timestamp timer overflow interrupt

Errata type: Errata
Description: The TS_TIMER interrupt signal is not connected to the NVIC and will not generate an interrupt event. This interrupt is set when the 1588 counter matches the period register.

Workaround: One of the 1588 counter channels can be configured in output compare software-only mode to generate the periodic interrupt events.

This can be used to generate a counter periodic interrupt:

Initialize the timer:

1) Set the ENET_ATPER to the desired value

2) Set the ENET_ATINC register to match the selected 1588 clock.

3) Set the ENET_TCCRn register with ENET_ATPER – ENET_ATINC[INC] value. The ENET_ATINC[INC] offset is needed to match the internal 1588 clock synchronization.

4) Set the ENET_TCSRn[TMODE] register with the 0100 encoding for output compare software-only mode and the ENET_TCSRn[TIE] to enable the timer interrupt.

5) Set the ENET_TCCRn register again with ENET_ATPER – ENET_ATINC[INC] value because output compare value is double buffered.

6) Set the ENET_ATCR[PEREN] to enable periodical event and set the ENET_ATCR[EN] to start the timer

Configure inside the ISR:

1) 1588 interrupts are generated via the NVIC vector 91 using the periodic timer. For each interrupt event, load the output compare buffer (ENET_TCCRn register) with ENET_ATPER – ENET_ATINC[INC] value.

2) Clear ENET_TCSRn[TF] flag

3) Clear ENET_TGSRn respective channel flag.

e2596: EzPort and FTFL: The 64-bit flash programming command PGMSEC is not fully implemented.

Errata type: Errata

Description: The 64-bit flash programming command PGMSEC is not fully implemented. The command can be used by flash programming algorithms and is used by the EzPort serial flash programming interface.

Workaround: Use the 32-bit flash programming command PGM4 in flash programming algorithms until the PGMSEC command is fully supported. Do not use the EzPort module until PGMSEC is fully supported.

e2590: FMC: Master Access Protection encoding for write only access does not work as specified.

Errata type: Errata

Description: The Access Protection Register (FMC_PFAPR) in the Flash Memory Controller provides write and/or read access control to the FlexRAM space on a per master granularity.

The eight two bit Master Access Protection fields in the FMC_PFAPR are encoded as follows:

00 - No access may be performed by this master

01 - Read only accesses may be performed by this master

10 - Write only accesses may be performed by this master

11 - Read and Write accesses may be performed by this master

The "10" encoding (write only accesses) does not work as specified. This encoding blocks all accesses.

So, the "10" encoding functions the same as the "00" encoding. Due to this error, it is not possible to designate the FMC memory space as "write only" for any master.

Note that the only writable portion of the FMC memory space is the FlexRAM space.

Workaround: The "11" encoding, allowing read and write accesses, must be programmed to allow writes for a given master.

e2592: FTFL: EEESPLIT feature not fully implemented

Errata type: Errata
Description: EEESPLIT feature not fully implemented within the firmware. Only the EEESPLIT = '11' case is supported.

Workaround: Use only the EEESPLIT = '11' case for a 50%/50% split of the FlexRAM for EEPROM.

e2781: FlexBus: False bus error on back-to-back writes when flash memory is secure

Errata type: Errata
Description: During back-to-back writes, the FlexBus incorrectly responds with a bus error on the second write when both of these conditions apply: the flash memory is secure (per the value of the FTFL module's FSEC[SEC] field), and the SIM's SOPT2[FBSL] field is 10b. This setting of the SOPT2[FBSL] field disallows instruction accesses but allows data accesses on the FlexBus interface when the flash memory is secure.

Workaround: When the flash memory is secure and FlexBus instruction accesses are inhibited but data accesses are allowed, do not use back-to-back writes. Insert a delay or NOP instruction between the write operations.

e2616: FlexCAN: Module receives data frames sent by itself although the self reception feature is disabled

Errata type: Errata
Description: The FlexCAN receives frames transmitted by itself although the self reception feature is disabled (MCR[SRX_DIS] is asserted). As a result, the transmitted data is moved into Mailbox and the IFLAG is asserted.

The error occurs when there is at least one reception Mailbox whose ID matches a frame that is being transmitted and the FlexCAN requests Freeze mode during the frame transmission.

The occurrence of this error depends on the software strategy used to request Freeze Mode and how often Freeze Mode is requested during module operation.

Workaround: If the self reception feature is disabled (MCR[SRX_DIS] = 1), in order to avoid receiving a self transmitted frame, Freeze Mode should only be requested when all Mailboxes that are configured as TX have been transmitted or aborted.

e3402: GPIO: XTAL pin cannot be used as GPIO if the ERCLKEN bit is set.

Errata type: Errata

Description: XTAL pin cannot be used as GPIO if the ERCLKEN bit is set. Errata applies only when an external clock is being used (the crystal oscillator is not being used) and OSC_CR[ERCLKEN] bit set to 1. In this specific case, the analog block of the crystal oscillator is enabled and the oscillator output is driving the XTAL pin even if the respective pin control register has been configured as a GPIO. This prevents the pin from being used as either an input or an ouput.

Workaround: If an external clock is not being used, then the OSCERCLK is not available and there is no need to set the ERCLKEN bit. If the ERCLKEN bit is not set then the XTAL pin can be used as a GPIO.

If an external clock is being used but the OSCERCLK is not required, then the ERCLKEN bit should not be set and the XTAL pin can be used as a GPIO.

If an external clock is being used and the OSCERCLK is required and the ERCLKEN bit is set, then there is no workaround and the XTAL pin cannot be used as a GPIO.

e2793: I2C: Module limitation for MCU wakeup

Errata type: Errata
Description: The I2C module's asynchronous wakeup has a limitation: it cannot wake the MCU from stop mode via an interrupt.

Workaround: When the MCU is in stop mode, ensure that the external I2C master sends data to wake the MCU before it sends any transaction to other I2C slaves.

e2674: LLWU: The LLWU glitch filter for pin and reset is not supported

Errata type: Errata
Description: LLWU glitch filter for pin and reset is not supported. Do not enable the filters. Writing a 1 to FLTEP or FLTR bits in the LLWU_CS register will result in abnormal LLWU behavior.

Workaround: It is recommended that the glitch filter functionality is not used. Always write a zero to the FLTEP or FLTR bits in the LLWU_CS register. If filtering is required, external components or software filters are required.

e2678: MC: The MC_SRS[PIN] is not always set after exiting a VLLS mode due to a RESET pin assertion

Errata type: Errata
Description: When waking the device from VLLS low power modes via a RESET pin, the MC_SRSL[PIN] bit is not reliably set on recovery and cannot be used to differentiate VLLS wakeup from the RESET pin from other low power mode wakeup sources enabled in the LLWU module. This condition is encountered when the device is in a VLLS low power mode and the RESET pin is held asserted for greater than 100us to initiate a VLLS wakeup.

Workaround: When using the RESET pin as a wakeup trigger for exit from VLLS, ensure that the wakeup pulse is short in duration (<100us).

An alternate workaround is to only use the MC_SRS[WAKEUP] bit to indicate VLLS exit recoveries and reset initialization routines to not distinguish between RESET pin triggered recoveries and other sources of VLLS wakeup.

e2676: MC: When waking the system from VLLS modes via a RESET pin, the I/O are not immediately released to their reset state.

Errata type: Errata
Description: When waking the system from VLLS modes via a RESET pin, the I/O are not immediately released to their reset state.

Workaround: The reset initialization/recovery software must set the LLWU_CS[ACKISO] bit just as it would due to a low power wakeup via any of the other low power mode wakeup sources.

e3580: MCG: Total deviation of trimmed average DCO output frequency over voltage and temperature does not meet specification.

Errata type: Errata
Description: The total deviation of the trimmed average DCO output frequency over voltage and temperature does not meet specifications outlined in the Datasheet when using the internal reference (slow clock) as the reference to the FLL (FEI clock mode).

Workaround: For higher accuracy, it is recommended that the user utilize an External Reference Clock. The RTC Oscillator or the System Oscillator with external crystal should be used as a reference to the FLL in order to clock the system in FEE or FBE modes. Additionally, the PLL can also be used with MHz external clock, bypassing the FLL in PEE or PBE modes.

e2798: PMC: STOP and VLPS mode currents are higher than specified.

Errata type: Errata
Description: STOP and VLPS mode currents are higher than targets specified in the datasheet.

Workaround: Users should account for the higher current draw in their prototype evaluation. Refer to the datasheet for production target values.

e2706: PMC: VLLS3 and VLLS2 recovery time is longer than specified

Errata type: Errata
Description: The VLLS3 and VLLS2 recovery time is expected to be a maximum of 49 us as outlined in the data sheet. However, the recovery time is approximately 75 us.

Workaround: Use another low power stop mode with faster recovery time.

e2542: PMC: Very Low Power Run (VLPR) and Very Low Power Wait (VLPW) power modes are not supported

Errata type: Errata
Description: Very Low Power Run (VLPR) and Very Low Power Wait (VLPW) power modes are not supported.

Workaround: Do not use the part in these two power modes.

e2576: RTC: When the RTC is configured to allow supervisor access only, the write and read access registers can be modified in user mode

Errata type: Errata

Description: When the RTC is configured to allow supervisor access only, the write and read access registers can be modified in user mode. A bus error is still generated.

Workaround: RTC supervisor mode access only option is not supported.

e2591: TSI: TSI_SCANC[SMOD] behaves as an inactive time instead of a scan period value

Errata type: Errata

Description: TSI_SCANC[SMOD] should configure the scanning interval. TSI_SCANC[SMOD] interacts with the TSI_SCANC[AMCLKS] prescaler to configure this interval: Reference clock -> AMCLKS -> SMOD. So the interval frequency should be: Reference clock / AMCLKS prescaler / SMOD. However, it is working as an inactive time. Therefore, when an SMOD value is configured, the TSI will scan all the enabled electrodes and then be inactive for as much time as the SMOD and AMCLKS registers are configured.

Workaround: TSI_SCANC[SMOD] is designed to provide a predictable and configurable scanning interval. Depending on the scenario, there are three possible workarounds:

1. When SMOD = 0, the TSI will continuously scan without a pause between scans. This scan time is dependent on the electrode capacitance value and the current configured for the electrode. If the application will use only the out-of-range interrupt and it is not necessary to continually log each measured value after each scan, then an adequate threshold configuration and SMOD = 0 will cause the TSI to only interrupt or enable the out-of-range flag whenever there is a touch detected.

2. Manually control scanning time: use a time base to trigger single scans with the TSI_GENCS[SWTS] bit with the desired period. This workaround is recommended when a stable, predictable scan period is desired.

3. Use SMOD as a complement to the scanning time. The scanning time depends on the capacitance of the external electrodes. As mentioned above, the SMOD will currently control how much time the TSI is inactive after a scan so assumming the normal scan and the inactive time SMOD is currently determining will give a variable scanning period. If the application doesn't require an exact scanning period, this mode is recommended because adding inactive time after each scan will save power between scans.

e2638: TSI: The counter registers are not immediately updated after the EOSF bit is set.

Errata type: Errata

Description: The counter registers are not immediately updated after the end of scan event (EOSF is set). The counter registers will become available approximately 0.25 ms after the EOSF flag is set. This also applies for the end-of-scan interrupt, as it is triggered with the EOSF flag. This behavior will occur both in continuous scan and in software triggered scan modes.

Workaround: When detecting an end of scan, include a delay that will take at least 0.25 ms. This delay does not need to be a blocking delay, so it can be executing other actions before reading the counter registers.

Notice that the out-of-range flag (OUTRGF) and interrupt occur after the counters have been updated, so in the case of polling the OUTRGF flag or using the out-of-range interrupt, the workaround is not needed.

e2582: UART: Flow control timing issue can result in loss of characters

Errata type: Errata

Description: When /RTS flow control signal is used in receiver request-to-send mode, the /RTS signal is negated if the number of characters in the RxFIFO is equal to or greater than the receive watermark. The /RTS signal will not negate until after the last character (the one that makes the condition for /RTS negation true) is completely received and recognized. This creates a delay between the end of the STOP bit and the negation of the /RTS signal. In some cases this delay can be long enough that a transmitter will start transmission of another character before it has a chance to recognize the negation of the /RTS signal (the /CTS input to the transmitter).

Workaround: UART0 and UART1 that implement an eight entry FIFO. When the FIFO is enabled, the receive watermark should be set to seven or less. This will ensure that there is space for at least one more character in the FIFO when /RTS negates. So in this case no data would be lost.

When using one of the UARTs without a FIFO (or UART0 or UART1 with the FIFO disabled), delay might need to be added between characters on the transmit side in order to allow time for the negation of /RTS to be recognized before the next character is sent.

e2584: UART: Possible conflicts between UART interrupt service routines and DMA requests

Errata type: Errata

Description: If the UARTn_S1[RDRF] and/or UARTn_S1[TDRE] flags are being used to generate DMA requests, there is a possible conflict that could occur if an interrupt service routine (ISR) or other code is used to clear any of the other flags in the UARTn_S1 register. The flags in the UARTn_S1 register use a side effect clearing mechanism where the procedure is to read the status register and then perform a read or write of the data register to clear the flag. If a DMA request for a flag bit is asserted while an ISR for another flag bit is executing, then in the process of clearing the ISR's flag bit, the ISR can also clear the flag bit for the DMA request, thereby negating the DMA request before the DMA responds to it. This could potentially cause servicing of the DMA event to be missed.

For example, assume a DMA request is being asserted for the RDRF flag. At the same time, the parity error flag (PF) sets and triggers an ISR. To clear the PF flag bit, the ISR must read the status register and read the data register. In the process, the RDRF flag would also be cleared, causing the DMA request to negate. If the DMA request asserts after the DMA has already prepared its next transfer, then it might still read from the data register, potentially causing an underflow.

Workaround: When possible, avoid enabling the UART for DMA requests and interrupts simultaneously. If error interrupts are needed while DMA requests are active, then the error ISR can be used to abort the current DMA transfer (by disabling the DMA request inside the UART and/or disabling the external request for the DMA channel) before clearing any error flags in the UARTn_S1 register.

e2686: WDOG: A watchdog reset while the system is in STOP or VLPS modes causes an incorrect wakeup sequence

Errata type: Errata

Description: A watchdog reset while the system is in STOP or VLPS modes causes an incorrect wakeup sequence

Workaround: The watchdog should not be configured to continue operation when the system has entered STOP or VLPS.

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