Mask Set Errata for Mask 0N38J

Introduction

This report applies to mask 0N38J for these products:

- S08PA4

Errata ID	Errata Title
6657	ADC: ADC FIFO not working when the bus clock is slower than ADC clock divided by two
5264	DBG: Comparator C with TAG type cannot generate breakpoint when setting breakpoint at the address other than instruction opcode address
7331	IO: High current drive pins not in high-Z state during power up
7040	SOC: Slow VDD ramp-up might cause unstable startup on some devices during power up at cold temperatures

e6657: ADC: ADC FIFO not working when the bus clock is slower than ADC clock divided by 2

Errata type: Errata

Description: When the ADC FIFO mode is enabled, the FIFO can not get correct result if the bus clock is slower than ADC conversion clock divided by 2.

Workaround: Configure the bus clock to be faster than the ADC conversion clock (ADCK) divided by 2 if the ADC FIFO is used.

e5264: DBG: Comparator C with TAG type can not generate breakpoint when setting breakpoint at the address other than instruction opcode address

Errata type: Errata

Description: When setting breakpoint at the address other than instruction opcode address, the comparator C with TAG type can not generate breakpoint. This issue does not affect code execution.

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Workaround: If such tag breakpoint at the address other than instruction opcode address is required, use comparator A and/or B tag breakpoint.

e7331: IO: High current drive pins not in high-Z state during power up

Errata type: Errata
Description: The high current drive pins on the chip are unexpectedly driven low for a short period during power up. All other I/O pins are high impedance. The issue happens only before VDD reaches the power-on reset voltage. After power up the normal I/O functions on the high current drive pins are not impacted.

Workaround: Use one or more combination of the following methods to avoid possible issues:

- Use high current drive pins as current source for LED connection, but keep total IDD < 120mA (refer to device data sheet for IDD)
- Configure the corresponding Flextimer channel output polarity as active high which are muxed with high current drive pins
- Use high current drive pins with NPN transistor (active high) to drive relays
- Keep VDD ramp-up time greater than or equal to 1KV/s and less than or equal to 10KVs to disable LED and/or driver action during power up

e7040: SOC: Slow VDD ramp-up might cause unstable startup on some devices during power up at cold temperatures

Errata type: Errata
Description: Some devices may not start up when both conditions are met: cold temperature (between -40°C and about -20°C) and slow VDD ramp up time (less than or equal to 900 V/s). The unstable startup is occasional and recoverable after an uncertain period of time.

Workaround: In order to avoid such startup issue either of these conditions shall be met:

- Temperature above -20°C;
- VDD ramp up time >=1K V/s and <= 10K V/s

This erratum will be fixed in the next revision.

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