Mask Set Errata for Mask 0N53H

This report applies to mask 0N53H for these products:

- S08PT60 S08PA60 S08PT32 S08PA32

Errata ID	Errata Title
6657	ADC: ADC FIFO not working when the bus clock is slower than ADC clock divided by 2
5264	DBG: Comparator C with TAG type can not generate breakpoint when setting breakpoint at the address other than instruction opcode address
6245	NVM: flash protection issue affecting program flash command
7331	IO: High current drive pins not in high-Z state during power up
7891	Port: both PTB6 and PTB7 pins can not function as open-drain when configured as IIC function
7040	SOC: Slow VDD ramp-up might cause unstable startup on some devices during power up at cold temperatures

e6657: ADC: ADC FIFO not working when the bus clock is slower than ADC clock divided by 2

Errata type: Errata
Description: When the ADC FIFO mode is enabled, the FIFO can not get correct result if the bus clock is slower than ADC conversion clock divided by 2.

Workaround: Configure the bus clock to be faster than the ADC conversion clock (ADCK) divided by 2 if the ADC FIFO is used.

e5264: DBG: Comparator C with TAG type can not generate breakpoint when setting breakpoint at the address other than instruction opcode address

Errata type: Errata
Description: When setting breakpoint at the address other than instruction opcode address, the comparator C with TAG type can not generate breakpoint. This issue does not affect code execution.

Workaround: If such tag breakpoint at the address other than instruction opcode address is required, use comparator A and/or B tag breakpoint.

e6245: NVM: flash protection issue affecting program flash command

Errata type: Errata

Description: There is a problem affecting program flash command in a scenario where the flash is partially protected.

When program flash command is used to program 8-bytes, starting from the address that corresponds to the last 4-bytes in the flash unprotected region (therefore crossing the boundary into the protected region), the program flash command will program the full set of 8 bytes: 4 bytes in the unprotected region and the next 4 bytes in the protected region, what results in an undetected protection violation.

Workaround: The application should launch program flash command to program 4-bytes or 8-bytes to correctly match the limits of the flash unprotected region, not forcing the transition from the unprotected to the protected region as explained above.

e7331: IO: High current drive pins not in high-Z state during power up

Errata type: Errata

Description: The high current drive pins on the chip are unexpectedly driven low for a short period during power up. All other I/O pins are high impedance. The issue happens only before VDD reaches the power-on reset voltage. After power up the normal I/O functions on the high current drive pins are not impacted.

Workaround: Use one or more combination of the following methods to avoid possible issues:

- Use high current drive pins as current source for LED connection, but keep total IDD < 120mA (refer to device data sheet for IDD)
- Configure the corresponding Flextimer channel output polarity as active high which are muxed with high current drive pins
- Use high current drive pins with NPN transistor (active high) to drive relays
- Keep VDD ramp-up time greater than or equal to 1KV/s and less than or equal to 10KVs to disable LED and/or driver action during power up

e7891: Port: both PTB6 and PTB7 pins can not function as open-drain when configured as IIC function

Errata type: Errata

Description: When configured as the IIC function, the PTB6 and PTB7 pins cannot operate as open-drain pins. These pins actively drive high and low, similar to normal GPIO pins. As a result, when another device on the IIC bus drives low, there will be high current to this device when the corresponding pin of PTB6 and/or PTB7 drives high.

Workaround: Use the true open-drain PTA2 and PTA3 pins for the IIC SDA and SCL functions. Do not use PTB6 and PTB7 as IIC function pins. This issue will be fixed on future silicon revisions.

e7040: SOC: Slow VDD ramp-up might cause unstable startup on some devices during power up at cold temperatures

Errata type: Errata

Description: Some devices may not start up as expected when both conditions are met: cold temperature (typically between -40°C and -10°C) and slow VDD ramp up time (typically between 500V/s to 900 V/s). The unstable startup is occasional and recoverable after an uncertain period of time. That is, some devices may start up after several hundreds of microseconds, while others may take several minutes to start up and the same device may start up as expected after several power cycles.

Workaround: Try to meet all the following conditions to reduce the possibility of this issue:

- Temperature above -10°C;
- VDD ramp up time: 13 V/s to 400 V/s, 1K V/s to 10K V/s

This erratum will be fixed in the next revision.

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Document Number: S08PT60_0N53H
Rev. 03 SEP 2014