# MSC8156 High-Performance Multicore DSP

## Six-core programmable DSP for medical imaging, aerospace, defense and advanced test and measurement

**Overview**

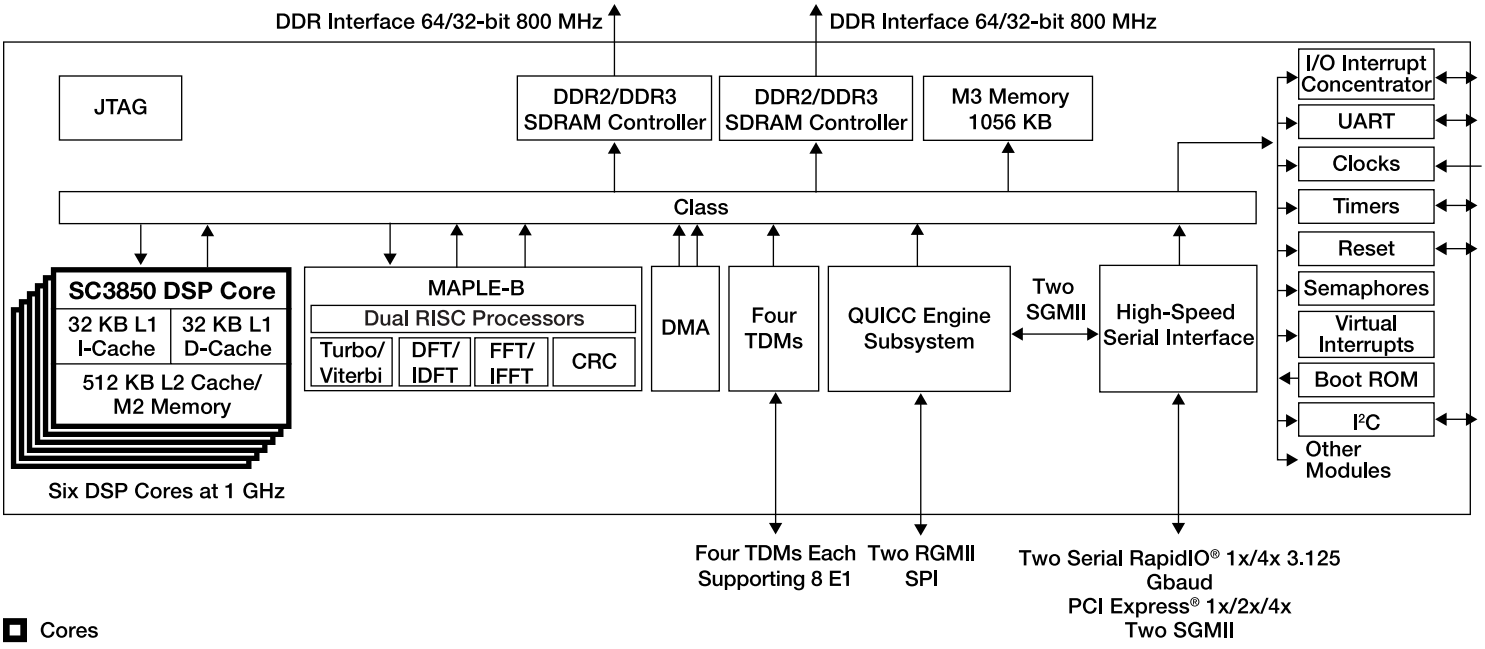
The MSC8156 is based on the industry's highest performance DSP core, built on StarCore technology, with added performance from a multi-accelerator platform engine (MAPLE-B) for fast Fourier transforms (FFT), inverse fast Fourier transforms (iFFT), discrete Fourier transforms (DFT), inverse discrete Fourier transforms (iDFT) and Turbo and Viterbi decoding. The MSC8156 supports the advanced processing requirements and capabilities of today's high-performance medical, aerospace and defense and advanced test and measurement markets. It delivers industry-leading performance and power savings, leveraging 45 nm process technology in a highly integrated SoC to provide performance equivalent to a 6 GHz, single-core device. The MSC8156 will help equipment manufacturers create end products and services that integrate more functionality in a smaller hardware footprint.

The MSC8156 DSP delivers a high level of performance and integration, combining six new and enhanced, fully programmable SC3850 cores, each running at up to 1 GHz. The SC3850 DSP core has been independently assessed to enable 40 percent more processing capability per MHz than the nearest DSP competition. A high-performance internal RISC-based QUICC Engine subsystem supports multiple networking protocols to guarantee reliable data transport over packet networks while significantly offloading processing from the DSP cores.

The MSC8156 embeds a substantial amount of internal memory to support a variety of advanced high-speed interface types, including two Serial RapidIO® interfaces, two Gigabit Ethernet interfaces for network communications, a PCI Express® interface, two DDR controllers for high-speed, industry standard memory interface and four multi-channel TDM interfaces.

The MSC8156 allows a high degree of scalability through pin compatibility with all MSC825x and MSC815x DSP devices.

### MSC8156 Block Diagram



## Features and Benefits

- Six StarCore DSP SC3850 core subsystems operating at up to 1 GHz/8000 MMACS per core and up to 48000 MMACS per device
- Multi-accelerator platform engine for baseband (MAPLE-B)
  - Highly flexible, programmable Turbo and Viterbi decoder supports configurable decoding parameters. It can perform up to 200 Mbps of Turbo decoding (6 iterations) or up to 115 Mbps of K = 9 (zero tail) Viterbi decoding
  - FFT/iFFT for sizes 128, 256, 512, 1024 or 2048 points at up to 350 million samples per second
  - DFT/iDFT for sizes up to 1536 points at up to 175 million samples per second
- Two master buses for data transfers from/to the system memory at total throughput up to 50 Gbps
- High-speed, high-bandwidth CLASS fabric arbitrates between the DSP cores and other CLASS masters to M2 memory, M3 memory, DDR controllers and the configuration registers
- Two DDR controllers with up to 400 MHz clock (800 MHz data) rate and 32/64-bit DDR2/3 SDRAM data bus. Supports SODIMMs and up to 2 GB per controller
- 32-channel DMA controller
- Dual RISC core QUICC Engine subsystem operating at up to 500 MHz provides parallel packet processing independent of the DSP cores
  Supports:
  - Two Gigabit Ethernet controllers supporting RGMII or SGMII
  - Serial peripheral interface
- HSSI that supports two x4 SerDes ports, including:
  - Two Serial RapidIO interfaces supporting x1/x4 operation up to 3.125 Gbaud
  - One PCI Express interface that supports x1/x2/x4 operation
  - Multiplexing capability for RapidIO, PCI Express and SGMII signals through the two SerDes ports
- Four TDM interfaces
- UART and $I^2C$ interfaces
- Eight software watchdog timers
- Sixteen 16-bit timers
- Two 32-bit general purpose timers per core for RTOS support
- I/O interrupt concentrator and virtual interrupt support
- Eight hardware semaphores
- 32 GPIO ports multiplexed with interface signals and IRQ inputs
- Boot options: Ethernet, Serial RapidIO, $I^2C$ and SPI
- Three input clocks and five PLLs
- JTAG Test Access Port (TAP) and boundary scan architecture designed to comply with IEEE 1149.1™ standard for profiling and performance monitoring support
- Reduced power dissipation with wait, stop and power down low-power standby modes
- Optimized power management circuitry
- Technology: CMOS 45 nm SOI technology in 29 mm x 29 mm, 783 ball, FC-PBGA package

## Development Support

Freescale supplies a complete set of CodeWarrior DSP development tools for the MSC8156 device. The tools provide easier, more robust ways for designers to develop optimized DSP and gives designers everything they need to exploit the advanced capabilities of the MSC8156 architecture.

Support tools include:

- Eclipse-based integrated development environment (IDE)
- C and C++ compiler with in-line assembly
- Librarian
- Multicore debugger
- Royalty-free RTOS
- Software simulator
- Profiler
- High-speed run control
- Host platform support
- MSC8156ADS development board
- MSC8156EVM evaluation module

Contact your local sales office or representative for availability.


**Learn More:** For current information about Freescale products and documentation, please visit **freescale.com/DSP**.



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