Freescale Semiconductor
Product Brief

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MPC5121e Product Brief

The MPC5121e integrated processor provides an exceptional computing platform for multimedia and infotainment vehicle applications for both OEM, aftermarket, as well as commercial and industrial products. The MPC5121e is also excellent for any embedded solution that requires graphics, a graphical user-interface, and network connectivity. The MPC5121e has automotive qualification; therefore, all customers can expect competitive cost, quality, reliability, and availability for years to come. The MPC5121e uses the e300 CPU core based on the Power Architecture Technology.

The MPC5121e has an integrated graphics engine, the PowerVR® MBX Lite IP core designed by Imagination Technologies, which supports 3D acceleration. With a 128-bit interface, this graphics engine has incredible performance. A separate 32-bit RISC audio acceleration engine (AXE) provides acceleration of popular media formats including MP3, AAC, WMA, AMR, Ogg Vorbis, and others. The audio acceleration engine can

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also support sample rate conversion important to speech recognition.

The MPC5121e integrated processor includes multiple cores and multiple buses, helping to avoid high clock rates to obtain high performance. The excellent balance between operating power consumption and performance allows for lower system cost and higher reliability. The low standby power consumption also makes the product suitable for portable applications.

The flexibility of the MPC5121e provides customers a platform for a variety of product applications. Its rich set of integrated I/O includes PCI, SATA, PATA, Ethernet, USB 2.0, CAN, twelve programmable serial controllers, and numerous others. The integrated display controller (DIU) allows for cost-effective support of thin film transistor (TFT) LCD panel displays with up to 1280 x 720 resolution.

Again, the MPC5121e uses the e300 CPU core, with 32-Kbyte instruction cache and 32-Kbyte data cache, based on the Power Architecture. Wide support of RTOS, software drivers, middleware, and application solutions from mobileGT alliance members is already in progress. This can greatly reduce development lead times and expense while improving software quality. The MPC5121e is designed for application code compatibility with current solutions on the MPC5200 and for easy scalability across product solutions. The MPC5121e is also fully pin compatible and software compatible with the MPC5123, for applications where a 3D graphics engine is not required.

The many embedded memory buffers help ensure balanced system performance and system bus throughput. The performance of the MPC5121e is enhanced by having well-balanced system resources for the integrated core, graphics and audio engines, as well as the DDR1 and DDR2 memory controllers with integrated 64-channel DMA support.

1 Application Examples

1.1 Automotive Infotainment and Navigation System

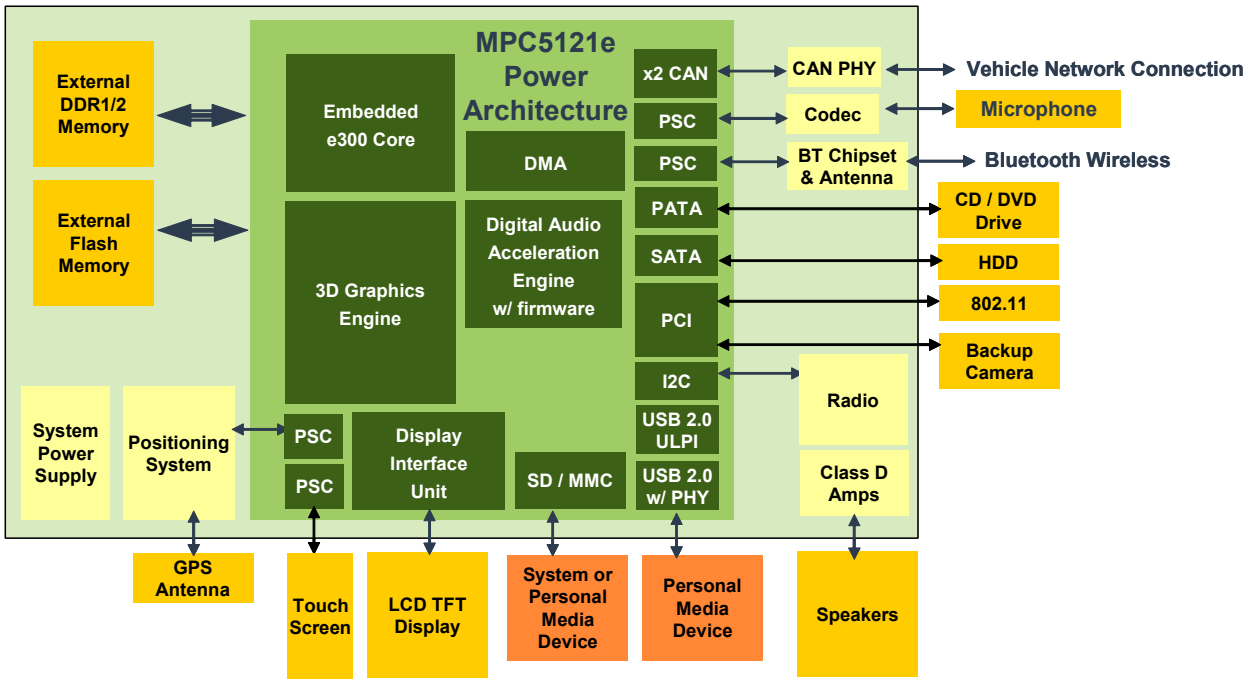

Figure 1. Automotive Infotainment and Navigation System

The highly-integrated features of the MPC5121e are optimal for systems such as automotive center stacks where an LCD display is desired for driver interface-to-vehicle systems. These systems include HVAC, audio, CD, DVD, HDD, navigation, and video for backup cameras. Systems may also include personal media devices (PMDs), speech recognition, text-to-speech, and various wireless connections like 802.11, Bluetooth, and cellular. The MPC5121e is also appropriate for networked display modules used in the rear seating area.

1.2 Building Automation and Security System

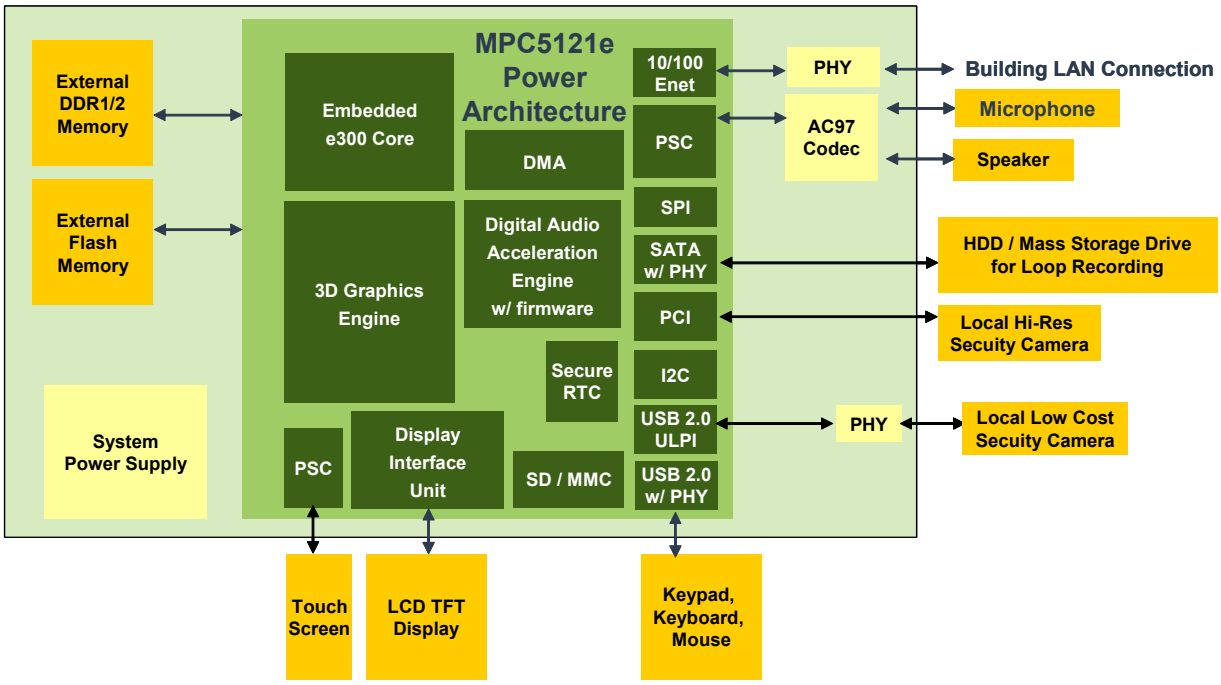

Figure 2. Building Automation and Security System

The MPC5121e is well-suited for industrial applications such as advanced security systems, particularly where an LCD display is desired for user interface and live monitoring. These systems usually involve networked cameras and may also include video and audio recording, biometric identification, radio frequency identification (RFID), monitoring, face or voice recognition, barcode or card swipe readers, and associated control of networked building functions (such as access, lighting, and air conditioning). These systems may also include secure, remote and web-based monitoring, wireless connectivity, and emergency services notification.

2 Features

The MPC5121e features an e300 Power Architecture compliant processor core that is a dual-issue, superscalar architecture. With 32-Kbyte instruction cache and 32-Kbyte data cache, a double-precision FPU, and instruction and data MMU, this is one of the most powerful processors designed for automotive applications.

The MPC5121e architecture is built around an arbitrated multi-master memory bus architecture with an integrated DDR1/DDR2 memory controller. The processor bus supports pipelined split transaction bus tenures to maximize performance. There are also several peripheral buses with widths and speeds matched to the requirements of each domain. With associated, distributed buffer memories, core interrupts and bus transfer overheads are reduced for improved system performance.

The MBX Lite 2D/3D graphics engine was licensed from Imagination Technologies Group Plc. and includes PowerVR geometry processing acceleration. The PowerVR MBX Lite's unique tile-based rendering architecture provides powerful, efficient performance and is implemented with a 128-bit interface to optimize byte transfers on the memory interface.

The AXE audio engine is a programmable 32-bit fixed-point RISC engine intended for hardware acceleration of digital audio formats, for encoding or decoding, but also supports other functions like sample rate conversion. It operates at 200 MHz and has eight registers each for data address and vector. The engine has a single-cycle 32 × 32 multiply-accumulate block. The single-channel DMA supports up to four pipelined transfers handling in excess of 500 MByte/sec. This is supported by a zero-wait 128-Kbyte SRAM bank. The engine also supports sleep mode, interrupts, and hardware debugging.

The DIU integrated display controller can support a wide variety of TFT LCD displays with resolution up to 1280 × 720 (720p) at a maximum refresh rate of 60 Hz and a color depth up to 24 bits per pixel. There are three input planes and output planes, but the output planes can be extended by write-back and blending to virtual n-plane output. Alpha blending can extend up to 256 levels, and chroma keying is selectable by range.

2.1 Block Diagram

Figure 3 shows a top-level block diagram of the MPC5121e.

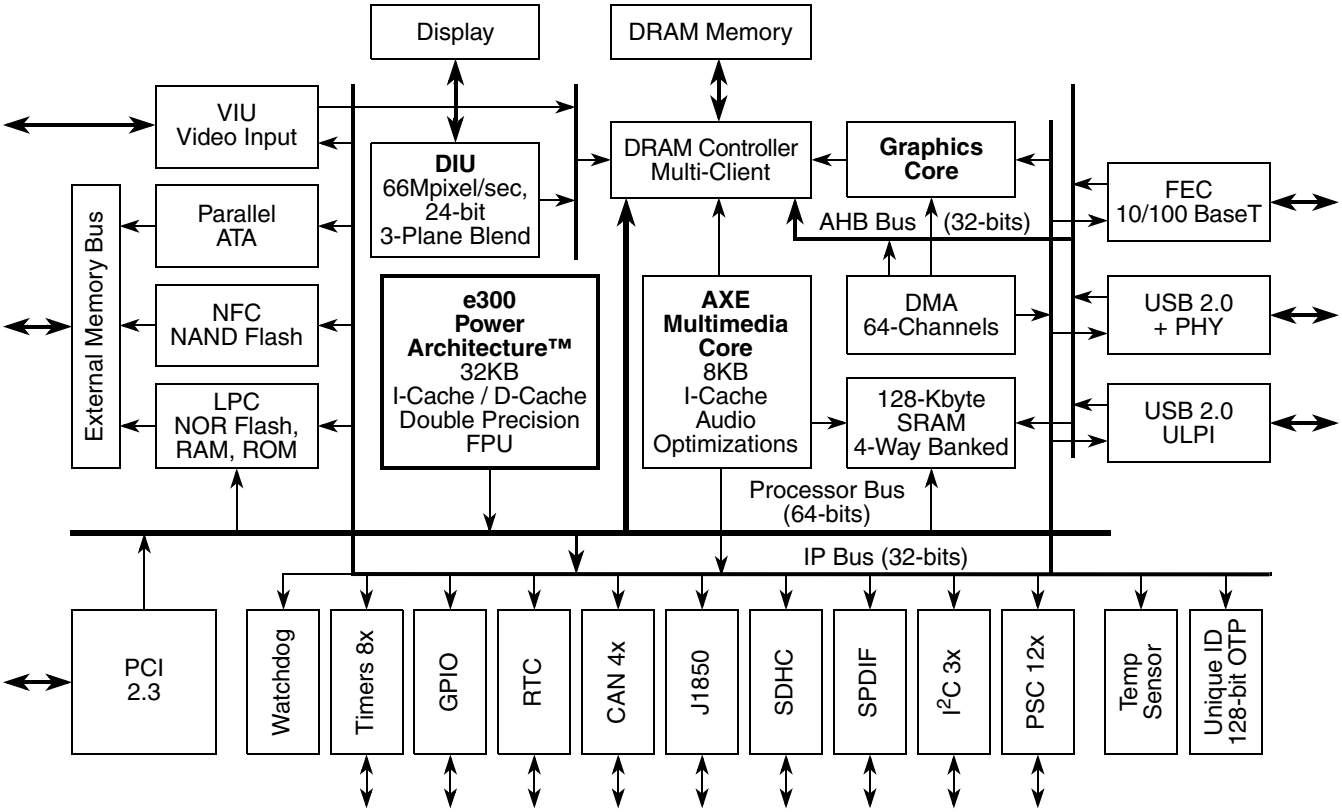

Figure 3. Multi-Core MPC5121e Block Diagram

2.2 Critical Performance Parameters

The following describes critical operating parameters of the MPC5121e:

- 1.4 V internal, 3.3 V external operation (2.5 V for DDR1 interface, 1.8 V for DDR2 interface)
- TTL-compatible I/O pins
- Full-performance extended temperature range (-40°C to +85°C ambient temperature T_A)
- High reliability, automotive grade, plastic ball grid array packaging:
  — 516-pin TEPBGA, 27 × 27 mm body, 1.0 mm ball pitch

2.3 Chip-Level Features

Major features of the MPC5121e are:

- e300 Power Architecture processor core (enhanced version of the MPC603e core), operates up to 350–400 MHz
- Power modes include doze, nap, sleep, deep sleep, and hibernate

- Auxillary execution engine (AXE) – Programmable auxillary execution engine, suitable for multi-standard audio applications
- MBX Lite – 2D/3D graphics engine with PowerVR vector processing
- DIU – Display interface unit
- DDR1, DDR2, and low-power mobile DDR (LPDDR) SDRAM memory controllers
- USB 2.0 OTG controller with integrated physical layer (PHY)
- DMA subsystem
- EMB – Flexible multi-function external memory bus interface
- NFC – NAND flash controller
- 10/100Base Ethernet
- PCI interface, version 2.3
- PATA – Parallel ATA integrated development environment (IDE) controller
- SATA – Serial ATA controller with integrated physical layer (PHY)
- SDHC – MMC/SD/SDIO card host controller
- PSC – Programmable serial controller
- S/PDIF – Serial audio interface
- CAN – Controller area network

2.4 Module Features

The following provides more details of modules implemented on the device:

- e300 processor core using the PowerPC instruction set
  - 32-Kbyte instruction cache and 32-Kbyte data cache
  - Instruction and data MMU
  - High-performance, superscalar processor core with a four-stage pipeline
  - Dual-issue processor with integrated double-precision, floating-point unit
  - Dynamic power management
- MBX Lite graphics block
  - Dedicated hardware graphics coprocessor
  - Superior 2D and 3D graphics performance
  - Supports OpenVG 1.0, OpenGL-ES 1.1
- Display interface unit
  - Supports LCD display resolution up to 1280 × 720 or 1024 x 768
  - Supports refresh rate up to 60 Hz
  - Color depth up to 24 bits per pixel
  - Hardware n-plane accelerated blending
- Auxillary execution engine (AXE)
  - Onboard, programmable 32-bit RISC coprocessor

  - Specialized instruction set and hardware for 32-bit audio applications
  - 8-Kbyte instruction cache, 48-bit fixed point arithmetic, and multiply-accumulate (MAC)
  - Supports up to 4x MP3 encode speed
  - Software available for many audio decode formats like MP3, AAC, Ogg Vorbis, AMR, and WMA
- Two USB controllers
  - Two on-chip USB controllers with On-The-Go host/device capability
  - Each supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps)
  - One USB controller with an integrated on-chip physical interface (PHY)
  - Both USB controllers can be accessed through the ULPI interface
- DMA
  - 64-channel, 32-bit data path width on-chip DMA engine with advanced capabilities
  - Flexible protocol programmability
- Multi-port DRAM controller
  - Five ports
  - Supports 16-bit wide and 32-bit wide DDR1, DDR2, and LPDDR SDRAM devices at up to 200 MHz
  - DRAM interface optimized for low EMI
- 128 Kbyte on-chip SRAM
  - 0-wait state memory for AXE audio processor
  - Usable as e300 core scratch pad memory
- PCI host controller
  - PCI specification revision 2.3 compliant
  - 32-bit PCI interface support on primary PCI port
  - On-chip arbitration supports three external PCI bus masters
- Serial ATA controller with integrated PHY
  - Compliant with serial ATA 1.0a spec
  - Supports 1.5 Gbps
- Parallel ATA controller
  - Compliant with ATA-6 specification
  - Supports PIO mode 0 to 4
  - Supports MDMA mode 0 to 2
  - Supports UDMA mode 0 to 4
- Ethernet controller
  - Supports 100 Mbps/10 Mbps IEEE 802.3 MII
  - Supports 10 Mbps 7-wire interface
  - IEEE 802.3 full duplex flow control
- NAND flash controller

  - Supports 8-bit-wide and 16-bit-wide NAND Flashes
  - Supports booting from NAND Flash
  - Supports 2 Kbyte block NAND devices
  - Supports dual chip selects
  - One-bit correction, two-bit detection capability
- LocalPlus interface
  - Interface to external memory-mapped or chip-selected devices
  - 32-bit address bus
  - 32-bit data bus
  - Eight chip selects
  - Supports burst mode flash
  - Supports 32-bit ALE-muxed interface
  - Supports up to 42-bit non-muxed interfaces
  - Supports large-packet DMA transfers
- Secure digitial host controller (SDHC)
  - Supports multimedia, secure digital (SD) memory cards, and I/O cards
  - Supports up to MMC card specification V. 4.0
  - Supports SDIO standard and SD physical layer spec with 1/4 channel(s)
- Four controller area network (CAN) interfaces
  - Implementation of CAN protocol, version 2.0 A/B
  - Programmable wakeup functionality
  - Both support low-speed or high-speed
- S/PDIF receive and transmit interface
  - Single channel receiver/transmitter
  - S/PDIF receiver operates with incoming frequencies in 32 kHz to 96 kHz range
- Three inter-integrated circuit communication (I^2C) interfaces
  - Multi-Master operation, master/slave modes supported
  - Input digital noise filtering
  - Software programmable for various serial clock frequencies
- Twelve programmable serial controllers
  - Each PSC is a flexible serial communication engine, supporting the following protocols:
    - UART
    - Codec/PCM
    - I^2S
    - SPI
    - AC97
  - Each PSC is serviced by a centralized FIFO to provide buffer storage

  - PSC UART mode
    - Full-duplex asynchronous receiver/transmitter channel
    - Programmable data format
  - PSC Codec mode
    - Programmable 8, 12, 16, 20, 24, or 32-bit data length for soft modem support
    - Master and slave clock support
    - Supports SPI and I^2S interface
    - Programmable data shift direction (msb or lsb first)
  - PSC SPI mode
    - Programmable 8, 12, 16, 20, 24, or 32-bit data length
    - Programmable clock polarity and clock phase
  - PSC AC97 mode
    - Supports AC97 controller functionality; bit clock must be provided by an external codec
    - Supports wake-up and power-down modes
- Video input
  - ITU-656 compliant
- Frequency measurement block
  - 4-channel frequency measurement of externally received slave clocks
- J1850 interface (BDLC)
  - SAE J1850 Class B data communications network interface compliant
  - ISO-compatible for low-speed (< 125 Kbps) serial data communications
  - Digital noise filter
- General purpose I/O
- On-chip real-time clock
  - Secure low-power timebase
  - Tamper bit indicates when Vbat has been removed
  - Programmable alarm
  - Periodic interrupts for one second, one minute, one day
  - Calendar support
- On-chip temperature sensor
- Power modes
  - Run
  - Deep sleep
  - Hibernation
  - Dynamic power
  - Doze
  - Nap

  - Sleep
- General purpose timers
  - Eight general-purpose timers
  - Real-time clock
- IEEE 1149.1 compliant JTAG boundary scan

3 Developer Environment

The MPC5121e is the latest addition to the mobileGT family of processors. Due to the consistent application of the e300 CPU core, significant software support and compatibility exists even prior to product introduction. Freescale is working to enable significant levels of firmware and software driver support at product introduction. This will include popular real-time operating systems from Green Hills, QNX, and Wind River. Freescale will also enable open-source Linux solutions.

An integrated development environment (IDE) will be provided by Freescale and include a full set of tools for compiling, assembling, linking, etc., which includes the e300 core and the AXE core. There will be CodeWarrior support for hardware-level development and to enable simultaneous multi-core debugging. Further, there will be tools for the AXE allowing developers and customers to expand the already-significant list of audio algorithms planned. These include many popular algorithms for decode and encode such as MPEG1 Layer 2/3, MPEG2 Layer 2/3, AAC, and Ogg Vorbis. An operating system audio driver can be used to enable the accelerated function that simplifies the writing of user applications software. There will also be support for sample rate conversion for efficient speech recognition solutions.

To provide a standard reference for these software solutions, Freescale has a standard hardware platform for the MPC5121e. This highly-flexible development board is packed with many features for application development, which includes on-board DRAM, NOR/NAND flash, RS232 ports, CAN ports, Ethernet, audiot ports, SATA/PATA drive support, PCI, DVI connector, TFT display connector. They are all in a mini-ATX form factor.

For more details, contact your local Freescale sales representative.

4 Document Revision History

Table 1 provides a revision history for this product brief.

Table 1. Revision History

Revision	Substantive Change(s)
Rev. 0, 04/18/2007	Initial release
Rev. 1, 02/15/2008	

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