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MPC5744P Product Brief

32-bit Qorivva dual-core MCU built on Power Architecture® technology, suitable for ISO26262 ASIL-D chassis and safety applications

The MPC5744P Qorivva microcontroller is based on the Power Architecture® developed by Freescale. It targets chassis and safety applications and other applications requiring a high Automotive Safety Integrity Level (ASIL). The MPC5744P is a SafeAssure solution.

All devices in this family are built around a safety concept based on delayed lock step, targeting an ISO26262 ASIL-D (Design) integrity level. According to FMEDA analysis, critical components of the microcontroller that must be replicated are the CPU core and DMA controller. Lock step Checking Units are implemented at each output of these blocks to compare the values between the redundant blocks.

In addition, the MPC5744P provides:

- A programmable Fault Collection and Control Unit (FCCU) to monitor the integrity status of the device and provide flexible safe state control.
- End-to-End Error Correcting Code (e2eECC) for improved fault tolerance and detection:

Contents

1	Target Applications	2
2	Features	3
2.1	Compatibility with MPC5643L	5
2.2	Block Diagram	6
2.3	Performance Parameters	8
2.4	Chip Features	9
2.5	Feature Differences by Package	10
2.6	Module Features	11
3	Developer Environment	34
4	Ordering information	34
5	Document Revision History	35



Target Applications

- All bus masters generate Single Error Correcting and Double Error Detecting (SECDED) code for every bus transaction
- SECDED covers 64-bit data and 29-bit address
- ECC is stored in memories on write operations and validated by the master on every read operation

The host processor core of the MPC5744P is a CPU from the e200 family of compatible Power Architecture cores. The Zen z420n3 dual issue core provides very high efficiency—high performance with minimum power dissipation—and operates at a maximum frequency of TBD (design target: 180 MHz or greater).

A Memory Protection Unit is also included which supports protections of various instruction and data memory areas.

The MPC5744P has a single level of memory hierarchy consisting of 384 KB on-chip SRAM and 64 KB tightly coupled local data SRAM with ECC and 2.5 MB on-chip flash memory including ECC. Both the SRAM and the flash memory can hold instructions and data.

Off-chip communication is performed by a suite of serial protocols including FlexRay, CANs, enhanced SPIs (DSPIs), SCIs (LINFlexD), SIPI (via LFAST), and the SENT sensor interface.

The System Integration Unit “Lite” (SIUL2) performs several chip-wide configuration functions. The SIUL2 controls pad configuration and general-purpose input/output (GPIO). It also provides external interrupts and reset control. The highly configurable I/O multiplexing block provides multiplexing options for the device pins’ output and input paths (for example, daisy chaining the DSPIs and external interrupt signal).

The peripheral set is compatible with the MPC5643L, providing high-end electrical motor control capability with very low CPU intervention due to the on-chip Cross Triggering Unit (CTU).

The MPC5744P is developed with 55 nm embedded flash memory technology, providing a significant performance improvement.

1 Target Applications

As a SafeAssure solution, the MPC5744P microcontroller targets applications requiring a high automotive Safety Integrity Level (SIL), especially:

- Chassis applications
- Electrical Stability Control (ESC)
- Higher-end Electrical Power Steering (EPS)
- Airbag and sensor fusion applications

A typical aspect of ESC and EPS is the presence of an advanced electrical motor control periphery with special enhancements in the area of pulse width modulations, highly flexible timers, and functional safety.

All devices in this family are built around a safety concept based on delayed lock step, targeting an ISO26262 ASIL-D integrity level.

2 Features

Table 1 summarizes the features of the MPC5744P.

Table 1. MPC5744P feature summary

Feature	Details
CPU	
Power Architecture	2 x e200z4 in delayed lock step
Architecture	Harvard
Execution Speed	0 MHz to TBD (design target: 180 MHz or greater) (+2% FM)
Embedded FPU	Yes
Core MPU	24 regions
Instruction Set PPC	No
Instruction Set VLE	Yes
Instruction cache	8 KB, EDC
Data cache	4 KB, EDC
Data local memory	64 KB, ECC
System MPU	Yes (16 regions)
Buses	
Core bus	AHB, 32-bit address, 64-bit data, e2e ECC
Internal periphery bus	32-bit address, 32-bit data
Crossbar	
Master x slave ports	4 x 5
Memory	
Code/data flash memory	2.5 MB , ECC, RWW
Data flash memory	Supported with RWW
SRAM	384 KB , ECC
Modules	
Interrupt controller	32 interrupt priority levels, 16 software programmable interrupts
PIT	1 module with 4 channels
System Timer Module (STM)	1 module with 4 channels
Software Watchdog Timer (SWT)	Yes
eDMA	32 channels, in delayed lock step
FlexRay	1 module with 64 message buffer, dual channel
FlexCAN	3 modules with 64 message buffer
LINFlexD (UART and LIN with DMA support)	2 modules
Clockout	Yes

Table 1. MPC5744P feature summary (continued)

Feature	Details
Fault Collection and Control Unit (FCCU)	Yes
Cross Triggering Unit (CTU)	2 modules
eTimer	3 modules with 6 channels
FlexPWM	2 modules with 4 x (2+1) channels
Analog-to-digital converter (ADC)	4 modules with 12 bit ADC, each with 16 channels (25 external channels including shared channels plus internal channels)
Sine-wave generator (SWG)	32 point
DSPI	4 modules As many as 8 chip selects
CRC Unit	Yes
SENT	2 modules with 2 channels
Interprocessor serial link interface (SIPI)	Yes
Junction temperature sensor	Yes Replicated module
Digital I/Os	>= 16
Peripheral register protection	Yes
Supply	
Device Power Supply	3.3 V with external ballast transistor or 3.3 V with external 1.25 V low drop-out (LDO) regulator
ADC Analog Reference voltage	3.15 V to 3.6 V and 4.5 V to 5.5 V
Clocking	
Phase Lock Loop (PLL)	1 x PLL and 1 coupled FMPLL
Internal RC Oscillator	16 MHz
External Crystal Oscillator	8 MHz to 40 MHz
Low power modes	
HALT and STOP	Yes
Debug	
Nexus	Level 3+, MDO and Aurora interface
Package	
LQFP	144 pins
LQFP exposed pads (EP)	176 pins
MAPBGA	257 MAPBGA

Table 1. MPC5744P feature summary (continued)

Feature	Details
Temperature	
Temperature range (junction)	-40°C to +150°C, option for 165°C
Ambient temperature range (LQFP)	-40°C to +125°C, TBD option (with 165°C junction option)
Ambient temperature range (BGA)	-40°C to +125°C, TBD option (with 165°C junction option)

The MPC5744P architecture is based on the Automotive Core Platform (ACP) developed as part of the C55 Template.

This architecture is centered around the scalable e200 family, the AMBA standards, and Freescale’s IP standards.

- AMBA is a 64-bit bus supporting a minimum bus cycle of 1 clock (one for address and one for data phase with limited pipelining). AMBA masters are implemented within the flexible crossbar and a very flexible synchronous protocol converter AMBA-to-IPS gasket (AIPS) is available.
- IPS is a 32-bit single master protocol that needs a minimum of 3 AMBA cycles for unbuffered write and minimum of 2 clocks for periphery read.

Redundancy is implemented for those blocks requiring it to ensure high diagnostic coverage for the key IP (for example: the e200z4 core, the DMA controller, and the AIPS bus bridge with the peripheral subsystems).

The architecture aims to guarantee maximum throughput at TBD (design target: 180 MHz or greater).

2.1 Compatibility with MPC5643L

The MPC5744P is compatible in important ways with the MPC5643L, a predecessor device in 90 nm CMOS technology. For customers migrating to the MPC5744P, this high degree of compatibility enables re-use and reduces unnecessary changes. The following table summarizes key aspects of the compatibility.

Table 2. MPC5744P Compatibility with MPC5643L

Topic	Remarks for MPC5744P
Package: 144 LQFP	Delivered in the same 144 LQFP with compatible pinout.
Package: 257 MAPBGA	Delivered in the same 257 MAPBGA package. The pinout is compatible, but with limitations due to the new LFAST and Aurora interfaces. Board changes are required.
Power supply concept	Supports an external ballast transistor with internal regulation that allows compatible use. In addition, offers an option with an external supply for the 1.25 V core voltage.
Supply monitoring	The same low voltage monitors for the 1.25 V core voltage and the 3.3 V voltage domains are offered. Both devices offer a high voltage detection for the 1.25 V domain.

Table 2. MPC5744P Compatibility with MPC5643L (continued)

Topic	Remarks for MPC5744P
Power supply pins	All power supply pins in 144 LQFP package are the same between the two parts, with an exception: the VDD_HV_REG_x pins are replaced with pads for reset/GPIO functionality because the MPC5744P does not offer an internal ballast supply option. When the MPC5744P is soldered into a board designed for the MPC5643L that is unchanged, these GPIOs must not be configured as output.
I/O multiplexing	All I/O multiplexing options in the 144 LQFP package are maintained to allow use of the same peripheral interfaces on the same pins. The MPC5744P adds additional multiplexing for new functionality.
ADC channels and reference voltage	The same pins can be mapped to the same ADC module channels. The ADC are 5 V input capable and have separate reference voltages, The use of ADC pads as inputs on the MPC5744P follows a 5 V I/O specification. In contrast, the specification is 3.3 V on the MPC5643L.
External hardware for safety	The same external components are required as on the MPC5643L: <ul style="list-style-type: none"> • monitoring of the Error Out interface • external watchdog functionality (periodic communication) • external 3.3 V HVD

2.2 Block Diagram

Figure 1 is a top-level diagram that shows the functional organization of the system.

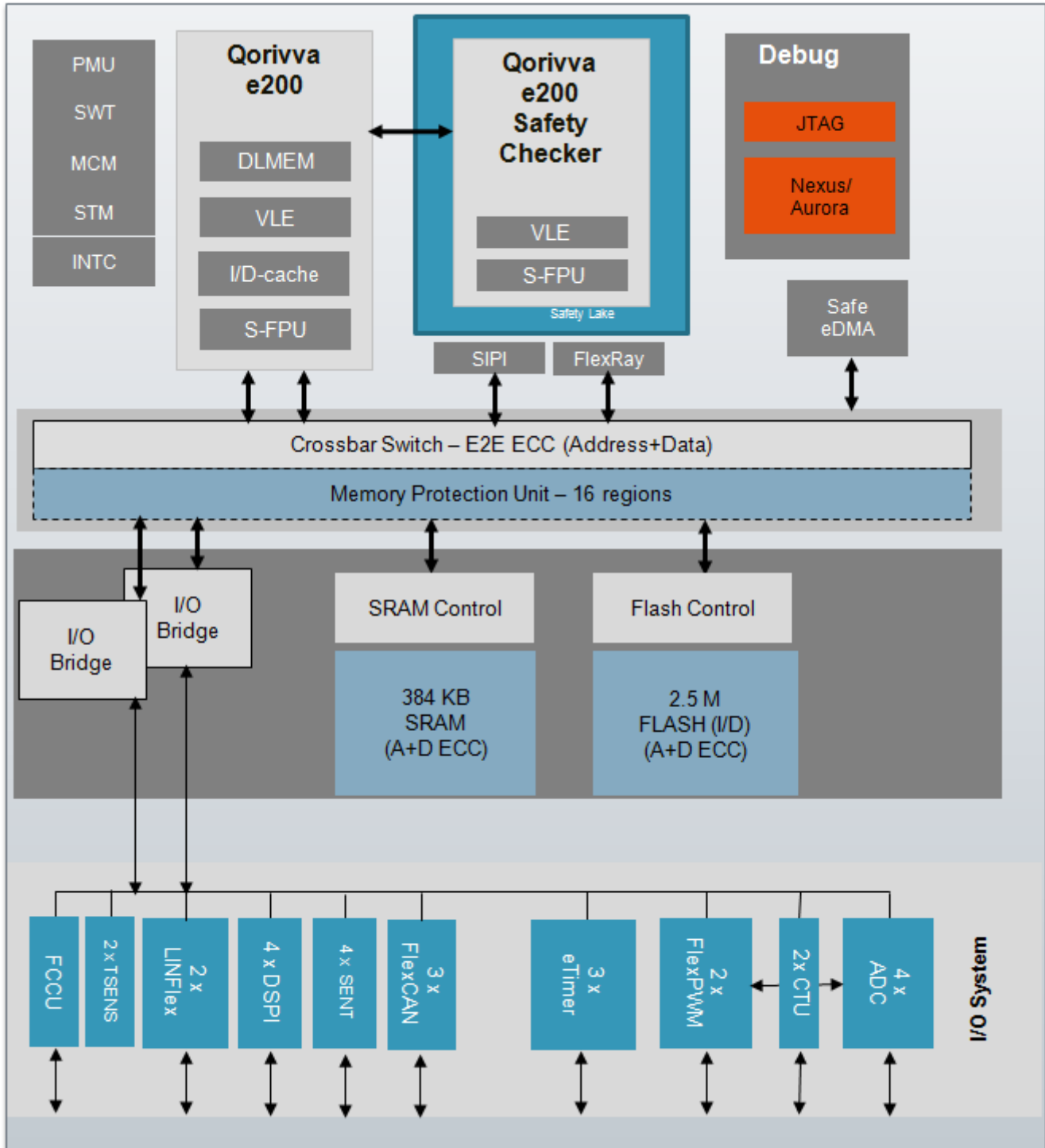


Figure 1. System Block Diagram

2.3 Performance Parameters

2.3.1 Operating Parameters

The MPC5744P system-on-chip (SoC) operating parameters are listed as follows:

- Fabricated in 55 nm low power process
- Internal voltage regulator (VREG) with external ballast transistor
 - Single supply designs offering high integration level to the customer
 - Possibility to supply 1.25 V internal logic from external regulator
- 1.25 V \pm 5% for digital core input supply voltage
- Low power design
 - Dynamic clock gating of core and peripherals
 - Software controlled clock gating of peripherals
 - HALT and STOP mode support
 - Power consumption targeted for 400 mA (RUNIDD typical at $T_J = 150^\circ\text{C}$)
- Selectable output edge rate control (full drive, half drive, full drive with slew-rate control, and half drive with slew-rate control)
- 3.15 V to 3.6 V Nexus pin rail—same as digital I/O rail
- Unused pins configurable as GPIO (or GPI for unused A/D channel inputs)
- 3.15 V to 3.6 V / 4.5 V to 5.5 V for A/D converter reference and analog input pins
- Designed with EMI reduction techniques
 - Phase locked loop
 - System clock with frequency modulation
 - On-chip bypass capacitance
 - Software selectable output edge rate control
 - Schmitt trigger on selected inputs
- Configurable pins
 - Selectable pullup, pulldown, or no pull on all pins controlled by the System Integration Unit “Lite” (SIUL2)
 - Selectable open drain
- Redundant temperature sensors in separate safety channels
- Multiple Low/High Voltage detector and inhibit units
 - High voltage detection and inhibit with off-line testing capability on 1.25 V only
 - Low voltage detection and inhibit with off-line testing capability on 1.25 V and 3.3 V supply
- Deep N-well to eliminate Single Event Latchup (SEL) and wide column multiplexing where required to reduce Soft Error Rate (SER) effect for SRAM
- Physical separation of replicated functional blocks achieved by layout

2.3.2 Operating Conditions

This section describes the operating conditions and environmental constraints under which the MPC5744P device is fully operational.

- Fully static operation 0 MHz to TBD (design target: 180 MHz or greater) plus 2% Frequency Modulation (SYS_CLK)
- 3.15 V to 3.6 V (minimum tolerance) for digital I/O input supply voltage
- 3.15 V to 3.6 V / 4.5 V to 5.5 V for A/D converter reference and analog input pins
 - A/D reference pins supply both converter reference and internal switch
- -40°C to +150°C junction temperature, option for 165°C extended temperature
- Lifetime for all products is 20 years which is equivalent to 12500 hours of active operation
- EEPROM emulation blocks write erase cycle life time
 - Blocks with 0 to 1000 P/E cycles with 20 years minimum
 - Blocks with 1001 to 10000 P/E cycles with 10 years minimum
 - Blocks with 10001 to 100000 P/E cycles with 5 years minimum
- Particle Radiation
 - Alpha Particles
 - Alpha particles are easily stopped by device packaging materials. Thus alpha emission outside the device does not need to be considered for SER. Only alpha emission internal to the device can interact with circuits and cause a soft error event.
 - Alpha particle flux < 0.001 alpha/cm²/h (low alpha mold compound material required)
 - High-energy cosmic neutrons
 - Neutrons with energies of 10 MeV or more contribute significantly to the SER. Neutrons with lower energies produce few additional upsets and are often ignored. The exact energy threshold depends on the properties of the silicon device but is decreasing with technology scaling. Neutrons are not attenuated by device packaging material and require several feet of concrete for any significant attenuation. The flux of neutrons with energies above 10 MeV at sea level is 14 neutrons/cm²/h in New York City. The neutron flux varies by as much as 30% as a function of the solar cycle and is affected by pinpoint solar flares. Furthermore, the neutron flux depends strongly on altitude and weakly on geographical location. At a height of 3 km, the neutron flux is almost ten times as high as at sea level.
 - Neutron flux < 14 neutrons/cm²/h (from 10 to 800 MeV), following the JESD-89 standard (normal background neutron flux at sea level at New York City, NY)

2.4 Chip Features

2.4.1 Mode Of Operation

The MPC5744P has one mode of operation:

- Delayed Lock Step Mode (LSM)

Features

2.4.1.1 Delayed Lock Step Mode

This mode supports the highest safety level. It is defined to enable reaching ASIL-D with minimum software overhead.

The safety concept is based on delayed lock step operation of the central processing blocks that must be redundant to meet the safety level of the standard. The CPU and DMA are in delayed lock step mode which means that the according checker block will receive all inputs delayed by 2 clock cycles. Outputs of the checker blocks will be compared with outputs of the first CPU and DMA. Any difference will be flagged as an error and processed by the Fault Collection and Control Unit (FCCU).

The delayed lock step mode is always enabled. There is no switch possible to a mode where just one CPU operates or where both CPUs operate in parallel for higher performance.

2.4.2 SafeAssure—Functional Safety Suitability

The MPC5744P device is targeted to meet functional safety according to ISO26262, level ASIL-D.

2.4.3 Packages

The MPC5744P is offered in the following package types:

- 144-pin LQFP: 0.5 mm pitch, 20 mm x 20 mm outline
- 176-pin LQFP exposed pad: 0.5 mm pitch, 24 mm x 24 mm outline
- 257 MAPBGA: 0.8 mm pitch, 14 mm x 14 mm outline

For all packages: Maximum ambient temperature 125°C, junction temperature 150°C; with extended ambient temperature option TBD, junction temperature 165°C (packaged version).

2.5 Feature Differences by Package

Most features are available in all of the package options. The following table summarizes features that differ among the packages.

Table 3. MPC5744P Features Differing by Package

Feature	144 LQFP	176 LQFP	257 MAPBGA
FlexPWM1	A[0-2]/B[0-2]	A[0-3]/B[0-3]/X[0-1]/Fault[0:3]	A[0-3]/B[0-3]/X[0-3]/Fault[0:3]
eTimer2	ETC2-5	ETC0-5	ETC0-5
Supplies	3.3 V (IO): 4 x V_{DD} , 4 x V_{SS} 3.3 V (PMU): 1 x V_{DD} ¹ 3.3 V (OSC): 1 x V_{DD} ¹ 3.3 V (flash): 1 x V_{DD} ¹ 1.25 V (core): 6 x V_{DD} , 8 x V_{SS} 1.25 V (PLL): 1 x V_{DD} ¹ , 1 x V_{SS} 1.25 V (flash): 1 x V_{DD} ^{2, 1} 3.3 V/5 V (ADR): 2 x V_{DD} , 2 x V_{SS} 3.3 V (ADV): 1 x V_{DD} , 1 x V_{SS}	Additional supplies beyond 144 LQFP: 3.3 V (IO): 2 x V_{DD} , 2 x V_{SS} 1.25 V (LFAST): 1 x V_{DD}	Additional supplies beyond 176 LQFP: 3.3 V (IO): 3 x V_{DD} , 13 x V_{SS} 1.25 V (core): 18 x V_{DD} , 17 x V_{SS}
GPIO	77 GPIO 22 GPI	Additional GPIO beyond 144 LQFP <ul style="list-style-type: none"> • 17 GPIO • 4 GPI • 2 LFAST differential pads 	Additional GPIO beyond 176 LQFP <ul style="list-style-type: none"> • 16 GPIO • Aurora Interface: 2 x transmit, 1 x receive (reference clock)
DSPI3	No external signals	No external signals	CS0-3
CTU external trigger(s)	CTU0	CTU0	CTU0 CTU1
ADCs ³	<ul style="list-style-type: none"> • 22 analog pads assigned to ADC0, ADC1, and ADC3 • Shared channels between ADC0/ADC1 and ADC1/ADC3 	<ul style="list-style-type: none"> • 25 analog pads assigned to ADC0, ADC1, ADC2, and ADC3 • Shared channels between ADC0/ADC1, ADC1/ADC3, and ADC2/ADC3 	<ul style="list-style-type: none"> • 25 analog pads assigned to ADC0, ADC1, ADC2, and ADC3 • Shared channels between ADC0/ADC1, ADC1/ADC3, and ADC2/ADC3
SIPI/LFAST interface	No	Yes	Yes
Nexus	Yes (MDO interface)	Yes (MDO interface)	Yes (RDY_B)
Nexus Aurora port	No	No	Yes (TX0/TX0_P/TX1/TX1_P/CLK/CLK_P)

NOTES:
¹ V_{SS} connected to Core Ground on 144LQFP

² 1.25 V flash memory supply connected to Core Supply on 144LQFP (93)

³ For all packages, internal analog sources/supplies can be connected to ADC0, ADC1, ADC2, and ADC3.

2.6 Module Features

2.6.1 High performance e200z420n3 Core Processor

The Zen processor family is a set of CPU cores that implement low-cost versions of the *PowerISA 2.06* architecture.

Features

The Zen z420n3 is a dual-issue, 32-bit, *PowerISA 2.06* VLE-compliant design with 32-bit general purpose registers (GPRs).

- The z420n3 core implements the VLE (variable-length encoding) ISA, providing improved code density.
- The base *PowerISA 2.06* fixed-length 32-bit instruction set is not directly supported.

An Embedded Floating Point (EFPU2) APU (Auxiliary Processing Unit) is provided to support real-time, single-precision, embedded numerics operations using the general-purpose registers.

The z420n3 processor integrates a pair of integer execution units, a branch control unit, an instruction fetch unit, a load/store unit, and a multi-ported register file capable of sustaining six read and three write operations per clock cycle. Most integer instructions execute in a single clock cycle. Branch target prefetching is performed by the branch unit to allow single-cycle branches in many cases.

The z420n3 also contains an 8 KB Instruction Cache and a 4 KB Data Cache, as well as a Nexus Class 3+ debug module.

A Memory Protection Unit is also included which supports protections of various instruction and data memory areas.

Features

The following is a list of some of the key features of the z420n3:

- Dual issue 32-bit *PowerISA 2.06*-VLE compliant CPU
- In-order execution and retirement
- Precise exception handling
- Branch processing unit
 - Dedicated branch address calculation adder
 - Branch target prefetching using BTB
 - Return Address Stack
- Load/store unit
 - 2 cycle load latency
 - Fully pipelined
 - Misaligned access support
- 32-bit General Purpose Register file
- Dual AHB 2.v6 64-bit System buses
- Local Data Memory (DMEM) with shared AHB 2.v6 64-bit slave interface
- Memory Protection Unit (MPU) implementing a 24-entry region descriptor table with support for 6 arbitrary-sized instruction memory regions, 12 arbitrary-sized data memory regions, and 6 additional arbitrary-sized instruction or data memory regions
- 2-Way Set Associative Harvard Instruction Cache (8Kbyte)
- 2-Way Set Associative Harvard Data Cache (4Kbyte)
- Embedded Floating-point APU (EFPU2) supporting single-precision floating-point operations
- Performance Monitor APU supporting execution profiling

- Nexus Class 3-plus Real-time Development Unit
- Power management
 - Low power design - extensive clock gating
 - Power saving modes: doze, nap, sleep, wait
 - Dynamic power management of execution units, Cache and Local memories
- Testability
 - Synthesizeable, MuxD scan design
 - ABIST/MBIST for arrays
 - Built-in LBIST

2.6.2 Crossbar Switch (XBAR)

The AXBS multi-port crossbar concurrently supports up to 4 simultaneous connections between master ports and slave ports. AXBS supports the AMBA AHB2.0 AHB-Lite protocol with AMBA V6 extensions for exclusive access support, extended cache control attributes, and misaligned data transfers (referred to as AHB2v6). AXBS supports a 32-bit address bus width and a 32 or 64-bit data bus width at all master and slave ports. It also supports both address and data sideband signals which are used to implement decorated storage and the e2eECC for the MPC5744P. A flow-through design allows zero wait-state slave responses.

Features

- Supports four master ports and five slave ports
- 32-bit Address, 64-bit Data paths (applies to all ports) with misaligned access signaling
- Concurrent transfers between independent master and slave ports
- Programmable arbitration priorities on a per-slave port basis
- Round-robin arbitration available on a per-slave port basis
- Parking on slave ports: explicit master, park_on_last_master, none (low power parking)
- Parameterized design description allows system designer to customize the exact crossbar implementation for a given platform instantiation

2.6.3 System Memory Protection Unit (SMPU)

The platform shell concept supports implementation of a three-level hierarchical set of storage resources distributed throughout the microcontroller. In a similar manner, the memory protection resources are also implemented in a three-level hierarchical manner. *The memory protection functionality is intended to provide hardware support for isolation between user and supervisor tasks through the application of region descriptors defining access control rights.* The three layers of memory protection are:

1. Processor core memory protection (CMPU), typically for its local memories (DMEM), in the core
2. System memory protection (SMPU) on the slave side of the crossbar switches
3. Peripheral access control registers (PACRs) for each address space slot in the PBRIDGE

Since the protection requirements for each level of this hierarchy differ, the corresponding hardware implementations vary across the three functions.

Features

The second layer of memory protection is implemented in the SMPU. System Memory Protection Unit splits the physical memory into 16 different regions. Each master (DMA, FlexRay, CPU, SIPI) can be assigned different access rights to each region.

- 16 regions MPU with concurrent checks against each master access
- 32 byte granularity for protected address region

2.6.4 Enhanced Direct Memory Access (eDMA)

The enhanced Direct Memory Access (eDMA) module is a second-generation platform module capable of performing complex data movements with minimal intervention from a host processor via 32 programmable channels. The hardware microarchitecture includes a `dma_engine` which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels. This implementation is utilized to minimize the overall module size.

Features

- 32-channels
- Connections to the AHB crossbar switch for data movement, IPS bus for programming the module, with 64-bit connections to the AHB bus.
- 32-byte transfer control descriptor per channel
- Data movement via dual-address transfers: read from source, write to destination
- Programmable source, destination addresses, transfer size, support for enhanced addressing modes
- Support for major and minor counters; one request and one interrupt per channel
- Support for channel-to-channel linking and scatter/gather for continuous transfers; fixed priority and round-robin channel arbitration

2.6.5 Platform Flash Memory Controller (PFLASH)

The PFLASH acts as an interface between the system bus (AHB-Lite 2v6) and the c55fm flash array. It intelligently converts the protocols between the system bus and the dedicated flash array interface.

The PFLASH supports a single 64-bit AHB bus and a 256-bit read data interface from each flash memory array. The PFLASH contains a 4-way set associative mini-cache as well as an associated controller that prefetches sequential lines of data from the flash arrays into the mini-cache. This local storage mechanism serves to deliver flash read data with zero-wait-state response on lines that reside in the cache. AHB read requests that miss the cache generate the needed flash array access and are forwarded to the AHB upon completion, typically incurring wait states based on the pipelined flash access time.

Features

- Supports up to 16 MB of flash memory with 24 bits of array addresses available
- System bus supports one 64-bit AHB interface

- Array interface supports a 256-bit read data bus + 64-bit write data buses
- Configurable read buffering and line prefetching support via 4-way set-associative mini-cache + prefetch controller to provide single-cycle “buffer hit” read response
- Configurable access control based on read/write and AHB master ID attributes
- Configurable access timing (wait-state programmable) allowing use in a wide range of frequency targets
- Optional address pipelining capability to optimize flash array throughput
- Support for reporting of single- and multi-bit flash ECC events on a 64-bit doubleword boundary
- Overlay access to System RAM

2.6.6 Platform RAM Controller (PRAM)

The PRAM memory controller module is the platform RAM array controller supporting the end-to-end ECC algorithm defined in this family of automotive microcontrollers. It is designed for use in high-performance platforms and supports a programmable zero or one wait-state response for all reads and zero wait-state doubleword-sized writes. Since the e2eECC is organized on a 64-bit data item, byte, halfword and word writes incur a 1-cycle stall so the PRAM controller can perform the required read-modify-write operation needed for ECC check and regeneration.

Features

- High-performance memory controller for cached and cacheless processor cores
- Supports byte-, halfword-, word- and doubleword-sized reads and writes
- Array interface supports 64-bit data + 8-bit end-to-end ECC algorithm
- Late write support via store buffer for single-cycle write accesses
- Supports programmable zero or one wait-state response for all reads
 - Read burst transactions support zero wait-state response on secondary accesses, that is, a {1,2}-1-1-1 response for a 4-beat burst
- Supports zero wait-state response for all double-word-sized writes
 - 8-, 16- and 32-bit writes incur a 1-cycle wait-state to perform the needed read-modify-write for ECC check and generation
- Supports a “backdoor” AHB port from platform flash controller
 - Used to retarget flash data calibration overlay accesses to the system RAM
 - Treated as highest priority access request
 - Will interrupt any frontdoor port request, including burst accesses, so calibration data timing can be maintained

2.6.7 On-chip Flash Memory with ECC

The MPC5744P on-chip flash memory provides programmable, non-volatile flash memory. The non-volatile memory (NVM) can be used for instruction storage or data storage, or both. The flash memory module interfaces the system bus to a dedicated flash memory array controller. It supports a 64-bit data

Features

bus width at the system bus port, and a 256-bit read data interface to flash memory. The module contains a 4-way set-associative mini-cache.

The flash memory module provides the following features

- 2.5MB flash memory in unique multi-partitioned hard macro
- Partitioning:
 - 4x 16 KB in partition 0/1 (2x blocks EEPROM emulation enabled)
 - 2x 32 KB in partition 2/3 (EEPROM emulation enabled)
 - 6x 64 KB in partition 4/5
 - 8x 256 KB in partition 6/7
- Support for reading-while-writing when the accesses are to different partitions.
- Flash memory protection
 - Write protection and OTP available for dedicated blocks.
- Test information stored in a non-volatile UTest block which will be OTP.
- Erase suspend, program suspend and erase-suspended program all supported.

2.6.8 On-chip SRAM with ECC

The MPC5744P device SRAM provides a general-purpose single port memory.

Frequency targets and SRAM wait states:

- 1 WS for SRAM read accesses at TBD (design target: 180 MHz or greater) + FM modulation system frequency

NOTE

Note also the 1 (or 2, if required) cycle transaction applies to the AHB “view” of a read transfer. The end-to-end ECC logic adds another cycle of latency in the bus master, making the transfer appear as a 2 (or 3) cycle read to the master)

ECC handling is done on a 64-bit boundary for data and it is extended to the address to have the highest possible diagnostic coverage including the array internal address decoder.

The SRAM module provides the following features:

- System SRAM: 384 KB
- ECC on 64-bit word (syndrome of 8bit)
 - ECC covers SRAM bus address
- 1 bit error correction and 2 bit error detection

2.6.9 Memory Subsystem Access Time

Every memory access the CPU performs requires at least one system clock cycle for the data phase of the access. Slower memories or peripherals may require additional data phase wait states. Additional data

phase wait states may also occur if the slave being accessed is not “parked” on the requesting master in the crossbar.

Table 4 shows the number of additional data phase wait states required for a range of memory accesses.

Table 4. MPC5744P platform memory access time summary

AHB Transfer	Data Phase Wait States ¹	Description
e200z420n3 Instruction Fetch	0	FLASH prefetch buffer hit (page hit)
e200z420n3 Instruction Fetch	8	FLASH prefetch buffer miss
e200z420n3 Data Read/Write	0	Local Data RAM read/write
e200z420n3 Data Read	1 ²	System RAM read
e200z420n3 Data Write	0 ³	System RAM 64-bit write
e200z420n3 Data Write	1-2 ⁴	System RAM 8,16,32-bit write (Read-modify-Write for ECC)
e200z420n3 Data Flash Memory Read	0 ⁵	FLASH prefetch buffer hit (page hit)
e200z420n3 Data Flash Memory Read	8	FLASH prefetch buffer miss (excluding 1-cycle of PFLASH controller evaluation of buffer hit)

NOTES:

- ¹ Maximum core frequency TBD (design target: 180 MHz or greater).
- ² The end-to-end ECC logic adds another cycle of latency in the bus master which is not included here.
- ³ The end-to-end ECC logic adds another cycle of latency in the bus master which is not included here.
- ⁴ The end-to-end ECC logic adds another cycle of latency in the bus master which is not included here. Non-correctable errors on <64-bit writes to the SRAM incur an additional WS.
- ⁵ The end-to-end ECC logic adds another cycle of latency in the bus master which is not included here.

2.6.10 Memory Error Management Unit (MEMU)

The MEMU is responsible for collecting and reporting error events associated with error correction code (ECC) logic used on SRAM, peripheral system RAM, and flash memory. When any of the following events occur, the MEMU receives an error signal that causes an event to be recorded and corresponding error flags to be set and reported to the Fault Collection and Control Unit (FCCU).

- Correctable Error consists of:
 - Single bit error in the data part that is detected via ECC for a system RAM or peripheral system RAM or flash memory
- Uncorrectable Error consists of:
 - Multiple bit error that is detected via ECC for a peripheral system SRAM, system RAM or flash memory
 - Addressing errors and unused data bit errors detected by ECC logic

2.6.11 AMBA-AHB-to-IPS/APB Bus Controller “Lite” (AIPS-Lite)

The AIPS-Lite module converts the 32/64-bit AMBA AHB 2.0Lite + V6 extensions interface (AHB2v6) to IPS and AMBA-APB interfaces.

Features

Features

- Direct support for up to thirty-two on-platform IPS peripherals, each with a dedicated module enable and a 16 KB memory space
- Direct support for up to 128 off-platform IPS or APB peripherals, each with a dedicated module enable and a 16 KB memory space
 - The operating clock speed of each off-platform slot can be independently specified as any integer divider (1, 2, 3,...) of the platform's clock speed if the peripheral allows this.
- Supports 8-, 16-, and 32-bit slave peripherals via byte, halfword, word reads and writes (transaction size must be \leq port size)

2.6.12 Interrupt Controller (INTC)

The INTC (interrupt controller) provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems.

For high priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource are supported.

The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource can not preempt each other.

The INTC provides the following features:

- Unique 10-bit vector per interrupt source
- 32 priority levels with fixed hardware arbitration within priority levels for each interrupt source
- Capable of handling up to 1023 selectable-priority interrupt request sources
- Priority elevation for shared resource
- 16 software interrupts are supported.

2.6.13 System Clocks and Clock Generation

The following list summarizes the system clock and clock generation on the MPC5744P:

- Lock status continuously monitored by lock detect circuitry
- Loss of clock (LOC) detection for reference and feedback clocks
- Programmable output clock divider of system clock
- Progressive clock frequency switching of system clock
- On-chip crystal oscillator with automatic level control
- Dedicated internal 16 MHz internal RC oscillator for rapid start-up

- Supports frequency trimming by user application
- Auxiliary clock domain with independent source clock selection for motor control periphery (FlexPWM, eTimer, CTU, ADC and SWG)

2.6.14 PLLs

The MPC5744P has a dual PLL—a Frequency Modulated PLL (FMPLL) and an auxiliary PLL—that provides separate system and peripheral clocks to the device.

Each PLL allows the user to generate high speed system clocks. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor, output clock divider ratio are all software configurable. The PLLs have the following major features:

System Frequency Modulated PLL

- Voltage controlled oscillator (VCO) range from 600 MHz to 1250 MHz
- Frequency modulation via software control to reduce and control emission peaks
 - Modulation depth $\pm 2\%$ if centered or -0.5% to -4% if downshift via software control register
 - Modulation frequency: triangular modulation with 250 kHz max
- Option to switch on and off the modulation via the software interface
- Reduced frequency divider (RFD) for reduced frequency operation without re-lock
- Three modes of operation
 - Bypass mode
 - Normal PLL mode with crystal reference (default)
 - Normal PLL mode with external reference
- Lock monitor circuitry with lock status
- Loss of Lock detection for reference and feedback clocks
- On-chip loop filter

Auxiliary PLL (not frequency modulated)

- Input frequency (first PLL): 8 MHz to 40 MHz continuous range (limited by the crystal oscillator)
- Used for FlexRay due to precise symbol rate requirement by the protocol
- Used for motor control periphery and connected IP (A/D digital interface CTU) to allow independent frequencies of operation for PWM and timers and jitter-free control
- Option to enable/disable modulation to avoid protocol violation on jitter and/or potential unadjusted error in electric motor control loop
- Allows to run Motor control periphery at different (precisely lower, equal or higher as required) frequency than the System to ensure higher resolution

2.6.15 Main Oscillator

The main oscillator provides these features:

- Input frequency range 8 MHz to 40 MHz

Features

- Crystal input mode
- Oscillator input mode 3.3 V
- PLL reference

2.6.16 Internal RC Oscillator

The architecture uses constant current charging of a capacitor. The voltage at the capacitor is compared to the stable bandgap reference voltage. The RC oscillator is the device safe clock.

The RC oscillator provides these features:

- Nominal frequency 16 MHz (untrimmed frequency from 9.6 MHz to 24 MHz)
- Targeting less than $\pm 5.0\%$ variation over voltage and temperature after process trim
- Clock output of the RC oscillator serves as system clock source in case loss of lock or loss of clock is detected by the PLL
- RC oscillator is used as the default system clock during startup and can be used as backup input source of PLL(s) in case the main oscillator fails

2.6.17 Clock, Reset, Power, and Mode control module

The Clock, Reset, Power and Mode control module has the following features:

- Clock gating and clock distribution control
- Halt and stop mode control
- Flexible configurable System and auxiliary clock dividers
- Three main reset phases
 - Initial power up sequence
 - Flash memory initialization and User option bits
 - Release of Sea-of-gates reset
- Various modes of execution
 - Reset, Idle, Test, Safe
 - Various RUN modes with software selectable powered modules

2.6.18 Periodic Interrupt Timer (PIT) Module

The PIT module implements the features below:

- 4 general purpose interrupt timers
- 32-bit counter resolution, chaining mode to implement a 64-bit timer
- Clocked by system clock frequency
- Can be used for software tick or Periodic DMA trigger operation

2.6.19 System Timer Unit (STM)

The STM module implements the features below:

- Up-counter with 4 output compare registers
- OS Task protection and Hardware tick implementation as per current state-of-the-art AutoSAR requirement

2.6.20 Safe Software Watchdog Timer (SWT)

This module implements the features below:

- Safe internal RC oscillator or oscillator clock as reference clock
- Windowed watchdog
- Program flow control monitor with 16-bit pseudorandom key generation
- Master access protection
- Hard and soft configuration lock bits

2.6.21 Fault Collection and Control Unit (FCCU)

The FCCU module has the following features:

- Redundant collection of hardware checker results
- Redundant collection of error information and latch of faults from critical modules on the device
- Collection of test results
- Configurable and graded fault control
 - Internal reactions (No internal reaction, NMI, Reset or safe mode)
 - External reaction (failure is reported to the outside world via configurable output pins)

2.6.22 System Integration Unit “Lite” (SIUL2)

The SIUL2 controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation. The reset configuration block contains the external pin boot configuration logic. The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU.

The SIUL2 provides the following features:

- Centralized pad control on per pin basis
 - Pin function selection
 - Configurable weak pull-up/down
 - Configurable slew rate control (slow/medium/fast)
 - Hysteresis on GPIO pins
 - Configurable automatic safe mode pad control
- Input filtering for external interrupts with digital glitch filters

2.6.23 Non-Maskable Interrupt (NMI)

The non-maskable interrupt with de-glitching filter is available to support high priority core exceptions.

2.6.24 Boot Assist ROM (BAR)

The BAM is a block of read-only memory. The BAR program is executed only if serial booting mode (as opposed to internal parallel flash booting mode) is selected via boot configuration pins.

The BAM provides the following features:

- Enable booting via serial mode (FlexCAN, LINFlexD-UART)
- Supports user programmable 64-bit password protection for serial boot mode

2.6.25 System Status and Configuration Module (SSCM)

The SSCM on the MPC5744P features the following:

- System configuration and status
- Debug port status and debug port enable
- Multiple boot code starting locations out of reset through implementation of search for valid Reset Configuration Half word
- Detection of user boot code
- Automatic switch to serial boot mode if internal flash is blank or invalid

2.6.26 CAN (FlexCAN)

The FlexCAN module is a communication controller implementing the CAN protocol according to Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth.

The FlexCAN module provides the following features:

- Full implementation of the CAN protocol specification, version 2.0B
 - Standard data and remote frames
 - Extended data and remote frames
 - Zero to eight bytes data length
 - Programmable bit rate up to 1 Mbit/s
- 64 message buffers of zero to eight bytes data length
- Each message buffer configurable as Rx or Tx, all supporting standard and extended messages
- Programmable loop-back mode supporting self-test operation
- 3 programmable mask registers
- Programmable transmit-first scheme: lowest ID or lowest buffer number
- Time Stamp based on 16-bit free-running timer

- Global network time, synchronized by a specific message
- Maskable interrupts
- Independent of the transmission medium (an external transceiver is assumed)
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages
- Transmit features
 - Supports configuration of multiple mailboxes to form message queues of scalable depth
 - Arbitration scheme according to message ID or message buffer number
 - Internal arbitration to guarantee no inner or outer priority inversion
 - Transmit abort procedure and notification
- Receive features
 - Individual programmable filters for each mailbox
 - 8 mailboxes configurable as a 6-entry receive FIFO
 - 8 programmable acceptance filters for receive FIFO
- Programmable clock source
 - System clock
 - Direct oscillator clock to avoid PLL jitter

2.6.27 FlexRay

The FlexRay module provides the following features:

- *FlexRay Communications System Protocol Specification, Version 2.1 Rev A compliant protocol implementation*
- *FlexRay Communications System Electrical Physical Layer Specification, Version 3.0 compliant bus driver interface*
- can be configured for single channel
 - FlexRay Port A can be configured to be connected either to physical FlexRay channel A or physical FlexRay channel B.
- FlexRay bus data rates of 10 Mbit/s, 8 Mbit/s, 5 Mbit/s, and 2.5 Mbit/s supported
- 64 configurable message buffers with
 - individual frame ID filtering
 - individual channel ID filtering
 - individual cycle counter filtering
- message buffer header, status and payload data stored in dedicated flexray memory area
 - allows for flexible and efficient message buffer implementation
 - consistent data access ensured by means of buffer locking scheme
 - application can lock multiple buffers at the same time
- size of message buffer payload data section configurable from 0 up to 254 bytes
- two independent message buffer segments with configurable size of payload data section

Features

- each segment can contain message buffers assigned to the static segment and message buffers assigned to the dynamic segment at the same time
- zero padding for transmit message buffers in static segment
 - applied when the frame payload length exceeds the size of the message buffer data section
- transmit message buffers configurable with state/event semantics
- message buffers can be configured as
 - receive message buffer
 - transmit message buffer
- individual message buffer reconfiguration supported
 - means provided to safely disable individual message buffers
 - disabled message buffers can be reconfigured
- two independent receive FIFOs
 - one receive FIFO per channel
 - up to 255 entries for each FIFO
 - global frame ID filtering, based on both value/mask filters and range filters
 - global channel ID filtering
 - global message ID filtering for the dynamic segment
- 4 configurable slot error counters
- 4 dedicated slot status indicators
 - used to observe slots without using receive message buffers
- measured value indicators for the clock synchronization
 - internal synchronization frame ID and synchronization frame measurement tables can be copied into the flexray memory area
- fractional macroticks are supported for clock correction
- maskable interrupt sources provided via individual and combined interrupt lines
- 1 absolute timer
- 1 timer that can be configured to absolute or relative
- SECDED for protocol engine data RAM
- SEDDED for chip lookup table RAM

2.6.28 Serial Communication Interface (LINFlexD)

The LINFlexD on the MPC5744P has the following features:

- Supports LIN Master mode, LIN Slave mode and UART mode
- LIN state machine compliant to LIN1.3, 2.0 and 2.1 Specifications
- Handles LIN frame transmission and reception without CPU intervention
- LIN features
 - Autonomous LIN frame handling
 - Message buffer to store up to 8 data bytes

- Supports message length of up to 64 bytes
- Detection and flagging of LIN errors (Sync field, delimiter, ID parity, bit framing, checksum and Time-out errors)
- Classic or extended checksum calculation
- Configurable Break duration of up to 36-bit times
- Programmable baud rate prescalers (13-bit mantissa, 4-bit fractional)
- Diagnostic features (Loop back, LIN bus stuck dominant detection)
- Interrupt driven operation with 16 interrupt sources
- LIN slave mode features
 - Autonomous LIN header handling
 - Autonomous LIN response handling
- UART mode
 - Full-duplex operation
 - Standard non return-to-zero (NRZ) mark/space format
 - Data buffers with 4-byte receive, 4-byte transmit
 - Configurable word length (8-bit, 9-bit or 16-bit words)
 - Configurable parity scheme: none, odd, even, always 0
 - Up to 2 Mbit/s
 - Error detection and flagging (Parity, Noise and Framing errors)
 - Interrupt driven operation with 4 interrupts sources
 - Separate transmitter and receiver CPU interrupt sources
 - 16-bit programmable baud-rate modulus counter and 16-bit fractional
 - 2 receiver wake-up methods
- Support for DMA enabled transfers

2.6.29 Serial Peripheral Interface (DSPI)

The serial peripheral interface (DSPI) block provides a synchronous serial interface for communication between the MCU and external devices.

Each DSPI module provides these features:

- Full duplex, synchronous transfers
- Master or slave operation
- Programmable master bit rates
- Programmable clock polarity and phase
- End-of-transmission interrupt flag
- Programmable transfer baud rate
- Programmable data frames from 4 to 16 bits

Features

- Up to 4 chip select lines available, depending on package and pin multiplexing, enabling 16 external devices to be selected using external muxing from a single DSPI
- Four clock and transfer attributes registers
- Chip select strobe available as alternate function on one of the chip select pins for de-glitching
- FIFOs for buffering up to 5 transfers on the transmit and receive side
- Queueing operation possible through use of the I/O processor or eDMA
- General purpose I/O functionality on pins when not used for SPI

2.6.30 FlexPWM

The pulse width modulator module (FlexPWM) contains 4 PWM channels, each of which is set up to control a single half-bridge power stage. There may also be one or more Fault channels. The MPC5744P device uses four-channel PWM. Two modules are instantiated for each variant.

This PWM is capable of controlling most motor types: AC induction motors (ACIM), Permanent Magnet AC motors (PMAC), both brushless (BLDC) and brush DC motors (BDC), switched (SRM) and variable reluctance motors (VRM), and stepper motors.

A FlexPWM module implements the following features:

- 16 bits of resolution for center, edge aligned, and asymmetrical PWMs
- Maximum operating frequency lower than or equal to 160 MHz
 - Clock source not modulated and independent from system clock (generated via auxiliary PLL)
- Fine granularity control for enhanced resolution of the PWM period
- PWM outputs can operate as complimentary pairs or independent channels
- Ability to accept signed numbers for PWM generation
- Independent control of both edges of each PWM output
- Synchronization to external hardware or other PWM supported
- Double buffered PWM registers
 - Integral reload rates from 1 to 16
 - Half cycle reload capability
- Multiple ADC trigger events can be generated per PWM cycle via hardware
- Fault inputs can be assigned to control multiple PWM outputs
- Programmable filters for fault inputs
- Independently programmable PWM output polarity
- Independent top and bottom deadtime insertion
- Each complementary pair can operate with its own PWM frequency and deadtime values
- Individual software-control for each PWM output
- All outputs can be forced to a value simultaneously
- PWMX pin can optionally output a third signal from each channel
- Channels not used for PWM generation can be used for buffered output compare functions

- Channels not used for PWM generation can be used for input capture functions
- Enhanced dual edge capture functionality
- Option to supply the source for each complementary PWM signal pair from any of the following:
 - External digital pin
 - Internal timer channel
 - External ADC input, taking into account values set in ADC high and low limit registers
- DMA support

2.6.31 eTimer

Six 16-bit general purpose up/down timer/counters per module are implemented with the following features:

- Maximum clock frequency 160 MHz
- Individual channel capability
 - Input capture trigger
 - Output compare
 - Double buffer (to capture rising edge and falling edge)
 - Separate prescaler for each counter
 - Selectable clock source
 - 0% - 100% pulse measurement
 - Rotation direction flag (quad decoder mode)
- Maximum count rate
 - Equals peripheral clock/2: for external event counting
 - Equals peripheral clock: for internal clock counting
- Cascadeable counters
- Programmable count modulo
- Quadrature decode capabilities
- Counters can share available input pins
- Count once or repeatedly
- Preloadable counters
- Pins available as GPIO when timer functionality not in use
- DMA support

2.6.32 Sine Wave Generator (SWG)

A customized Digital to Analog converter is available to generate a sine-wave based on 32 stored values for external devices (ex: resolver).

Input clock frequency range: 12–20 MHz

- Output sinusoidal signal:

Features

- Frequency range: 1–50 kHz
- Peak-to-peak amplitude: 0.47–2.26 V

2.6.33 Analog to Digital Converter (ADC)

The ADC module's features are listed below.

Analog part:

- 4 on-chip ADCs
 - 12-bit resolution SAR architecture
 - Same digital interface as in MPC5643L
 - A/D channels:
 - 9 dedicated external channels for ADC0
 - 4 dedicated external channels for ADC1
 - 4 external channels shared between ADC0 and ADC1
 - 5 external channels shared between ADC1 and ADC3
 - 3 external channels shared between ADC2 and ADC3
 - 14 internal channels
 - 1 channel dedicated to each T-sensor to enable temperature reading during application
 - Conversion and sampling compounded time less than 1 μ s (1 MSamples/s)
 - DNL target less than ± 1 LSB (no missing code)
 - INL target less than 2 LSB
 - TUE target less or equal than 6 LSB
 - Gain less than 2 LSB
 - Offset less than 2 LSB
 - 4 analog watchdogs comparing ADC results against predefined levels (low, high, range) before results are stored in the appropriate ADC result location
 - 3.3 V analog power supply
 - 3.3 V / 5.0 V analog input and reference to support high dynamic conversion range
 - 1 sample and hold unit per ADC
 - Sample times of 2 (default), 8, 64, or 128 ADC clock cycles
 - Software selectable presampling

Digital part:

- 4 analog watchdogs comparing ADC results against predefined levels (low, high, range) before results are stored in the appropriate ADC result location
- 2 modes of operation: Motor Control Mode or Regular Mode
- Regular mode features
 - Register based interface with the CPU: 1 result register per channel

- ADC state machine managing 3 request flows: regular command, hardware injected command, software injected command
- Selectable priority between software and hardware injected commands
- 4 analog watchdogs comparing ADC results against predefined levels (low, high, range)
- DMA compatible interface
- Motor control mode features
 - Triggered mode only
 - 4 independent result queues (1x16 entries, 2x8 entries, 1x4 entries)
 - Result alignment circuitry (left justified; right justified)
 - 32-bit read mode allows channel ID on one of the 16-bit parts
 - DMA compatible interfaces
- Built-in self-test

2.6.34 Cross Triggering Unit (CTU)

The ADC cross-triggering unit allows automatic generation of ADC conversion requests on user selected conditions without CPU load during the PWM period and with minimized CPU load for dynamic configuration.

It implements the following features:

- Cross triggering between ADC, FlexPWM, eTimer, and external pins
- Double buffered trigger generation unit with up to 8 independent triggers generated from external triggers
- Maximum operating frequency lower than or equal to 160 MHz
- Trigger generation unit configurable in sequential mode or in triggered mode
- Trigger delay unit to compensate the delay of external low pass filter
- Double buffered global trigger unit allowing eTimer synchronization and/or ADC command generation
- Double buffered ADC command list pointers to minimize ADC-trigger unit update
- Double buffered ADC conversion command list with up to 24 ADC commands
- Each trigger has the capability to generate consecutive commands
- ADC conversion command allows to control ADC channel from each ADC, single or synchronous sampling, independent result queue selection
- DMA support with safety features

2.6.35 CRC Unit

The CRC module is a configurable multiple data flow unit to compute CRC on data written to input register.

Features

The CRC unit has the following features:

- Three sets of registers to allow three concurrent contexts with possibly different CRC computations, each of them with different polynomial and seed
- Computes 8-bit, 16-bit, or 32-bit wide CRC on the fly (single-cycle computation) and stores result in internal register. The following standard CRC polynomials are implemented:
 - $x^8+x^4+x^3+x^2+1$ [for bits CRC7:0 as defined in VDA CAN protocol according to SAEJ1850]

The bit field 28:29 of the register CRC_CFG for each context shall be used to select the polynomial preserving compatibility with previous versions of this IP.
 - $x^{16} + x^{12} + x^5 + 1$ [16-bit CRC-CCITT]
 - $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$ [32-bit CRC-ethernet(32)]
- Key engine to be coupled with communication periphery where CRC application is added to allow implementation of safe communication protocol
- Offloads cycle consuming CRC from core and helps checking configuration signature for safe start-up or periodic procedures
- CRC unit connected as peripheral bus on IP bus
- DMA support

2.6.36 Redundancy Control and Checker Unit (RCCU)

The RCCU checks all outputs of the delayed lock step blocks (addresses, data, control signals). It has the following features:

- Module to guarantee highest possible diagnostic coverage (check of checker)
- Used to check the DMA and core output signals
- Redundancy of the checks by replicated compare units for the ECC encoded signal groups

2.6.37 SENT Receiver

The Single Edge Nibble Transmission (SENT) Receiver module is a multi-channel receiver to receive serial data frames which are being transmitted by a sensor implementing the SENT encoding scheme and present them to the CPU for further processing.

This module is based on the *J2716 Proposed Draft OCT2009 Specification*. As per this specification, the SENT (from <http://www.sae.org>) is intended for use in applications where high resolution sensor data needs to be communicated from a sensor to an MCU. It is intended as a replacement for the lower resolution methods of 10 bit A/D's and PWM and as a simpler low cost alternative to CAN or LIN. The implementation assumes that the sensor is a smart sensor containing a microprocessor or dedicated logic device (ASIC) to create the signal.

2.6.38 Serial Interprocessor Interface (SIPI)

SIPI is an application layer protocol which runs on top of the LFAST module. It is used by the local device to access the shared memory of the remote device. SIPI defines point-to-point communication between two devices, where LFAST works as a physical medium of communication between both the devices. SIPI supports full duplex operation. Address translation for accessing the shared memory of the remote device is out of the scope of SIPI.

SIPI contains an AHB master interface, a DMA interface, and LFAST Tx/Rx interfaces along with IPS interface.

2.6.39 LVDS Fast Asynchronous Serial Transmission (LFAST) Interface

The LFAST module is used to transfer data and control information between two devices (Master and Slave), and is capable of supporting either Dual mode (for example, configurable Master/Slave) or Slave-only mode functionality.

LFAST is a 5-pin interface with the following signals:

- lfast_sysclk
— Reference clock of the LFAST master and slave
- txdatap/txdatan
— Differential transmit (Tx) interface pair
- rxdatap/rxdatan
— Differential receive (Rx) interface pair

An LFAST frame is transmitted/received across the interface. The maximum data rate for Tx/Rx is 320 Mbit/s.

2.6.40 Junction Temperature Sensor

The junction temperature sensor is used by the ADC to measure the temperature of the silicon.

These are the key parameters of the junction temperature sensor:

- Nominal temperature range from -40°C to +150°C
- Accuracy of the sensor after two-temperature calibration targeting +/- 10°C from -40°C to +150°C with an option for extended temperature
- Temperature alarm via analog ADC comparator possible

2.6.41 Nexus Debug Interface (NDI)

The NDI (Nexus Debug Interface) block provides real-time development support capabilities for this Power Architecture-based MCU in compliance with the IEEE-ISTO 5001-2003 standard. This development support is supplied for MCUs without requiring external address and data pins for internal visibility.

Features

The NDI block interfaces to the host processor and internal buses to provide development support as per the IEEE-ISTO 5001-2003 Class 3 + selected features from Class 4 standard.

The development support provided includes program trace, data trace, watchpoint trace, ownership trace, run-time access to the MCUs internal memory map and access to the PowerPC internal registers during halt. The Nexus interface also supports a JTAG only mode using only the JTAG pins. The following features are implemented:

- Support to do data tracing for all AHB masters (FlexRay, DMA)
- Nexus Auxiliary interface in reduced port mode only
 - 1 MCKO (message clock out) pin
 - 4 MDO (message data out) pins
 - 2 $\overline{\text{MSEO}}$ (message start/end out) pins
 - 1 $\overline{\text{RDY}}$ (ready) pin
 - 1 $\overline{\text{EVTO}}$ (event out) pin
 - Auxiliary input port
 - 1 $\overline{\text{EVTI}}$ (event in) pin
- High speed debug interface Nexus Aurora
 - Xilinx Aurora Protocol Specification V2.0 compliant
 - Two transmit-only lanes running at up to 1.25 GHz using LVDS-like signal pairs
 - Receives transmit reference clock from connected tool
- 5-pin JTAG port (JCOMP, TDI, TDO, TMS, and TCK)
 - Supports JTAG mode
- Host processor (e200) development support features
 - Data trace via data write messaging (DWM) and data read messaging (DRM). This allows the development tool to trace reads or writes, or both, to selected internal memory resources.
 - Ownership trace via ownership trace messaging (OTM). OTM facilitates ownership trace by providing visibility of which process ID or operating system task is activated. An ownership trace message is transmitted when a new process/task is activated, allowing development tools to trace ownership flow.
 - Program trace via branch trace messaging (BTM). Branch trace messaging displays program flow discontinuities (direct branches, indirect branches, exceptions, etc.), allowing the development tool to interpolate what transpires between the discontinuities. Thus, static code may be traced.
 - Watchpoint messaging (WPM) via the auxiliary port
 - Watchpoint trigger enable of program and/or data trace messaging
 - Data tracing of instruction fetches via private opcodes

2.6.42 IEEE 1149.1-2001 JTAG Controller (JTAGC)

The JTAGC (JTAG Controller) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. All data input to and output from the JTAGC

block is communicated in serial format. The JTAGC block is compliant with the IEEE 1149.1-2001 standard.

The JTAG controller provides the following features:

- IEEE Test Access Port (TAP) interface 5 pins (TDI, TMS, TCK, TDO, JCOMP)
- Selectable modes of operation include JTAGC/debug or normal system operation
- 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:
 - BYPASS, IDCODE, EXTEST, SAMPLE, SAMPLE/PRELOAD, HIGHZ, CLAMP
- 3 test data registers: a bypass register, a boundary scan register, and a device identification register. The size of the boundary scan register is parameterized to support a variety of boundary scan chain lengths.
- TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry

2.6.43 Power Management Unit (PMU)

The on-chip voltage regulator module provides the following features:

- Single external rail required
- Single high supply required: nominal 3.3 V both for all package options
- Regulator for core voltage
 - Requires external BJT supporting the current
 - Optional, external regulator (LDO), internal regulator not active
- Supply voltage monitoring
 - Several high and low voltage detectors (HVD/LVD) covering a range of voltages
 - Low and high voltage detectors for core supply
 - Low voltage detector for external 3.3 V supplies
 - Disable option for external monitoring, test mode and application stress test
 - Independent disable for core LVD/HVD
 - Can be used as interrupts instead of triggering reset
 - Fine trimming of threshold levels in flash operational state
 - Supports SW based calibration of threshold levels
- Generation of POR
 - Detects external 3.3 V supply
 - Provides hysteresis for rising/falling edge
- Functional Safety
 - Built-in self-test for all LVD and HVD
 - Redundant reference generation for POR and LVD/HVD
 - Supports diagnostics by ADC

2.6.44 Built-in Self-Test (BIST) capability

This device includes the following protection against latent faults:

- Boot-time and shutdown time Memory Built-In Self-Test (MBIST)
- Boot-time and shutdown time scan-based Logic Built-In Self-Test (LBIST)
- Run-time ADC Built-In Self-Test (BIST)
- Run-time Built-In Self Test of LVDs

3 Developer Environment

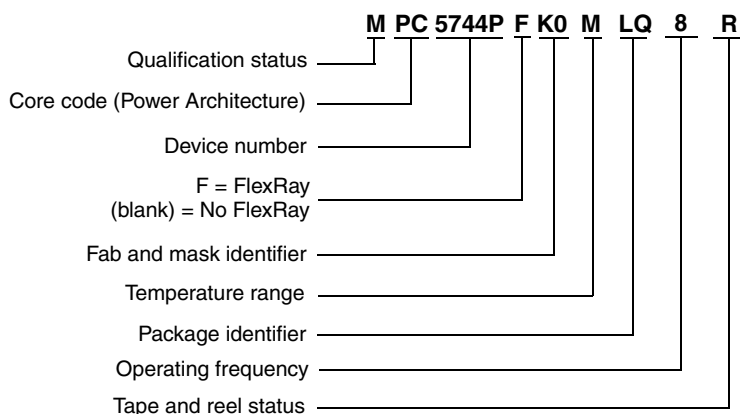
Development tools available to support the product include:

- Automotive evaluation board (EVB) with MPC57xx motherboard and MPC5744P daughter card
- Debug, compile, and build tools
- JTAG and Nexus interfaces

Software and drivers available to support the product include:

- AutoSAR software package
- Flash memory drivers

4 Ordering information



Temperature range	Package identifier	Operating frequency	Qualification status	Tape and reel status
M = -40°C to +125°C	LQ = 144 LQFP	8 = 180 MHz	P = Pre-qualification	R = Tape and reel
K = -40°C to +TBD°C for extended temp (+165°C T _J)	MM = 257 MAPBGA KU = 176 LQFP	5 = 150 MHz	M = Fully spec. qualified, general market flow S = Fully spec. qualified, automotive flow	(blank) = Trays

Note: Not all options are available on all devices. See [Table 5](#).

Table 5. Orderable part number summary

Part number ¹	Flash/SRAM	Package	Other features ²
PPC5744PFK0MLQ8	2.5 MB/384 KB	144 LQFP (Pb free)	–40 to +125 °C
PPC5744PFK0MKU8	2.5 MB/384 KB	176 LQFP exposed pad (Pb free) ³	LFAST interface –40 to +125 °C
PPC5744PFK0MMM8	2.5 MB/384 KB	257 MAPBGA (Pb free)	LFAST interface Nexus Aurora –40 to +125 °C
MPC5743PFK0MLQ8	2 MB/256 KB	144 LQFP (Pb free)	–40 to +125 °C
MPC5743PFK0MMM8	2 MB/256 KB	257 MAPBGA (Pb free)	LFAST interface Nexus Aurora –40 to +125 °C
MPC5742PFK0MLQ8	1.5 MB/192 KB	144 LQFP (Pb free)	–40 to +125 °C
MPC5742PFK0MMM8	1.5 MB/192 KB	257 MAPBGA (Pb free)	LFAST interface Nexus Aurora –40 to +125 °C

NOTES:

- ¹ All packaged devices are PPC, rather than MPC or SPC, until product qualifications are complete. Not all configurations are available in the PPC parts.
- ² The N33E maskset version of the device is limited to a maximum frequency of 180 MHz.
- ³ The 176 LQFP-EP package is not planned to be available with the N33E maskset version of the PPC5744 device. The 176 LQFP-EP package is under consideration, but not committed, for future maskset versions.

5 Document Revision History

Table 6 summarizes updates to the document’s content compared to the previously released version.

Table 6. Revision History

Revision	Location(s)	Substantive Change(s)
Rev. 2	Table 3 on page 11	Updated information about FlexPWM1, supplies, and GPIO
	Section 2.6.33, “Analog to Digital Converter (ADC),” on page 28	Updated details about available ADC channels
	Section 4, “Ordering information,” on page 34	Updated list and format of orderable part numbers as well as information about the 176 LQFP-EP package’s availability
	Throughout document	Updated the name of Freescale’s DigRF module to LFAST module

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