Product Brief

MPC8349EPB
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MPC8349E Integrated Host Processor Product Brief

The MPC8349E PowerQUICC II™ Pro family of integrated communications processors is a next-generation extension to the popular PowerQUICC II line. The MPC8349E PowerQUICC II Pro family, the first of the PowerQUICC II processors based on a system-on-a-chip (SoC) architecture, integrates the enhanced e300 PowerPC™ core and advanced features, such as DDR memory, dual PCI, Gigabit Ethernet, and high-speed USB controllers.

Motorola developed the MPC8349E PowerQUICC II Pro family to provide a cost-effective, highly integrated control processing solution that addresses the emerging needs of networking infrastructure, telecommunications, and other embedded control applications. MPC8349E processors can be used in such applications as Ethernet routers and switches, wireless LAN (WLAN) equipment, network storage, home network appliances, industrial control equipment, copiers, printers, and other imaging systems.

The MPC8349E PowerQUICC II Pro family is based on the e300 SoC platform—making it easier and faster to add or remove functional blocks and develop additional SoC-based family members targeting emerging market requirements. At the heart of the e300 SoC platform is Motorola's e300 PowerPC core. Based on the classic PowerPC instruction set architecture, the e300 core is an enhanced version of the MPC603e PowerPC core used in previous-generation PowerQUICC II processors. Enhancements include twice as much L1 cache (32-Kbyte data cache and 32-Kbyte instruction cache) with integrated parity-checking, and other performance-enhancing features. The e300 core is completely software-compatible with existing MPC603e core-based products.

In addition to the e300 PowerPC core, the SoC platform includes features such as a DDR SDRAM memory controller, dual three-speed 10, 100, 1000 Mbps Ethernet controllers, dual 32-bit/single 64-bit PCI controllers, integrated security engine, USB 2.0 host and device controller, flexible local bus controller, programmable interrupt controller, dual I^2C controllers, 4-channel DMA controller, DUART, serial peripheral interface, general-purpose I/O port, and system timers. The high level of integration in the MPC8349E helps simplify board design and offers significant bandwidth and performance.

This product brief contains the following topics:

Part I Overview

This section provides a high-level overview of the MPC8349E features. Figure 1 shows the major functional units within the MPC8349E.

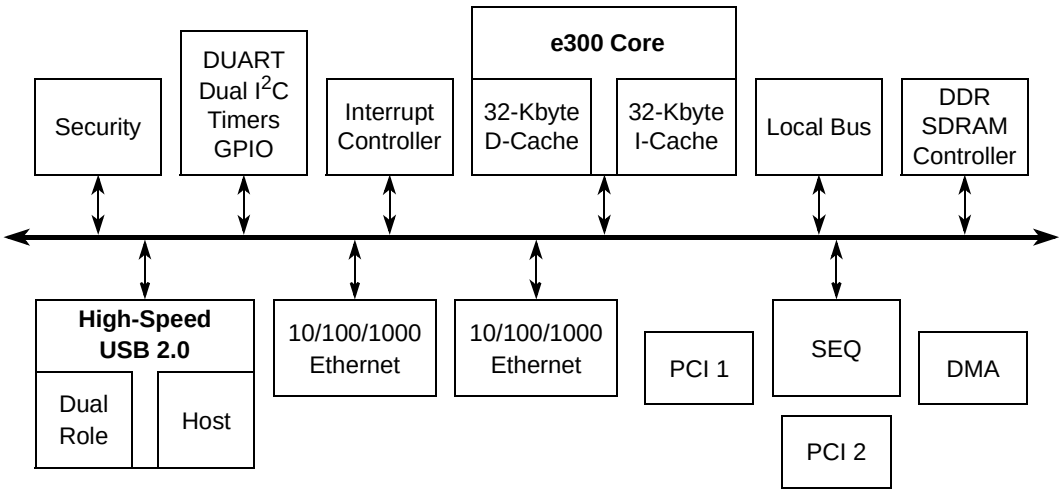

Figure 1. MPC8349E Block Diagram

1.1 Features

Major features of the MPC8349E are as follows:

- e300 PowerPC processor core (enhanced version of the MPC603e core), operates at up to 667 MHz
  - High-performance, superscalar processor core
  - Floating-point, integer, load/store, system register, and branch processing units
  - 32-Kbyte instruction cache, 32-Kbyte data cache
  - Lockable portion of L1 cache
  - Dynamic power management
  - Software-compatible with the Motorola processor families implementing PowerPC
- DDR SDRAM memory controller
  - Programmable timing supporting DDR-1 SDRAM
  - 32- or 64-bit data interface, up to 333 MHz data rate
  - Four banks of memory, each up to 1 Gbyte
  - DRAM chip configurations from 64 Mbits to 1 Gbit with x8/x16 data ports
  - Full ECC support
  - Page mode support (up to 16 simultaneous open pages)
  - Contiguous or discontiguous memory mapping
  - Read-modify-write support
  - Sleep mode support for self refresh SDRAM
  - Supports auto refreshing
  - On-the-fly power management using CKE

  - Registered DIMM support
  - 2.5-V SSTL2 compatible I/O
- Dual three-speed (10/100/1000) Ethernet controllers (TSECs)
  - Dual IEEE 802.3, 802.3u, 820.3x, 802.3z, 802.3 AC compliant controllers
  - Support for different Ethernet physical interfaces:
    - 1000 Mbps IEEE 802.3 GMII/RGMII, 802.3z TBI/RTBI, full-duplex
    - 10/100 Mbps IEEE 802.3 MII full- and half-duplex
  - Buffer descriptors are backwards-compatible with MPC8260 and MPC860T 10/100 programming models
  - 9.6-Kbyte jumbo frame support
  - RMON statistics support
  - Internal 2-Kbyte transmit and 2-Kbyte receive FIFOs per TSEC module
  - MII management interface for control and status
  - Programmable CRC generation and checking
- Dual PCI interfaces
  - PCI Specification Revision 2.2 compatible
  - Data bus widths (2 options):
    - Dual 32-bit data PCI interface that operates at up to 66 MHz
    - Single 64-bit data PCI interface that operates at up to 66 MHz
  - PCI 3.3-V compatible
  - PCI host bridge capabilities on both interfaces
  - PCI agent mode supported on PCI1 interface
  - Support for PCI-to-memory and memory-to-PCI streaming
  - Memory prefetching of PCI read accesses and support for delayed read transactions
  - Support for posting of processor-to-PCI and PCI-to-memory writes
  - On-chip arbitration, supporting five masters on PCI1, three masters on PCI2
  - Support for accesses to all PCI address spaces
  - Parity supported
  - Selectable hardware-enforced coherency
  - Address translation units for address mapping between host and peripheral
  - Dual address cycle support when target
  - Internal configuration registers accessible from PCI
- Security engine is optimized to handle all the algorithms associated with IPSec, SSL/TLS, SRTP, 802.11i, iSCSI, and IKE processing. The security engine contains four crypto-channels, a controller, and a set of crypto execution units (EUs). The execution units are:
  - Public key execution unit (PKEU) supporting the following:
    - RSA and Diffie-Hellman
    - Programmable field size up to 2048 bits
    - Elliptic curve cryptography
    - F2m and F(p) modes
    - Programmable field size up to 511 bits

— Data encryption standard execution unit (DEU)
  – DES, 3DES
  – Two key (K1, K2) or three key (K1, K2, K3)
  – ECB and CBC modes for both DES and 3DES
— Advanced encryption standard unit (AESU)
  – Implements the Rinjdael symmetric key cipher
  – Key lengths of 128, 192, and 256 bits, two key
  – ECB, CBC, CCM, and counter modes
— ARC four execution unit (AFEU)
  – Implements a stream cipher compatible with the RC4 algorithm
  – 40- to 128-bit programmable key
— Message digest execution unit (MDEU)
  – SHA with 160- or 256-bit message digest
  – MD5 with 128-bit message digest
  – HMAC with either algorithm
— Random number generator (RNG)
— Four crypto-channels, each supporting multi-command descriptor chains
  – Static and/or dynamic assignment of crypto-execution units via an integrated controller
  – Buffer size of 256 bytes for each execution unit, with flow control for large data sizes

- Universal serial bus (USB) dual role controller
  — Supports USB on-the-go mode, which includes both device and host functionality
  — Complies with USB Specification Revision 2.0
  — Supports operation as a stand-alone USB device
    – Supports one upstream facing port
    – Supports six programmable USB endpoints
  — Supports operation as a stand-alone USB host controller
    – Supports USB root hub with one downstream-facing port
    – Enhanced host controller interface (EHCI) compatible
  — Supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
  — Supports external PHY with UTMI, serial and UTMI+ low-pin interface (ULPI)
- USB multi-port host controller
  — Supports operation as a stand-alone USB host controller
    – Supports USB root hub with one or two downstream-facing ports
    – Enhanced host controller interface (EHCI) compatible
  — Complies with USB Specification Revision 2.0
  — Supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
  — Supports a direct connection to a high-speed device without an external hub
  — Supports external PHY with serial and low-pin count (ULPI) interfaces
- Local bus controller (LBC)
  — Multiplexed 32-bit address and data operating at up to 133 MHz

  - Four chip selects support four external slaves
  - Up to eight-beat burst transfers
  - 32-, 16-, and 8-bit port sizes are controlled by an on-chip memory controller
  - Three protocol engines available on a per chip select basis:
    - General-purpose chip select machine (GPCM)
    - Three user programmable machines (UPMs)
    - Dedicated single data rate SDRAM controller
  - Parity support
  - Default boot ROM chip select with configurable bus width (8-, 16-, or 32-bit)
- Programmable interrupt controller (PIC)
  - Functional and programming compatibility with the MPC8260 interrupt controller
  - Support for 8 external and 35 internal discrete interrupt sources
  - Support for one external (optional) and seven internal machine checkstop interrupt sources
  - Programmable highest priority request
  - Four groups of interrupts with programmable priority
  - External and internal interrupts directed to host processor
  - Redirects interrupts to external $\overline{\text{INTA}}$ pin when in core disable mode
  - Unique vector number for each interrupt source
- Dual industry-standard I^2C interfaces
  - Two-wire interface
  - Multiple master support
  - Master or slave I^2C mode support
  - On-chip digital filtering rejects spikes on the bus
  - System initialization data is optionally loaded from I^2C-1 EPROM by boot sequencer embedded hardware
- DMA controller
  - Four independent virtual channels
  - Concurrent execution across multiple channels with programmable bandwidth control
  - All channels accessible by local core and remote PCI masters
  - Misaligned transfer capability
  - Data chaining and direct mode
  - Interrupt on completed segment and chain
- DUART
  - Two 4-wire interfaces (RxD, TxD, RTS, CTS)
  - Programming model compatible with the original 16450 UART and the PC16550D
- Serial peripheral interface (SPI)
  - Master or slave support
- General-purpose parallel I/O (GPIO)
  - 64 parallel I/O pins multiplexed on various chip interfaces

- System timers
  - Periodic interrupt timer
  - Real-time clock
  - Software watchdog timer
  - Eight general-purpose timers
- IEEE 1149.1 compliant, JTAG boundary scan
- Integrated PCI bus and SDRAM clock generation

1.2 Functional Differences

Table 1 highlights (in bold) the primary functional differences between the MPC8349E, MPC8347E, and MPC8343E.

Table 1. Functionality of the MPC8349E, MPC8347E, and MPC8343E

Descriptions	MPC8349E	MPC8347E	MPC8343E
L1 I/D cache	32-Kbyte instruction/ 32K data	32-Kbyte instruction/ 32-Kbyte data	32-Kbyte instruction/ 32-Kbyte data
Memory controller	64-/32-bit DDR	64-/32-bit DDR	**32-bit DDR**
Local bus	Yes	Yes	Yes
PCI interface	**Two 32-bit up to 66 MHz or one 64-bit up to 66 MHz**	One 32-bit up to 66 MHz	One 32-bit up to 66 MHz
Ethernet	Two 10/100/1000	Two 10/100/1000	Two 10/100/1000
USB	2.0 host and device	2.0 host and device	**2.0 host or device**
Security	DES/3DES, AES, SH1	DES/3DES, AES, SH1	DES/3DES, AES, SH1
UART	Dual	Dual	Dual
I^2C	Dual	Dual	Dual
SPI	Yes	Yes	Yes
Interrupt controller	Yes	Yes	Yes

Part II MPC8349E Architecture Overview

The following sections describe the major functional units of the MPC8349E.

2.1 PowerPC Core Overview

The MPC8349E PowerQUICC II Pro contains the e300 PowerPC processor core, which is an enhanced version of the MPC603e core (used in previous generations of PowerQUICC II processors). Enhancements include twice as much L1 cache (32-Kbyte data cache and 32-Kbyte instruction cache) with integrated parity-checking and other performance-enhancing features. The e300 core is completely software-compatible with existing MPC603e core-based products.

For detailed information regarding the processor core refer to the following:

- The *G2 PowerPCCore Reference Manual* (chapters describing the programming model, cache model, memory management model, exception model, and instruction timing)
- The *Programming Environments Manual*

This section is an overview of the processor core, provides a block diagram showing the major functional units, and describes briefly how those units interact.

The processor core is a low-power implementation of the family of microprocessors that implement the PowerPC architecture. The processor core implements the 32-bit portion of the PowerPC architecture, which provides 32-bit effective addresses, integer data types of 8, 16, and 32 bits, and floating-point data types of 32 and 64 bits.

The processor core is a superscalar processor that can issue and retire as many as three instructions per clock. Instructions can execute out of order for increased performance, however, the processor core makes completion appear sequential.

The processor core integrates five execution units—an integer unit (IU), a floating-point unit (FPU), a branch processing unit (BPU), a load/store unit (LSU), and a system register unit (SRU). The ability to execute five instructions in parallel and the use of simple instructions with rapid execution times yield high efficiency and throughput. Most integer instructions execute in one clock cycle. On the processor core, the FPU is pipelined so a single-precision multiply-add instruction can be issued and completed every clock cycle.

The processor core supports integer data types of 8, 16, and 32 bits, and floating-point data types of 32 and 64 bits.

The processor core provides independent on-chip, 32-Kbyte, eight-way set-associative, physically-addressed instruction and data caches. The processor also features independent on-chip instruction and data memory management units (MMUs). The MMUs contain 64-entry, two-way set-associative, data and instruction translation lookaside buffers (DTLB and ITLB) that provide support for demand-paged virtual memory address translation and variable-sized block translation. The TLBs and caches use a least recently used (LRU) replacement algorithm. The processor also supports block address translation through the use of two independent instruction and data block address translation (IBAT and DBAT) arrays of eight entries each. Effective addresses are compared simultaneously with all eight entries in the BAT array during block translation. In accordance with the PowerPC architecture, if an effective address hits in both the TLB and BAT array, the BAT translation takes priority.

As an added feature to the processor core, the MPC8349E can lock the contents of one to all ways in the instruction and data cache (or an entire cache). For example, this allows embedded applications to lock interrupt routines or other important (time-sensitive) instruction sequences into the instruction cache. It allows data to be locked into the data cache, which may be important to code that must have deterministic execution.

The processor core has a 64-bit data bus and a 32-bit address bus. The processor core supports single-beat and burst data transfers for memory accesses, and memory-mapped I/O operations.

Figure 2 provides a block diagram of the MPC8349E processor core that shows how the execution units (IU, FPU, BPU, LSU, and SRU) operate independently and in parallel. Note that this is a conceptual diagram and does not attempt to show how these features are physically implemented on the chip.

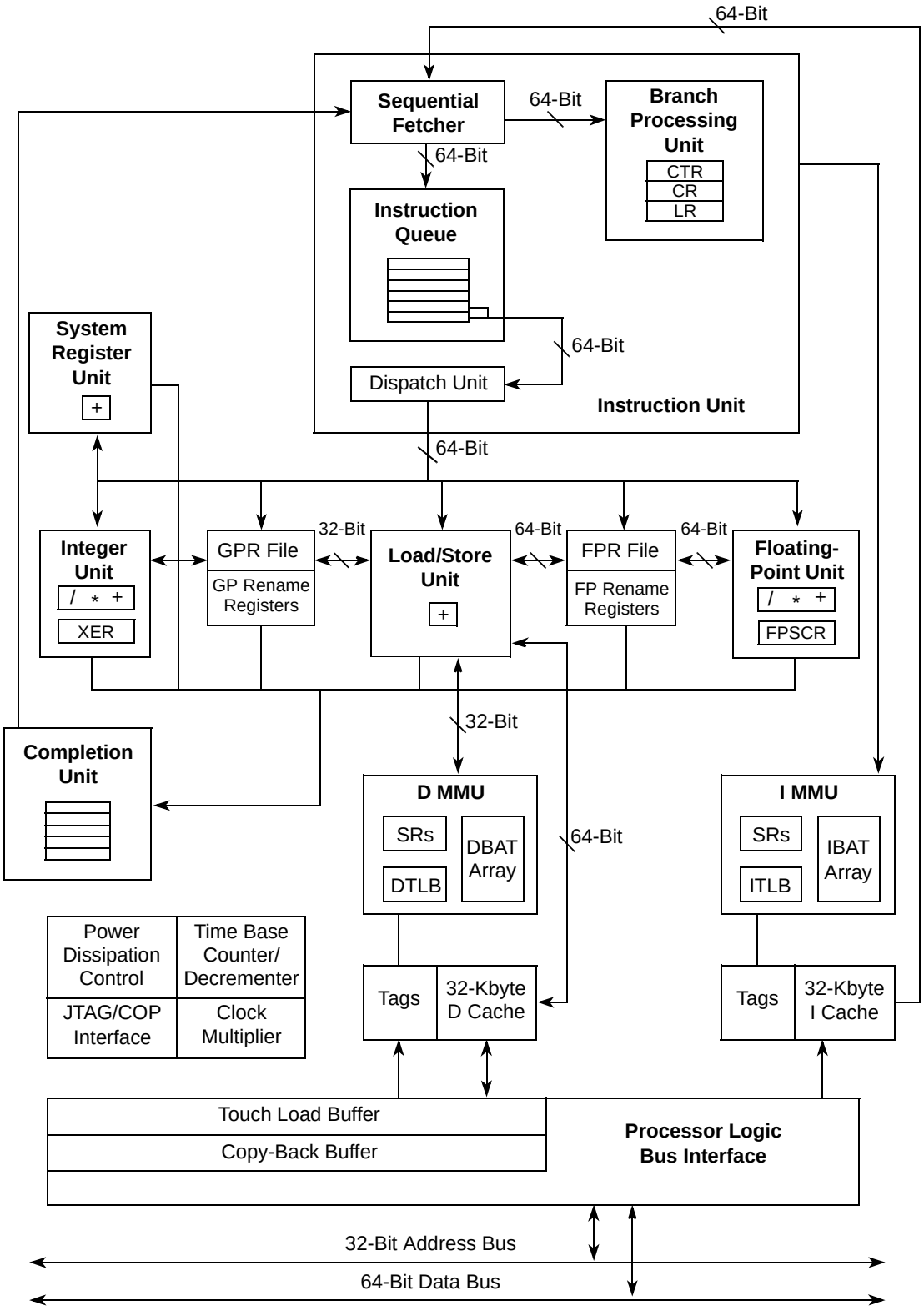

Figure 2. MPC8349E Integrated Processor Core Block Diagram

2.2 DDR Memory Controller

This fully programmable DDR SDRAM controller supports most JEDEC standard x8 or x16 DDR memories available today, including buffered and unbuffered DIMMs. However, mixing nonregistered and registered DIMMs in the same system is not supported. The built-in error checking and correction (ECC) ensures very low bit-error rates for reliable high-frequency operation. Dynamic power management and auto-precharge modes simplify memory system design. A large set of special features like DLL software override, crawl mode, and ECC error injection support rapid system debug.

The MPC8349E DDR memory controller includes the following distinctive features:

- Supports for DDR SDRAM
- 32-/40-bit and 64/72-bit SDRAM data bus
- Programmable settings for meeting all SDRAM timing parameters
- Many different SDRAM configurations supported
  - Support for as many as four physical banks (chip selects), each bank independently addressable
  - Support for 64-Mbit to 1-Gbit devices with x8 or x16 data ports (no direct x4 support)
  - Support for unbuffered and registered DIMMs
- Support for data mask signals and read-modify-write for sub-double word writes
- Support for double-bit error detection and single-bit error correction ECC (8-bit check word across 64- or 32-bit data when in 32-bit mode)
- Two-entry input request queue
- Open page management (dedicated entry for each sub-bank)
- Memory controller clock frequency of two times the SDRAM clock with support for sleep power management mode
- Support for error injection on ECC

2.3 Dual Three-Speed Ethernet Controllers

The three-speed Ethernet controllers (TSECs) are designed to support 10/100 Ethernet to 1000 Mbps, or 1 Gbps IEEE 802.3 protocol. The Ethernet IEEE 802.3 protocol is a widely used LAN, based on the carrier-sense multiple access/collision detect (CSMA/CD) approach. Because Ethernet and IEEE 802.3 protocols are similar and can coexist on the same LAN, 10/100 Ethernet provides increased Ethernet speed from 10 to 100 Mbps and provides a simple, cost-effective option for backbone and server connectivity. The standard implemented TSEC in the MPC8349E is Gigabit Ethernet, which builds on top of the Ethernet protocol, but increases speed tenfold over 10/100 Ethernet to 1000 Mbps, or 1 Gbps.

The MPC8349E TSECs include these distinctive features:

- Ethernet media access controller (MAC)
- First-in first-out (FIFO) controller
- Direct memory access (DMA) controller
- Ten-bit interface (TBI)
- Register-based statistical module that supports management information base (MIB) remote monitoring (RMON)

The most significant byte of data in a receive or transmit data buffer corresponds to the most significant byte of a frame, respectively.

The complete TSEC is designed for single MAC applications. The TSECs support several standard MAC-PHY interfaces to connect to an external Ethernet transceiver:

- MII interface running at 10/100 Mbps
- GMII interface running at 1000 Mbps
- TBI interface that can be connected to a SerDes device for fibre channel applications.
- Reduced pin count versions of the GMII (RGMII) and ten-bit (RTBI) interfaces

The TSEC software programming model is similar to the MPC8260 (PowerQUICC II) device. Hence, it enables Motorola customers to leverage already implemented Ethernet drivers, reducing the software development cycle.

2.4 PCI Controllers

The MPC8349E 32-/64-bit PCI controllers are compatible with the *PCI Local Bus Specification, Rev. 2.2*. Both PCI1 and PCI2 interfaces can function as a host bridge interface. PCI1 interface can optionally function as an agent device. Both PCI controllers supports 32-bit addressing and 32-bit data buses. PCI1 controller also supports a 64-bit data bus.

As a master, the MPC8349E supports read and write operations to the PCI memory space, the PCI I/O space, and the PCI configuration space. Also, the MPC8349E can generate PCI special-cycle and interrupt acknowledge commands. As a target, the MPC8349E supports read and write operations to system memory, as well as PCI configuration space and the on-chip memory mapped configuration space.

The MPC8349E PCI controller includes the following distinctive features:

- Address stepping on configuration transaction
- Fast back-to-back
- Data streaming
- When in host mode, the PCI controllers support external signals isolation, thus enable shut off power to external devices

2.5 PCI Bus Arbitration Unit

The MPC8349E PCI controllers each contain a PCI bus arbitration unit, which eliminates the need for an external unit, thus lowering system complexity and cost. It has the following features:

- PCI1 supports five $\overline{\text{REQ}}$/$\overline{\text{GNT}}$ signal pairs, thus supporting five external masters. The MPC8349E PCI1 controller is the sixth member of the arbitration pool.
- PCI2 supports three $\overline{\text{REQ}}$/$\overline{\text{GNT}}$ signal pairs, thus supporting three external masters. The MPC8349E PCI1 controller is the fourth member of the arbitration pool.
- The bus arbitration unit allows fairness as well as a priority mechanism.
- A two-level round-robin scheme is used in which each device can be programmed within a pool of a high- or low-priority arbitration. One member of the low-priority pool is promoted to the high-priority pool. As soon as it is granted the bus, it returns to the low-priority pool.
- The unit can be disabled to allow a remote arbitration unit to be used.
- The unit can be isolated to allow power shut off of external devices.

2.6 Security Engine

A hardware encryption block is also integrated in the MPC8349E. It supports many different encryption algorithms allowing for high performance data encryption and authentication as required in today's SOHO/ROBO routers. The encryption block is compatible with the block in the MPC8280.

It supports DES, 3DES, MD-5, SHA-1, AES, PKEU, RNG, and RC-4 encryption algorithms in hardware.

A block diagram of the security engine's internal architecture is shown in Figure 3. The bus interface module is designed to transfer 64-bit words between the internal bus and any register inside the security engine.

An operation begins with a write of a pointer to a crypto-channel fetch register which points to a data packet descriptor. The channel requests the descriptor and decodes the operation to be performed. The channel then requests the controller to assign crypto execution units and fetch the keys, IVs, and data needed to perform the given operation. The controller satisfies the requests by assigning execution units to the channel and by making requests to the master interface. As data is processed, it is written to the individual execution unit's output buffer and then back to system memory via the bus interface module.

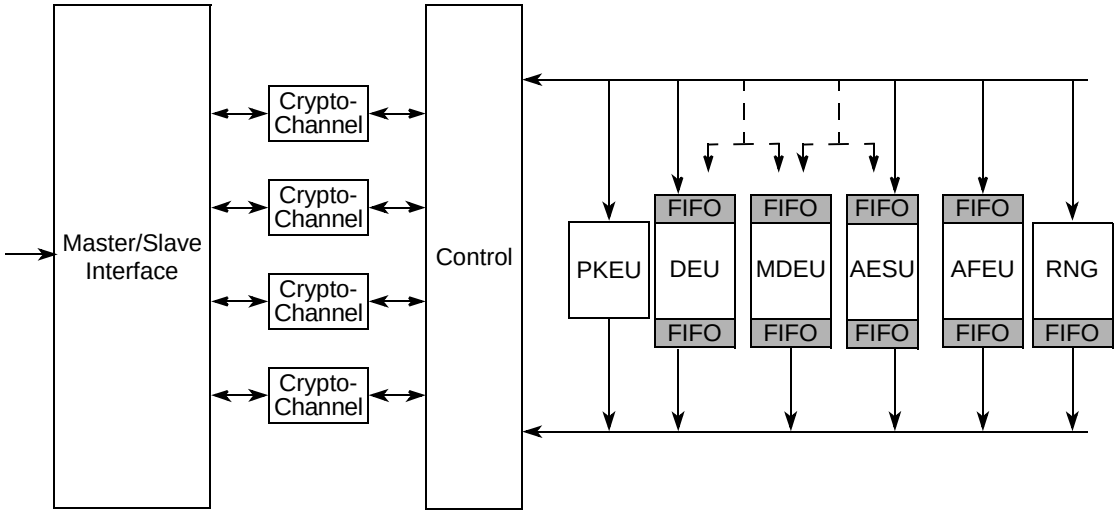

Figure 3. Integrated Security Engine Functional Blocks

2.7 Universal Serial Bus (USB) 2.0

The MPC8349E USB 2.0 controller offers simultaneous operation of host and device. The USB host and device controllers provide point-to-point connectivity which complies with the USB Specification, Rev. 2.0. It also allows the host and device functions to co-exist and operate simultaneously. The USB controllers can be configured to operate as a stand-alone host, stand-alone device, dual hosts, or both host and device functions that are operating simultaneously. See Figure 4 for more information.

The host and device functions are both configured to support the following four types of USB transfers:

- Bulk
- Control
- Interrupt
- Isochronous

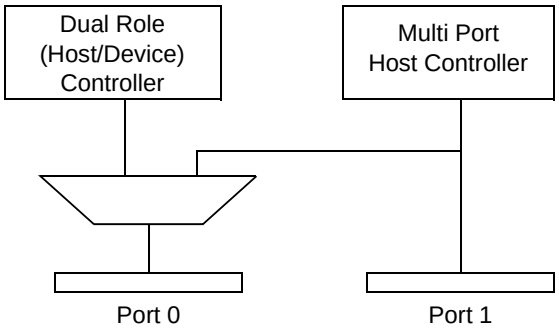

Figure 4. USB Configuration Block Diagram

2.7.1 USB Dual-Role Controller

- Supports USB on-the-go mode, which includes both device and host functionality
- Complies with USB Specification, Rev. 2.0
- Supports operation as a stand-alone USB device
  - — Supports one upstream facing port
  - — Supports six programmable USB endpoints
- Supports operation as a stand-alone USB host controller
  - — Supports USB root hub with one downstream-facing port
  - — Enhanced host controller interface (EHCI) compatible
- Supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
- Supports external PHY with UTMI, serial and UTMI+ low-pin interface (ULPI)

2.7.2 USB Multi-Port Host Controller

- Supports operation as a stand-alone USB host controller
  - — Supports USB root hub with one or two downstream-facing port
  - — Enhanced host controller interface (EHCI) compatible
- Complies with USB Specification, Rev. 2.0
- Supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
- Supports a direct connection to a high-speed device without an external hub
- Supports external PHY with serial and low-pin count (ULPI) interfaces

2.8 Local Bus Controller

The main component of the local bus controller (LBC) is its memory controller which provides a seamless interface to many types of memory devices and peripherals. The memory controller is responsible for controlling four memory banks shared by a high performance SDRAM machine, a general-purpose chip-select machine (GPCM), and up to three user-programmable machines (UPMs). As such, it supports a minimal glue logic interface to synchronous DRAM (SDRAM), SRAM, EPROM, Flash EPROM, burstable RAM, and other peripherals. The LBC external address latch enable (LALE) signal allows multiplexing of addresses with data signals to reduce the device pin count.

The local bus controller also includes a number of data checking and protection features such as data parity generation and checking, write protection and a bus monitor to ensure that each bus cycle is terminated within a user-specified period.

The main features of the local bus controller are as follows:

- Memory controller with four memory banks
  - 32-bit address decoding with mask
  - Variable memory block sizes (32 Kbytes to 2 Gbytes)
  - Selection of control signal generation on a per-bank basis
  - Data buffer controls activated on a per-bank basis
  - Odd/even parity checking including read-modify-write (RMW) parity for single accesses
  - Write-protection capability
  - Parity byte-select
- Synchronous DRAM (SDRAM) machine
  - Provides the control functions and signals for glueless connection to JEDEC-compliant SDRAM devices
  - Supports up to four concurrent open pages
  - Supports SDRAM port size of 32-, 16-, and 8-bit
  - Supports external address and/or command lines buffering
- General-purpose chip-select machine (GPCM)
  - Compatible with SRAM, EPROM, FEPROM, and peripherals
  - Global (boot) chip-select available at system reset
  - Boot chip-select support for 8-, 16-, and 32-bit devices
  - Minimum three-clock access to external devices
  - Four byte-write-enable signals ($\overline{\text{LWE}}$[0:3])
  - Output enable signal ($\overline{\text{LOE}}$)
  - External access termination signal ($\overline{\text{LGTA}}$)
- Three user-programmable machines (UPMs)
  - Programmable-array-based machine controls external signal timing with a granularity of up to one quarter of an external bus clock period
  - User-specified control-signal patterns run when an internal master requests a single-beat or burst read or write access
  - User-specified control-signal patterns can be initiated by software
  - Support for 8-, 16-, and 32-bit devices
  - Page mode support for successive transfers within a burst
- Support for delay locked loop (DLL) with software-configurable bypass for low frequency bus clocks

2.9 Programmable Interrupt Controller (PIC)

The programmable interrupt controller (PIC) implements the necessary functions to provide a flexible solution for a general-purpose interrupt control. The PIC includes the following features:

- Functional and programming models are compatible with the MPC8260 interrupt controller
- Support for 8 external and 35 internal discrete interrupt sources
- Support for one external (optional) and seven internal machine checkstop interrupt sources
- Programmable highest priority request
- Two programmable priority mixed groups of four on-chip and four external interrupt signals with two priority schemes for each group: grouped and spread
- Two programmable priority internal groups of eight on-chip interrupt signals with two priority schemes for each group: grouped and spread
- Priority interrupts can be programmed to support a critical ($\overline{cint}$) or system management ($\overline{smi}$) interrupt type
- External and internal interrupts directed to a host processor
- Unique vector number for each interrupt source
- Redirect interrupts to external $\overline{\text{INTA}}$ pin when in core disable mode

2.10 Dual I^{2}C Interfaces

The inter-IC (IIC or I^{2}C) bus is a two-wire—serial data (SDA) and serial clock (SCL)— bidirectional serial bus that provides a simple, efficient method of data exchange between the system and other devices, such as microcontrollers, EEPROMs, real-time clock devices, A/D converters, and LCDs. The two-wire bus minimizes the interconnections between devices. The synchronous, multi-master bus of the I^{2}C allows the connection of additional devices to the bus for expansion and system development.

The I^{2}C controller is a true multimaster bus which includes collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously. This feature allows for complex applications with multiprocessor control. The I^{2}C controller consists of a transmitter/receiver unit, clocking unit, and control unit. The I^{2}C unit supports general broadcast mode and on-chip filtering rejects spikes on the bus.

The I^{2}C interface includes the following features:

- Two-wire interface
- Multi-master operational
- Arbitration lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- START and STOP signal generation/detection
- Acknowledge bit generation/detection
- Bus busy detection
- Software-programmable clock frequency
- Software-selectable acknowledge bit
- On-chip filtering for spikes on the bus

- Address broadcasting supported
- System initialization data is optionally loaded from I^2C-1 EPROM by boot sequencer embedded hardware

2.11 DMA Controller

The MPC8349E DMA engine is capable of transferring blocks of data from any legal address range to any other legal address range. Therefore, it can perform a DMA transfer between any of its I/O or memory ports or even between two devices or locations on the same port.

The DMA controller offers the following features:

- Four high-speed/high-bandwidth channels accessible by local and remote masters
- Basic DMA operation modes (direct, simple chaining)
- Misaligned transfers
- Programmable bandwidth control between channels
- Interrupt on error and completed segment or chain

2.12 Dual Universal Asynchronous Receiver/Transmitter (DUART)

The MPC8349E includes a DUART intended for use in maintenance, bring up, and debug systems. The MPC8349E provides a standard four-wire handshake (TXD, RXD, RTS, CTS) for each port. The DUART is a slave interface. An interrupt is provided to the interrupt controller or optionally steered externally to allow device handshakes. Interrupts are generated for transmit, receive, and line status.

The MPC8349E DUART supports full-duplex operation. It is compatible with the PC16450 and PC16550 programming models. The transmitter and receiver both support 16-byte FIFOs.

Software programmable baud generators divide the system clock to generate a 16x clock. Serial interface data formats (data length, parity, 1/1.5/2 STOP bit, baud rate) are also software selectable.

The DUART includes the following distinctive features:

- Full-duplex operation
- Programming model compatible with the original PC16450 UART and the PC16550D (an improved version of the PC16450 that also operates in FIFO mode)
- PC16450 register reset values
- FIFO mode for both transmitter and receiver, providing 16-byte FIFOs
- Serial data encapsulation and decapsulation with standard asynchronous communication bits (START, STOP, and parity)
- Maskable transmit, receive, and line status interrupts
- Software-programmable baud generators that divide the system clock by 1 to $(2^{16} - 1)$ and generate a 16x clock for the transmitter and receiver engines
- Clear to send ($\overline{\text{CTS}}$) and ready to send ($\overline{\text{RTS}}$) MODEM control functions
- Software-selectable serial-interface data format (data length, parity, 1/1.5/2 STOP bit, baud rate)
- Line status registers
- Line-break detection and generation

- Internal diagnostic support, local loopback, and break functions
- Prioritized interrupt reporting
- Overrun, parity, and framing error detection

2.13 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) allows the MPC8349E to exchange data between other PowerQUICC family chips, Ethernet PHYs for configuration, and peripheral devices such as EEPROMs, real-time clocks, A/D converters, and ISDN devices.

The SPI is a full-duplex, synchronous, character-oriented channel that supports a four-wire interface (receive, transmit, clock, and slave select). The SPI block consists of transmitter and receiver sections, an independent baud-rate generator, and a control unit.

2.14 System Timers

The MPC8349E includes a number of timers. The MPC8349E system timers include the following distinctive features:

- Periodic interrupt timer
  - Maintains a 32-bit down-counter, clocked by a 16-bit prescaled input clock
  - Provides programmable and maskable ‘periodic’ interrupt
  - Provides a maximum period of about 10 days (at 333 MHz)
  - Use two possible clock sources:
    - Internal system bus clock
    - External PIT clock
  - PIT function can be disabled if needed
- Real time clock
  - Maintains a one-second count, unique over a period of about 68 years
  - 32-bit RTC counter
  - Provides an ‘alarm’ function with programmable and maskable ‘alarm’ interrupt
  - Provides programmable and maskable ‘every second’ interrupt
  - Use two possible clock sources: an internal bus or an external RTC clock
  - RTC function can be disabled if needed
- Software watchdog timer
  - Based on a 16-bit prescaler and a 16-bit down-counter
  - Provides a selectable range for the time-out period
  - Provide about 12.8 seconds maximum software time-out delay for 333 MHz input clock
  - Functional and programming compatibility with MPC8260 watchdog timer
- Two general-purpose timer blocks, each supports the following features:
  - Maximum input clock is the system bus clock
  - Four 16-bit programmable timers, two cascaded 32-bit timers, or one cascaded 64-bit counter
  - Three programmable input clock sources for the timer prescalers
  - Input capture capability

— Optionally generate pulse on output pin when count equals to reference
— Free run and restart modes
— Functional and programming compatibility with MPC8260 timers

2.15 MPC8349E Applications

The MPC8349E can be used for control processing in applications such as wireless LAN, routers/switches, line cards, embedded computing, multi-channel modems, network storage, image display systems, enterprise I/O processor, internet access device (IAD), disk controller for RAID systems, and copier/printer board control.

Part III Document Revision History

Table 2 provides a revision history for this product brief.

Table 2. Document Revision History

Rev. No.	Date	Substantive Change(s)
0	3/31/2004	Initial release under NDA.
1	4/26/2004	Published on the web.

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JAPAN:

Motorola Japan Ltd.
SPS, Technical Information Center
3-20-1, Minami-Azabu Minato-ku
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81-3-3440-3569

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852-26668334

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