Freescale Semiconductor
Product Brief

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MPC8536E Integrated Processor Product Brief

The MPC8536E is a new low-power, high-performance member of the PowerQUICC III™ processor family that combines a computation-intensive super-scalar Power Architecture™ processor core with high-performance system peripherals and advanced power management techniques to deliver high-performance computing in low-power envelopes required for imaging, communications, and industrial applications.

The integration of vector and double-precision floating point processing engines makes the MPC8536E ideal for mathematically intensive applications such as printing, imaging, and industrial computing. The MPC8536E is optimized for control and data plane intensive processing applications such as routers, wireless base-stations, switches, and storage networks, where the benefits of processing and moving large amounts of data can be leveraged. MPC8536E integrates SATA, USB, multi-lane PCI Express, Gigabit Ethernet, and DDR memory to increase data bandwidths, reduce valuable board real estate, and lower overall power consumption. Jog mode, in which core frequency is dynamically adjustable, further optimizes power consumption.

Contents

1 Application Examples

The MPC8536E is a very flexible device and can be configured to meet many system application needs. The following section provides block diagrams of various applications.

1.1 Multi-Function Printer

Figure 1 illustrates how the MPC8536E can be incorporated in a high-speed color printer application. In this application, the CPU interfaces to the print and scan ASIC through the PCI Express interfaces. Image data from the scanner, fax, or network is processed by CPU and the math accelerators on the MPC8536E before being sent to the printer engine. High-speed color processing and concurrency of application in MFP systems require the higher processor performance and fast data movement provided by MPC8536E in order to manipulate large, high-quality images at high speeds. The MPC8536E implements advanced power management methods to minimize power consumption.

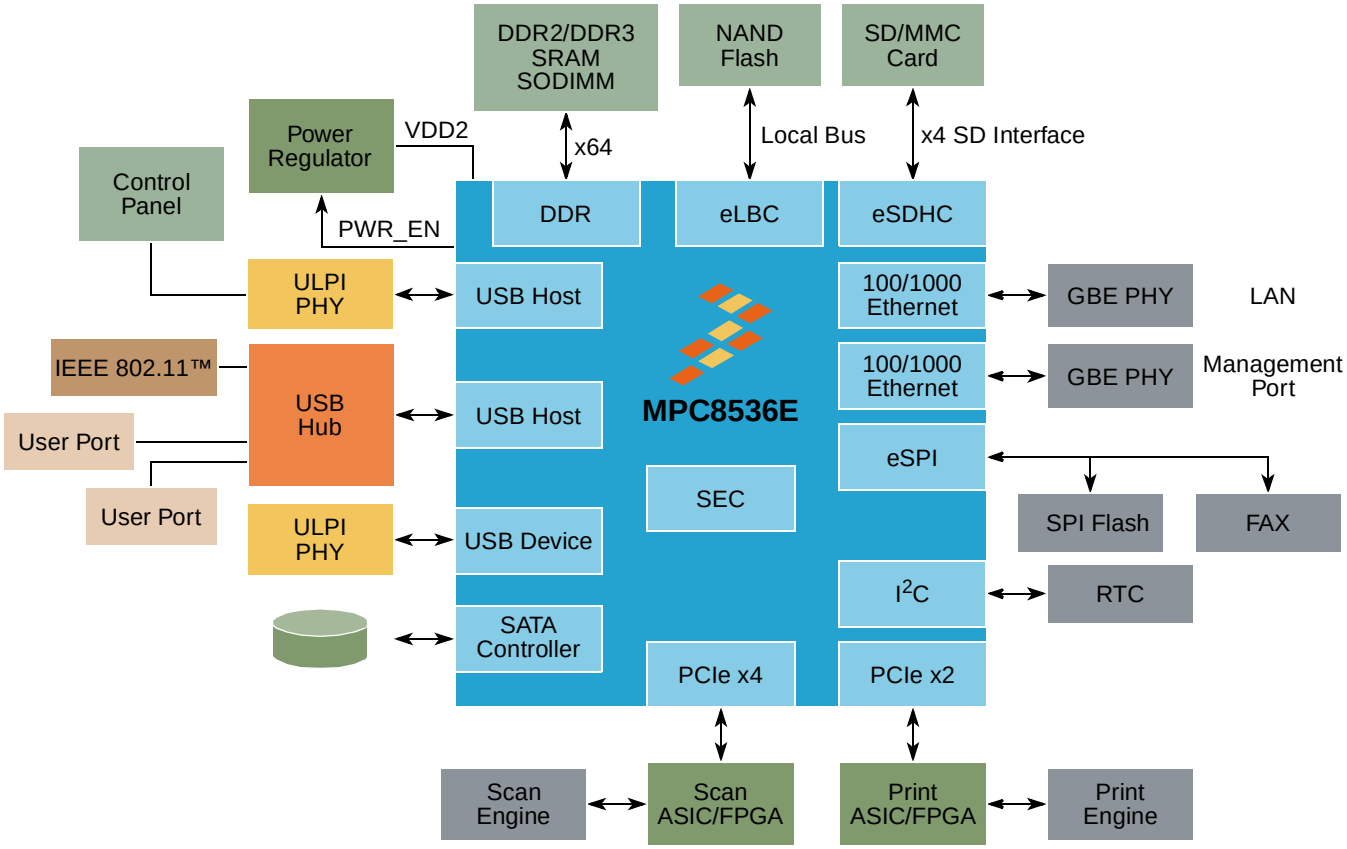

Figure 1. Multi-Function Printer Application

1.2 Network Attached Storage

Figure 2 illustrates how a network attached storage application can be realized with the MPC8536E. In this application, the MPC8536E PCI Express can be configured for high-speed, 8 lane configuration, which can support high-data-rate RAID interfaces. For network connectivity, dual Gigabit Ethernet controllers provide high bandwidth to the storage medium. The security engine provides acceleration for IPSec as well as XOR acceleration for RAID parity calculations, and CRC32C digest calculations for iSCSI applications. The platform also supports battery back-up for data protection in the event of power loss.

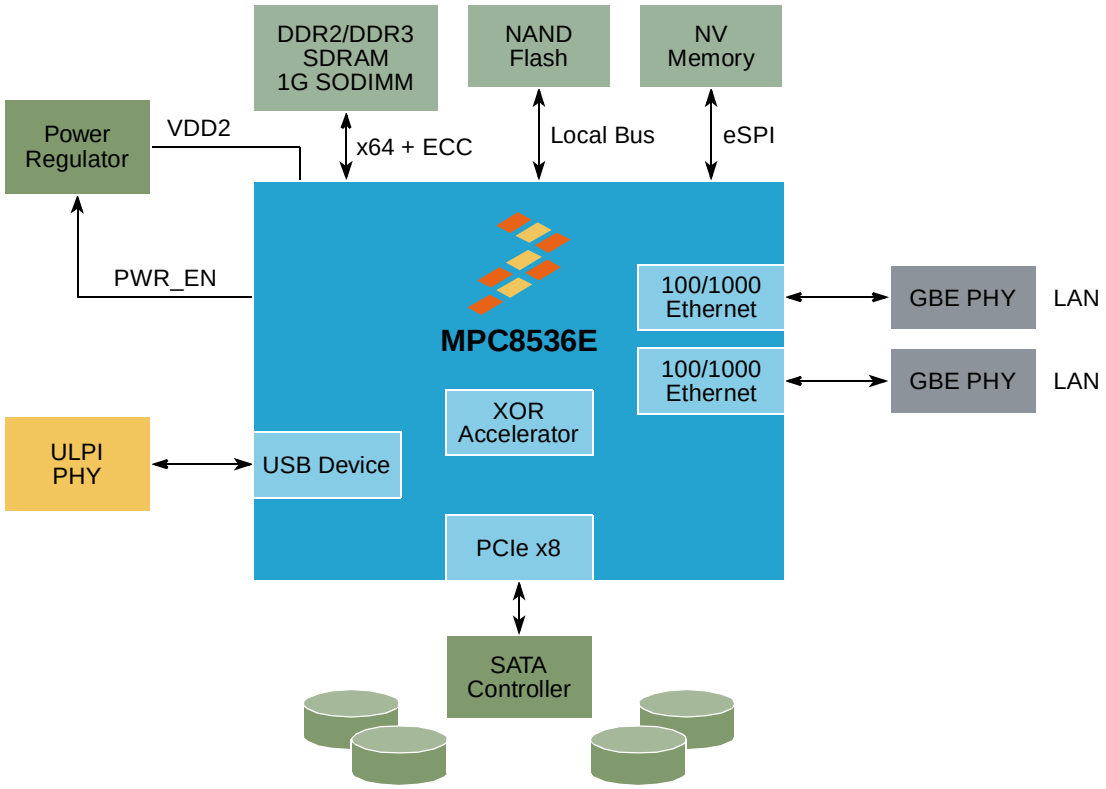

Figure 2. Network Attached Storage Application

1.3 Gaming Kiosk

Figure 3 illustrates a highly integrated implementation of the MPC8536E in a gaming and information kiosk application. Gaming systems require fast responsive controls and vibrant graphics processing. MPC8536E PCI Express provides the high bandwidth interface to transfer graphics image data and control to the graphics processor. Gaming systems are mechanically secure and require low-power operation. MPC8536E GHz performance in low-power envelopes provides the mechanism for the designer to create high performance in a fanless system.

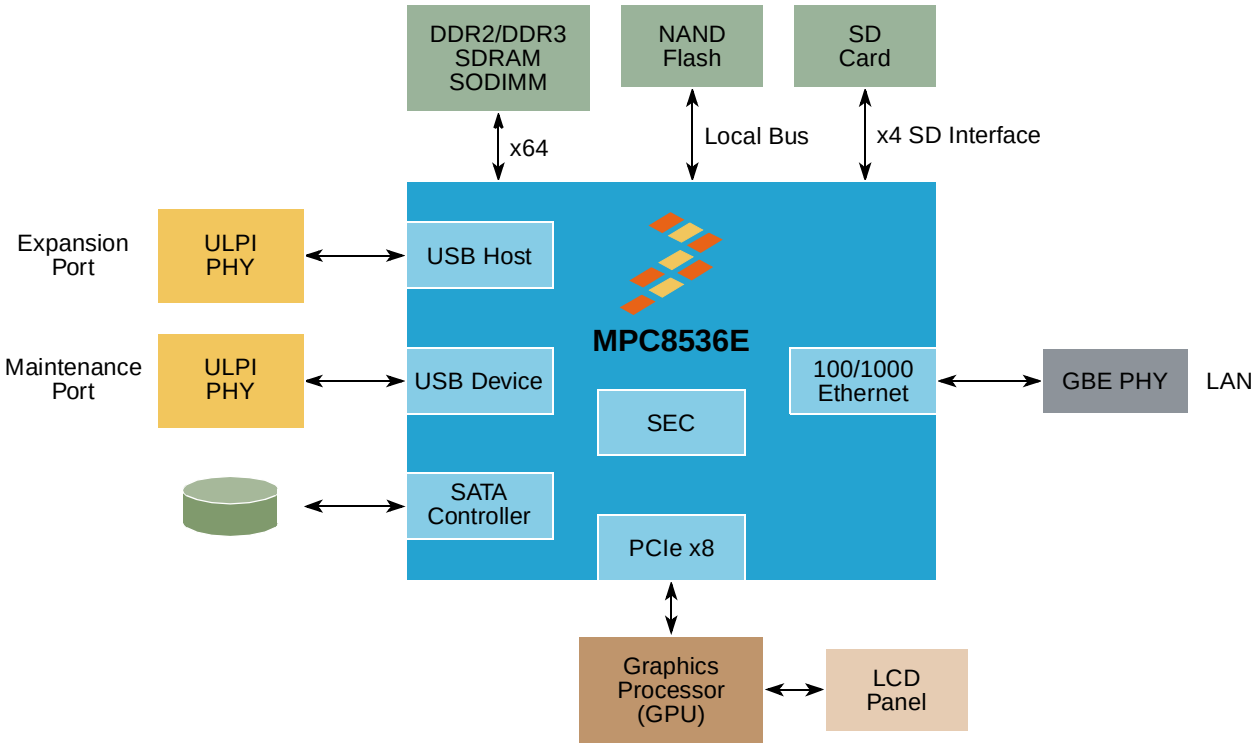

Figure 3. Gaming Kiosk Application

1.4 Network Controller

Figure 4 illustrates how a network controller application can be realized with the MPC8536E. One of the Gigabit Ethernet controllers can be used to interface to an Ethernet switch while the other two provide redundant connectivity to the system back plane. The Ethernet interfaces allow the option for SGMII, which provide robust low-power connectivity to PHY devices. MPC8536E also implements IEEE 1588™ standard for network synchronization.

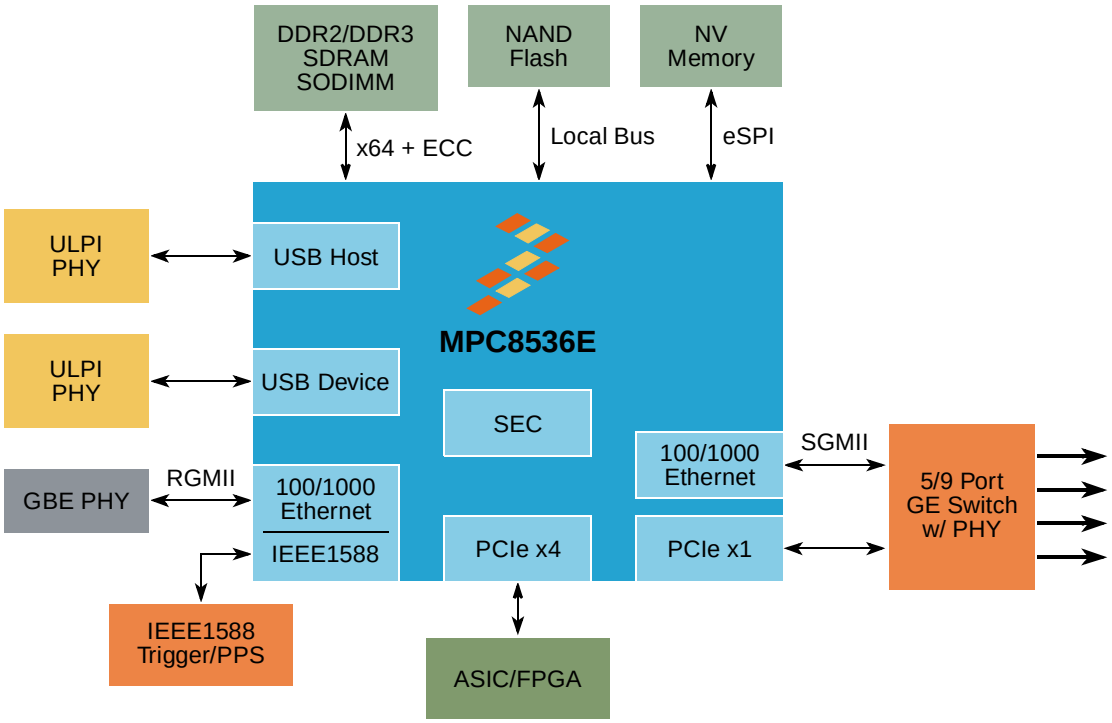

Figure 4. Network Controller Application

2 Features

This section describes features of the MPC8536E.

2.1 Block Diagram

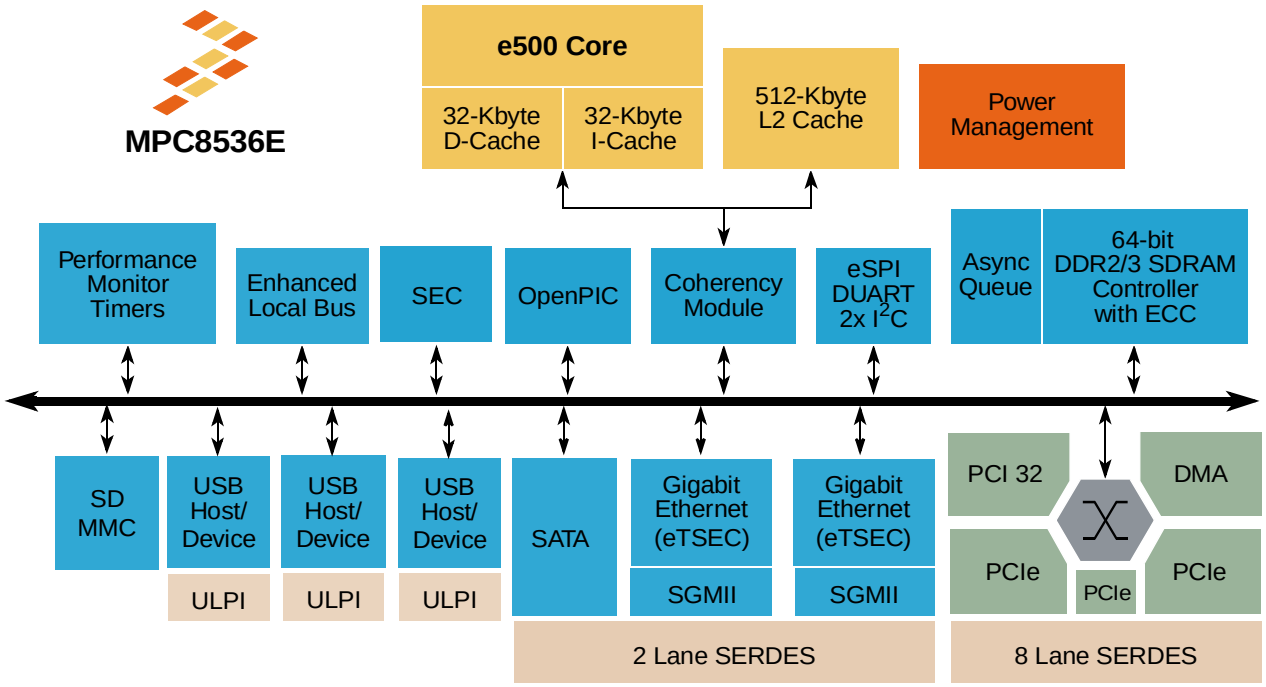

Figure 5. MPC8536E Block Diagram

2.2 Critical Performance Parameters

- Maximum e500 core frequency of 1.5 GHz
- Maximum memory bus frequency of 333 MHz for DDR2 and DDR3 (667-MHz data rate)
- Supply voltages:
  - Core: 1.0–1.1 V
  - Platform/SerDes: 1.0 V
  - PCI: 3.3 V
  - Ethernet: 2.5 V or 3.3 V (subject to protocol)
  - Enhanced local bus: 1.8 V, 2.5 V, 3.3 V
  - DDR: 1.8 V for DDR2, 1.5 V for DDR3 (conforms to JEDEC standard)
- Operating junction temperature range is 0–95° C
- Package: 783-pin FC PBGA (flip-chip plastic ball grid array)

2.3 Chip-Level Features

Key features of the MPC8536E include:

- High-performance Power Architecture e500v2 core with 36-bit physical addressing
- 512-Kbyte L2 cache with ECC
- Serial ATA (SATA) interface
- Integrated security engine (SEC) with XOR acceleration
- Power management controller
- Jog mode feature allows core frequency to be adjusted to optimize power consumption
- Three USB 2.0 dual-role controllers with ULPI interfaces
- Two integrated 10/100/1000 Mb enhanced three-speed Ethernet controllers (eTSECs) with TCP/IP acceleration and classification capabilities and SGMII interface support (through the SerDes interface)
- Three PCI Express controllers utilizing the SerDes interface
- DDR2/DDR3 SDRAM memory controller
- Programmable interrupt controller (PIC)
- High-speed enhanced serial peripheral interface (eSPI) with slave support
- IEEE 1588
- Enhanced secure digital host controller (eSDHC)
- Four-channel DMA controller
- Two I^2C controllers
- DUART
- Enhanced local bus controller (eLBC)
- 16 general-purpose I/O signals (independently configurable)

2.4 Module Features

The following sections cover the numerous features of the device in greater detail.

2.4.1 e500 Core and Memory Unit

The MPC8536E contains a high-performance 32-bit Book E-enhanced e500v2 core that implements the Power Architecture.

In addition to 36-bit physical addressing, this version of the e500 core includes:

- Double-precision floating-point APU with an instruction set for double-precision (64-bit) floating-point instructions that use the 64-bit general-purpose registers.
- Embedded vector and scalar single-precision floating-point APUs with an instruction set for single-precision (32-bit) floating-point instructions.

The MPC8536E contains a 512-Kbyte L2 cache/SRAM, as follows:

- Eight-way set-associative cache organization with 32-byte cache lines.

- Flexible configuration (one, two, four, or eight ways can be configured as SRAM).
- External masters can force data to be allocated into the cache through programmed memory ranges or special transaction types (stashing).
- SRAM:
  - I/O devices access SRAM regions by marking transactions as snoopable (global).
  - Regions can reside at any aligned location in the memory map.
  - Byte-accessible ECC uses read-modify-write accesses for smaller-than-cache-line accesses.

2.4.2 e500 Coherency Module (ECM) and Address Map

The e500 coherency module (ECM) provides a mechanism for I/O-initiated transactions to snoop the bus between the e500 core and the integrated L2 cache in order to maintain coherency across local cacheable memory. It also provides a flexible switch-type structure for core- and I/O-initiated transactions to be routed or dispatched to target modules on the device.

The MPC8536E supports a flexible 36-bit physical address map. Conceptually, the address map consists of local space and external address space. The local address map is supported by 12 local access windows that define mapping within the local 36-bit (64-Gbyte) address space.

The MPC8536E can be made part of a larger system address space through the mapping of translation windows. This functionality is included in the address translation and mapping units (ATMUs). Both inbound and outbound translation windows are provided. The ATMUs allows the MPC8536E to be part of larger address maps such as the PCI Express 64-bit address environment.

2.4.3 Integrated Security Engine (SEC)

The SEC 3.0 offloads computationally intensive security functions, such as key generation and exchange, authentication, and bulk encryption from the processor cores of the MPC8536E. It is optimized to process all cryptographic algorithms associated with IPsec, IKE, SSL/TLS, iSCSI, SRTP, IEEE Std. 802.11i™, 3G, A5/3 for GSM and EDGE, and GEA3 for GPRS. The SEC 3.0 derives from integrated security cores in other members of the PowerQUICC family, including the SEC 2.1 in the MPC8548E and the SEC 1.0 in the MPC8272E.

Components of the SEC are as follows:

- XOR engine for parity checking in RAID storage applications. Also, the exclusive OR (XOR) operation to generate parity data in RAID applications can be accelerated. XOR operations use SEC descriptors and offload both parity generation and data movement from the e500 core.
- Four crypto-channels, each supporting multi-command descriptor chains.
- Eight cryptographic execution units:
  - Advanced Encryption Standard unit (AESU)
  - ARC four execution unit (AFEU)
  - Cyclic redundancy check accelerator (CRCA)
  - Data Encryption Standard execution unit (DEU)
  - Kasumi execution unit (KEU)

— Message digest execution unit (MDEU)
— Public key execution unit (PKEU)
— Random number generator (RNGB)

2.4.4 High-Speed Interface Blocks (SerDes)

The MPC8536E offers two high-speed SerDes interface blocks. These blocks are connected to the SGMII, PCI Express, and SATA interfaces as described in this section.

2.4.4.1 Eight-Lane SerDes

The eight-lane SerDes allows use of the three PCI Express controllers. One of the configurations in Table 1 can be selected during power-on reset. See the reset chapter of the reference manual for further details.

Table 1. Supported SerDes 1 (PCI Express) Configurations

PCI Express Signal/Lane							
0/A	**1/B**	**2/C**	**3/D**	**4/E**	**5/F**	**6/G**	**7/H**
PEX1 x8							
PEX1 x4				PEX2 x4			
PEX1 x4				PEX2 x2		PEX3 x2	

2.4.4.2 Two-Lane SerDes

The two-lane SerDes allows use of the SATA controllers or of the SGMII interfaces of the eTSEC controllers (selected at power-on reset). Both lanes must be either SATA or SGMII. See the reset chapter of the reference manual for configuration options.

2.4.5 Enhanced Three-Speed Ethernet Controllers (eTSECs)

Two on-chip enhanced three-speed Ethernet controllers (eTSECs) incorporate a media access control (MAC) sublayer that supports 10- and 100-Mbps and 1-Gbps Ethernet/802.3 networks with MII, RMII, GMII, RGMII, TBI, and RTBI physical interfaces as well as SGMII interfaces through a dedicated SerDes. Each eTSEC includes a 2-Kbyte receive FIFO, a 10-Kbyte transmit FIFO, and DMA functions.

The MPC8536E eTSECs support programmable CRC generation and checking, RMON statistics, and jumbo frames of up to 9.6 Kbytes. Frame headers and buffer descriptors (BDs) can be forced into the L2 cache to speed classification or other frame processing. They are designed to comply with **IEEE** Std. 802.3™, 802.3u™, 802.3x™, 802.3z™, 802.3ac™, 802.3ab™. The BDs are based on the MPC8260 and MPC860T 10/100 Ethernet programming models. Each eTSEC provides hardware support for accelerating TCP/IP packet transmission and reception. By default, TCP/IP acceleration is not enabled and the eTSEC processes frames as pure Ethernet frames, emulating a PowerQUICC III TSEC and allowing existing driver software to be re-used with minimal change. Key features of these controllers include:

- Flexible configuration for multiple PHY interface configurations. The SGMII interface is available for any combination of eTSECs, regardless of the configuration of any other eTSEC.
- TCP/IP acceleration and QoS features:

  - IP v4 and IP v6 header recognition on receive
  - IP v4 header checksum verification and generation
  - TCP and UDP checksum verification and generation
  - Per-packet configurable acceleration
  - Recognition of VLAN, stacked (queue in queue) VLAN, IEEE Std. 802.2™, PPPoE session, MPLS stacks, and ESP/AH IP-security headers
  - All FIFO modes
  - Transmission from up to eight physical queues
  - Reception to up to eight physical queues
- Full- and half-duplex Ethernet support (1000 Mbps supports only full duplex): IEEE Std. 802.3 full-duplex flow control (automatic PAUSE frame generation or software-programmed PAUSE frame generation and recognition)
- IEEE Std. 802.1 virtual local area network (VLAN) tags and priority
- VLAN insertion and deletion
  - Per-frame VLAN control word or default VLAN for each eTSEC
  - Extracted VLAN control word passed to software separately
- Programmable Ethernet preamble insertion and extraction of up to 7 bytes
- MAC address recognition
- Can force allocation of header information and buffer descriptors into L2 cache

2.4.5.1 IEEE 1588 Integration

The eTSEC's IEEE 1588 integration allows extremely precise clock synchronization, with accuracy in the sub-microsecond range. This precision is achieved using regular Ethernet connectivity with standard Ethernet frames.

Benefits of the IEEE 1588 protocol include:

- Rapid convergence to sub-microsecond time synchronization between heterogeneous devices with different clocks, resolution, and stability
- Automatic configuration and segmentation
- Very simple configuration and operation with low computation resource and bandwidth consumption

2.4.6 Universal Serial Bus (USB) Controllers

The three USB dual-role controllers comply with USB specification revision 2.0.

2.4.6.1 Host Mode Operation

- Support operation as stand-alone USB host controllers
  - Support USB root hub with one downstream-facing port
  - Enhanced host controller interface (EHCI) compatible

- Support high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operations
- Support a direct connection to a high-speed device without an external hub
- Support external PHY with UTMI+ low-pin interface (ULPI)

2.4.6.2 Device Mode Operation

- Support operation as a stand-alone USB device
  - Support one upstream facing port
  - Support six programmable USB endpoints
- Support high-speed (480 Mbps) and full-speed (12 Mbps)
- Support external PHY with UTMI+ low-pin interface (ULPI)

2.4.7 DDR SDRAM Controller

The DDR memory controllers supports DDR2 and DDR3 SDRAM. The memory interface controls main memory accesses and provides a maximum of 32 Gbytes of main memory. The MPC8536E also supports chip-select interleaving. There is a variety of MPC8536E SDRAM configurations. SDRAM banks can be built using DIMMs or directly-attached memory devices. Sixteen multiplexed address signals provide for device densities of 64 Mbits, 128 Mbits, 256 Mbits, 512 Mbits, 1 Gbit, 2 Gbits, and 4 Gbits. Four chip-select signals support up to four banks of memory. Bank sizes range from 64 Mbytes to 4 Gbytes. Nine column address strobes (D*n*_MDM[0:8]) provide byte selection for memory bank writes.

The MPC8536E can be configured to retain the currently active SDRAM page for pipelined burst accesses. Page mode support of up to 32 simultaneously open pages can dramatically reduce access latencies for page hits. Depending on the memory system design and timing parameters, page mode can save 3 to 4 clock cycles for subsequent burst accesses that hit in an active page.

Using ECC, the MPC8536E detects and corrects all single-bit errors and detects all double-bit errors and all errors within a nibble.

The MPC8536E can invoke a level of system power management by asserting the D*n*_MCKE SDRAM signal on-the-fly to put the memory into a low-power sleep mode.

The DDR controllers offer both hardware and software options for battery-backed main memory. In addition, the DDR controllers offer an initialization bypass feature for use by system designers to prevent re-initialization of main memory during system power-on after an abnormal shutdown.

2.4.8 Power Management Controller

The MPC8536E is designed for low power consumption benefitting equipment manufacturers wishing to support ENERGY STAR standards. Dynamic power management locally minimizes power consumption in the doze, nap, or sleep modes. Additional static power saving can be accomplished by using deep sleep mode.

A jog mode feature is provided on the MPC8536E. In jog mode, the e500 core frequency can be adjusted dynamically while the platform frequency remains unchanged, resulting in optimal device temperature and power dissipation.

The power management controller (PMC) is responsible for maintaining the device in various low power modes. The PMC has the following features:

- Low standby power
- Jog mode support—Adjusts core frequency to optimize power consumption
- Support for dynamic and static power management to minimize power consumption of idle blocks:
  - Doze, nap, and sleep modes for dynamic power management
  - Deep sleep mode for static power management
- PMC wake on: LAN activity, USB connection or GPIO, internal timer, or external interrupt event

2.4.9 PCI Express Controller

The MPC8536E supports a PCI Express interface compliant with the *PCI Express Base Specification Revision 1.0a*. Each controller is configurable at boot time to act as either root complex or endpoint.

The physical layer of the PCI Express interface operates at a 2.5-Gbps data rate (effective rate of 2 Gbps due to encoding overhead) per lane. Receive and transmit ports operate independently, resulting in an aggregate theoretical bandwidth of 32 Gbps (x8 link) or 16 Gbps (x4 link).

Other features of the PCI Express interface include:

- x8, x4, x2, and x1 link widths supported
- Selectable operation as root complex or endpoint
- Both 32- and 64-bit addressing and 256-byte maximum payload size
- Full 64-bit decode with 36-bit wide windows

2.4.10 Programmable Interrupt Controller (PIC)

The MPC8536E PIC implements the logic and programming structures of the OpenPIC architecture, providing for external interrupts (with fully nested interrupt delivery), message interrupts, internal-logic driven interrupts, and global high-resolution timers. Up to 16 programmable interrupt priority levels are supported.

The PIC can be bypassed to allow use of an external interrupt controller.

2.4.11 Enhanced Secure Digital Host Controller (eSDHC)

The eSDHC provides an interface between the host system SD/MMC cards. The eSDHC acts as a bridge, passing host bus transactions to SD/MMC cards by sending commands and performing data accesses to or from the cards. The memory card invokes a copyright protection mechanism that complies with the security of the SDMI standard.

2.4.12 Enhanced Serial Peripheral Interface (eSPI)

The enhanced serial peripheral interface (eSPI) allows the device to operate as an SPI master to exchange data between other PowerQUICC family chips, Ethernet PHYs for configuration, and peripheral devices such as EEPROMs, real-time clocks, A/D converters, and ISDN devices.

The eSPI is a full-duplex, synchronous, character-oriented channel that supports a four-wire interface (receive, transmit, clock, and slave select). The eSPI block consists of transmitter and receiver sections, an independent baud-rate generator, and a control unit. It has the ability to boot from an SPI serial flash device.

The eSPI receiver and transmitter each have a FIFO of 32 bytes to support RapidS™ for Atmel™ devices. The eSPI also supports Winbond™ dual-output read commands; in this mode the eSPI uses two bits in parallel for read.

2.4.13 Serial ATA (SATA) Controllers

The SATA controllers have the following features:

- Supports host SATA I per spec Rev 1.0a
  - OOB
  - Port multipliers
  - ATAPI 6+
  - Spread spectrum clocking on receive
- Support for SATA II extensions
  - Asynchronous notification
  - Hot plug including asynchronous signal recovery
  - Link power management
  - Native command queuing
  - Staggered spin-up and port multiplier support
- Support for SATA I and II data rates (1.5 & 3.0 Gbaud)
- Standard ATA master-only emulation
- Includes ATA shadow registers
- Implements SATA superset registers (SError, SControl, SStatus)
- Interrupt driven
- Power management support
- Error handling and diagnostic features
  - Far end/near end loopback
  - Failed CRC error reporting
  - Increased ALIGN insertion rates
  - Scrambling and CONT override

2.4.14 DMA Controller, I^2C, DUART, eLBC

An integrated four-channel DMA controller can transfer data between any I/O or memory ports or between two devices or locations on the same port. The DMA controllers can be used as follows:

- To chain (both extended and direct) through local memory-mapped chain descriptors.

- To handle misaligned transfers, as well as stride transfers and complex transaction chaining.
- To specify local attributes such as snoop and L2 write stashing.

There are two I^2C controllers. These synchronous, multimaster buses can be connected to additional devices for expansion and system development.

The DUART supports full-duplex operation and is compatible with the PC16450 and PC16550 programming models. 16-byte FIFOs are supported for both the transmitter and the receiver.

The enhanced local bus controller (eLBC) port connects to a wide variety of external memories, DSPs, and ASICs. Three separate state machines share the same external pins and can be programmed separately to access different types of devices. The general-purpose chip select machine (GPCM) controls accesses to asynchronous devices using a simple handshake protocol. The user-programmable machine (UPM) can be programmed to interface to synchronous devices or custom ASIC interfaces. Features of the local bus controller are as follows:

- Multiplexed 32-bit address and data bus operating at up to 133 MHz
- Eight chip selects for eight external slaves
- Up to eight-beat burst transfers
- 32-, 16-, and 8-bit port sizes controlled by an internal memory controller
- Three protocol engines on a per-chip-select basis
- Parity support
- Default boot ROM chip select with configurable bus width (8, 16, or 32 bits)

3 Developer Environment

Development tools, hardware platforms, software building blocks and application-specific software solutions are available from Freescale and our Freescale Alliance Program, including third-party protocol and signaling stack suppliers, real-time operating systems support, and a variety of applications software support. All of these resources build upon the existing industry-standard PowerQUICC family support program.

To simplify and accelerate the development process, Freescale provides a user-friendly, integrated development environment (IDE), which includes a compiler, instruction set simulator, and debugger for the e500v2 Power Architecture core.

4 Document Revision History

Table 2 shows the revision history of this product brief.

Table 2. Revision History

Revision	Section/Page	Substantive Change(s)	Date
Rev 0		Initial revision	

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