Motorola's e500 Integrated Host Processor

Dan Bouvier

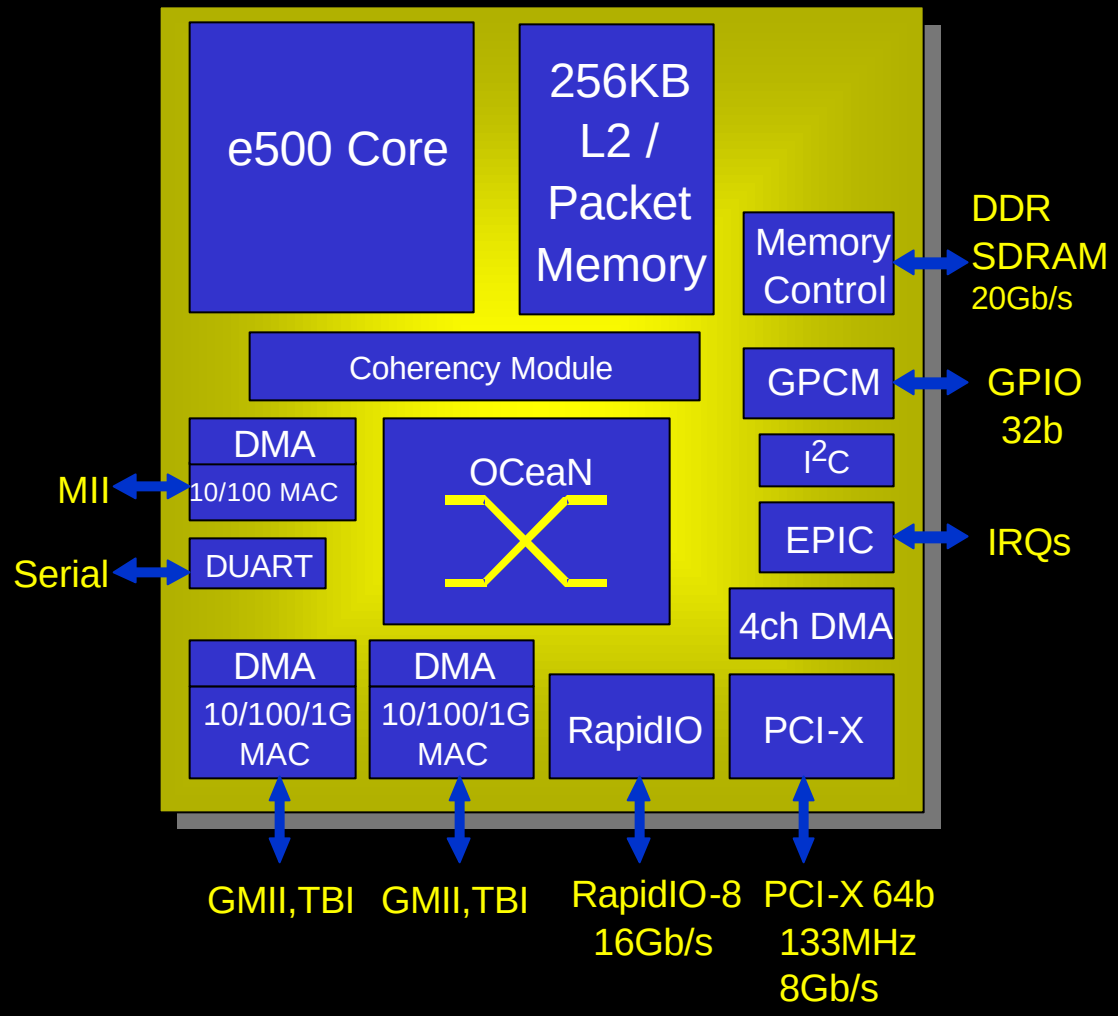
Motorola Semiconductor Products Sector

Somerset Architecture Manager

MPC85xx Family Design Goals

- Integration of RapidIO with a high performance, low power, 1 GHz e500 processor
- Address the processing needs for:
  - Network control plane workloads such as route exception processing and high touch services
  - Enterprise Storage Channel Processing
  - High Density Distributed Computing Platforms
- Optimize an SoC platform for performance and flexibility
  - Focus on MIPs / Watt / Packet / $
  - Balance processor performance with I/O system throughput
  - Include necessary Integration to enable multiple applications
  - Define a flexible architecture for easy integration of value added IP
    - Conform to Motorola's Semiconductor Reuse Standards SRS 3.0
- Provide a platform for a family of Motorola ASSPs for Communications, Automotive, and Consumer applications

Motorola's MPC8540

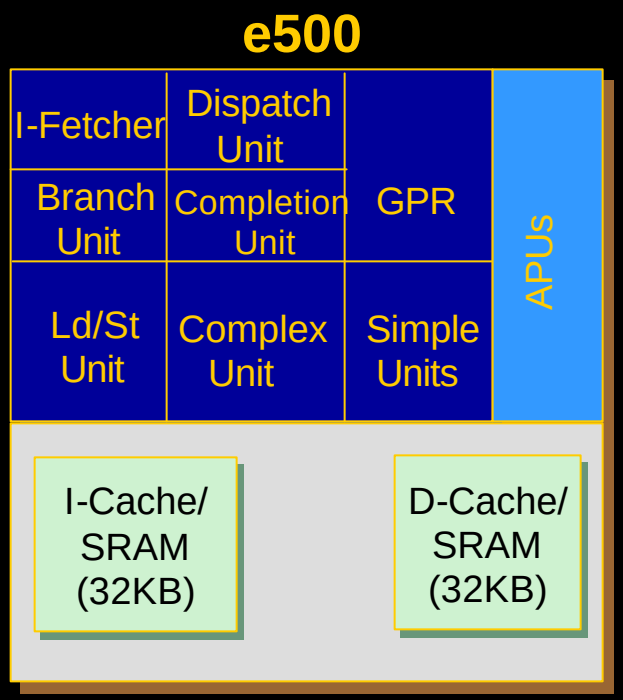


Features

- e500 "Book E" Processor 600Mhz - 1GHz
- 256k On-chip L2
- High Performance On Chip Fabric
- DDR Memory Controller
- Advanced I/O ports
  - RapidIO
  - PCI-X
  - 10/100/Gbit Ethernet
  - General Purpose ChipSelect Machine
- 4-Channel DMA
- Interrupt Controller
- DUART Serial Interface

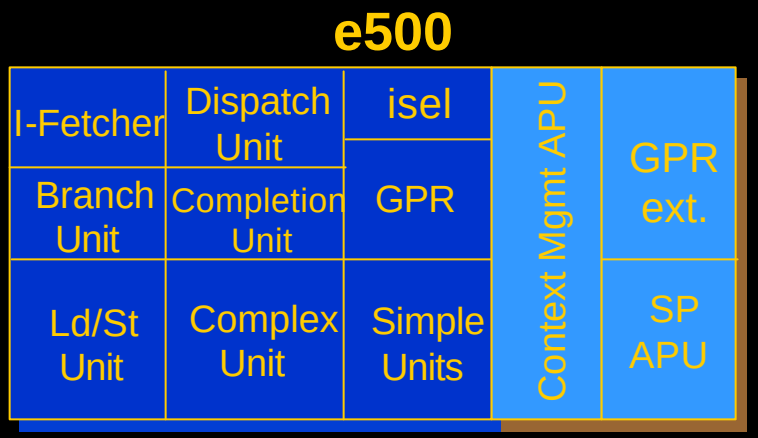
e500 Core Features

- 600MHz - 1GHz “Book E“ Microprocessor
- 2-way Superscalar
- Out-of-Order Issue and Execution with multiple execution units
- Support for Auxiliary Processor Units (APU)s
  - Context Management APU
  - isel APU
  - Signal Processing APU
- Book E MMU
  - Variable page sizes (4KB to 256MB)
  - Big/Little-Endian Support by page
- 32KB L1 I-Cache and D-Cache
  - Line by Line Locking
  - MESI cache coherency



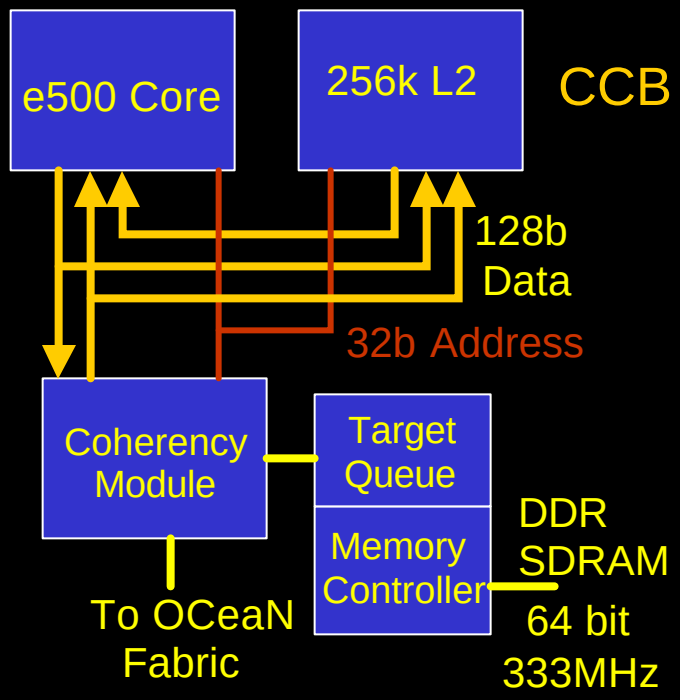
e500 APUs

- Context Management APU
  - Fast and Deterministic Context switching for lower interrupt latency
  - Registers for two contexts
- isel APU
  - Conditional MOVE Operation
  - Improves performance of code through simple predication to remove branches
  - *isel* instruction: **rd = crN ? rs1:rs2;**
- Signal Processing APU
  - Aimed at convergent Integer and DSP applications
  - SIMD unit with 222 new instructions
  - 64-bit GPRs overlaid on existing GPRs
  - Accumulator for single-cycle MAC



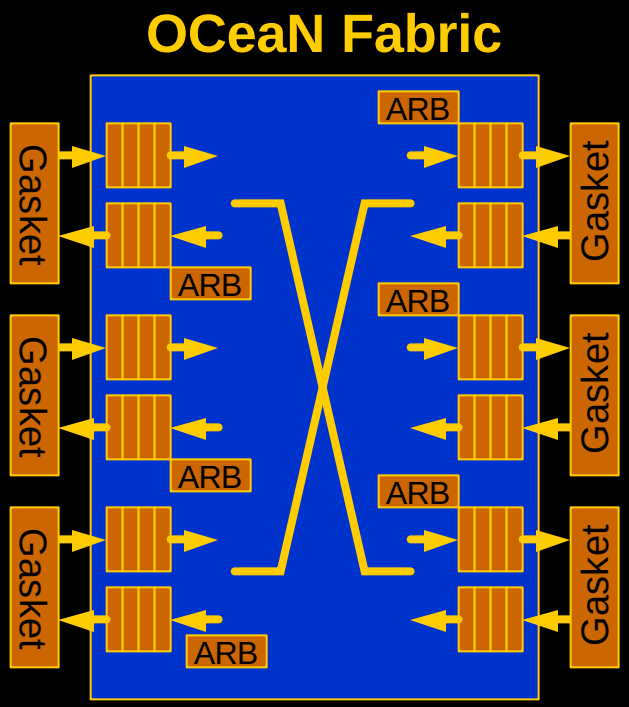
Core Complex

- Core Complex Bus (CCB)
  - SMP - MESI protocol, 32-bit address, Three 128b data busses
  - Split, out-of-order and multiple outstanding transactions
- Coherency Module
  - Manages 3 Concurrent Coherent Addresses
  - Entry point for non-coherent traffic
  - Speculative Fetches
- L2 Cache
  - 256kB 8-way set associative
  - Line by Line Locking
  - Memory-Mappable in 128k granules (externally writeable)
  - Allocate and Lock on DMA
- Memory Controller
  - 64-bit, 333MHz DDR SDRAM
  - 16 Outstanding Transactions
  - 4 - chip selects each supporting up to 1 Gbyte



OCeaN (On Chip Network)

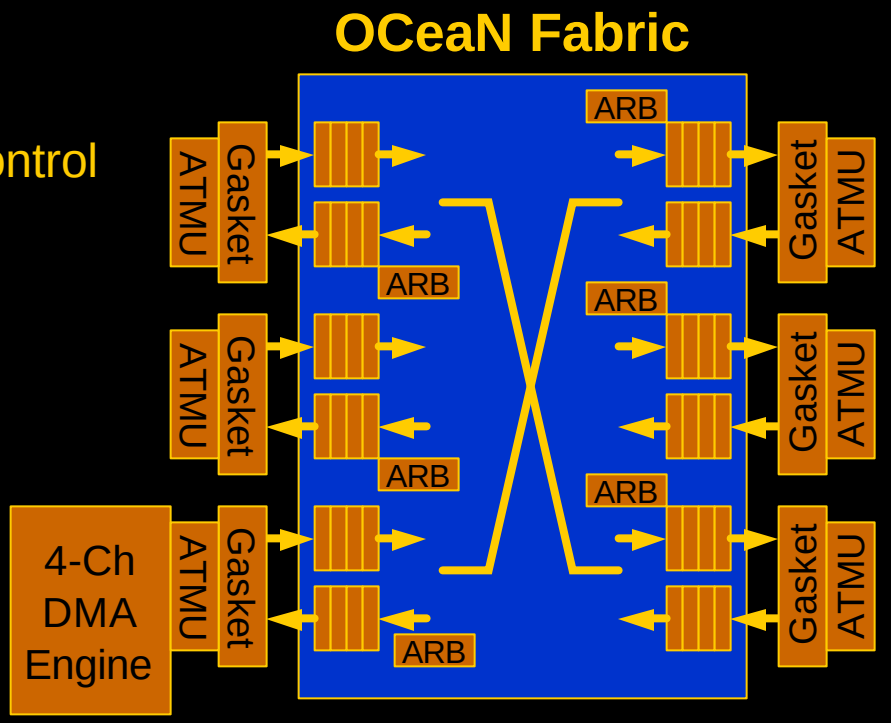
- Required an on-chip connection medium for multiple processors and peripherals
- On-chip peripheral busses don't scale well!
  - Needed scalability in numbers of ports and frequency
  - While maintaining chip route-ability
  - Needed a high level of transaction concurrency
- OCeaN (On Chip Network)
  - Scalable Non-Blocking Switch Fabric
  - Leverages RapidIO concepts
  - Full Duplex port connections 128Gb/s concurrent throughput
  - Independent Per Port Transaction Queuing and Flow Control
  - Latch to Latch protocol



High Performance Data Flow

- Address Translation and Mapping Unit ATMU
  - Flexible Address Mapping through Inbound and Outbound Windows
  - Port to port transaction routing
  - Provides all transaction attributes

- High Performance DMA Engine
  - 4 Channels - with Independent control
  - OCeaN allows concurrent load and store any port to any port
  - Bandwidth Allocation
  - 2-Level Descriptor Chain
  - Scatter Gather, Stride, Source/Destination Hold
  - Data Payloads up to 256 Bytes

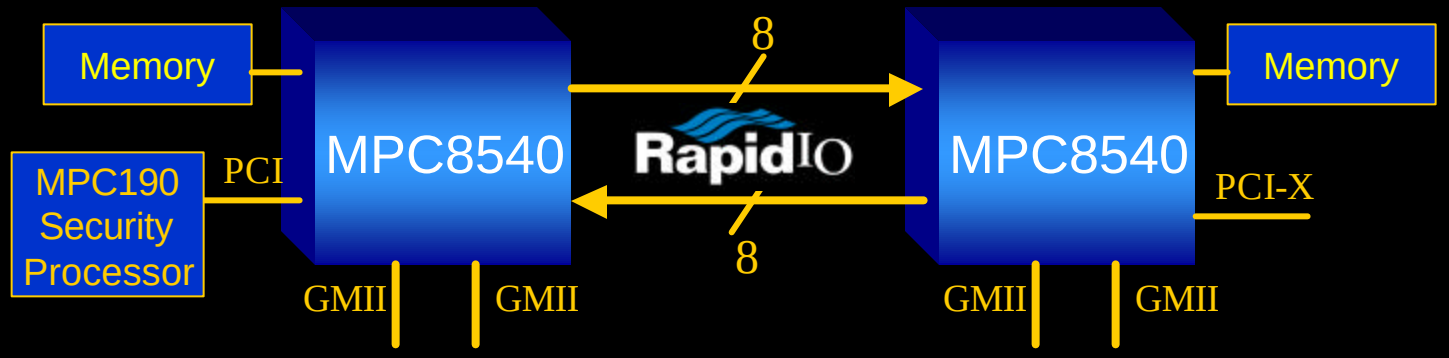


RapidIO

- Control Interconnect for High Performance Embedded Systems
- Open Standard backed by 46 companies
  led by: Alcatel, Cisco, EMC, Ericsson, IBM,
  Mercury Computer, Motorola, and Nortel
- Source addressed true switched control interconnect
  - Supports rich topologies and high level of concurrency
  - Scalable to 64k devices
- Highly Reliable
  - Automatic hardware error detection and recovery
- Software Transparent
- PCI bridge capable
- Parallel and soon to be released Serial Physical Layers

RapidIO on MPC8540

- Rev 1.1 Compliant 500MHz - 16 Gb/s Bandwidth
- Interface Point for Network Processors, ASICs, FPGAs, Protocol Chips, Accelerators
- 8 to 256 Byte packet data payloads with 4 Transaction Priorities
- Source Addressing for up to 256 Devices in arbitrary topologies
- Support for I/O system and Message Passing
  - up to 4 KByte Messages



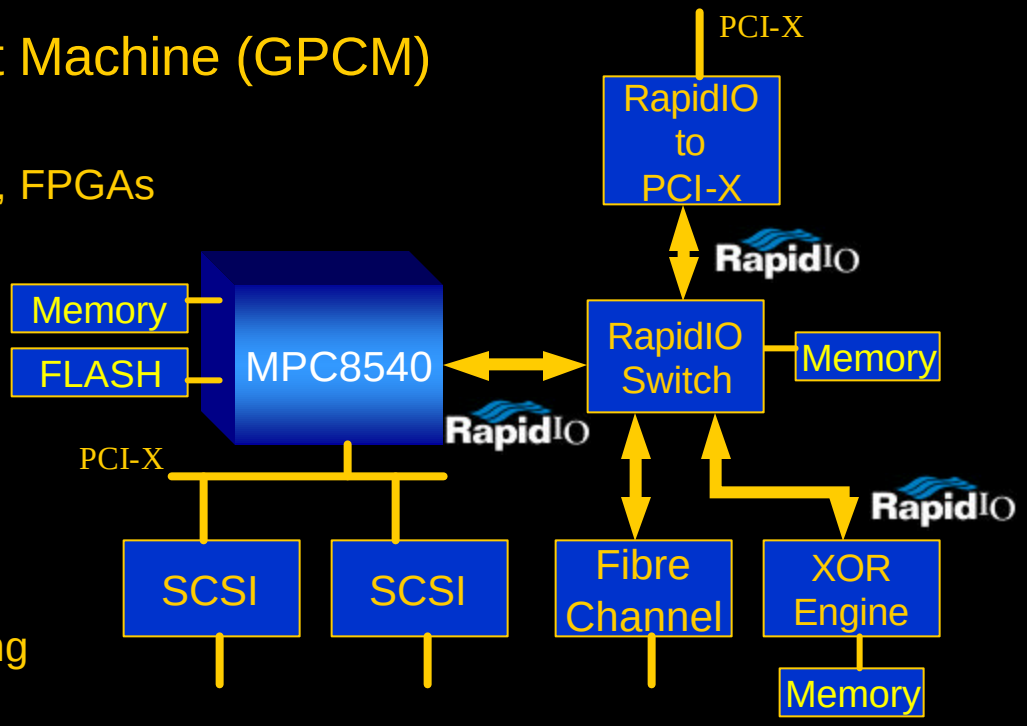
Ethernet Controllers

- Two High Performance 10/100/1G Controllers
  - IEEE 802.3, 802.3u, 820.3x, 802.3z, 802.3ac compliant
  - Consistent with Proven Programming Model (PowerQUICC)
  - Layer 2 Acceleration
    - 8 UniCast Address Matches
    - 512 entry hash for Broadcast and Multicast
    - Direct Queuing of 8 flows
  - Packet Field Extraction and Insertion
  - 9.6KB Jumbo Frame support
  - GMII and TBI SERDES interface
  - RMON statistics support
  - 2KB internal transmit and receive FIFOs
- One Maintenance 10/100 Controller
  - For console, debug, and maintenance interface

MPC8540 Peripheral Interfaces

- PCI-X Controller
  - 64b,133MHz
  - 64b Dual Address Cycle Support
  - Host and Agent Modes
  - PCI to RapidIO Bridge Support
- General Purpose Chip-select Machine (GPCM)
  - GPIO Port with 4 Chip Selects
  - Connect Flash, DSP Host Ports, FPGAs
- EPIC Interrupt Controller
  - 8 discrete or 16 serial IRQs
  - IPI Interface for up to 4 CPUs
  - Four - 32b Message Registers
  - Four cascade-able Timers
  - Selectable CPU notification using standard or critical interrupt

Storage Subsystem Processor

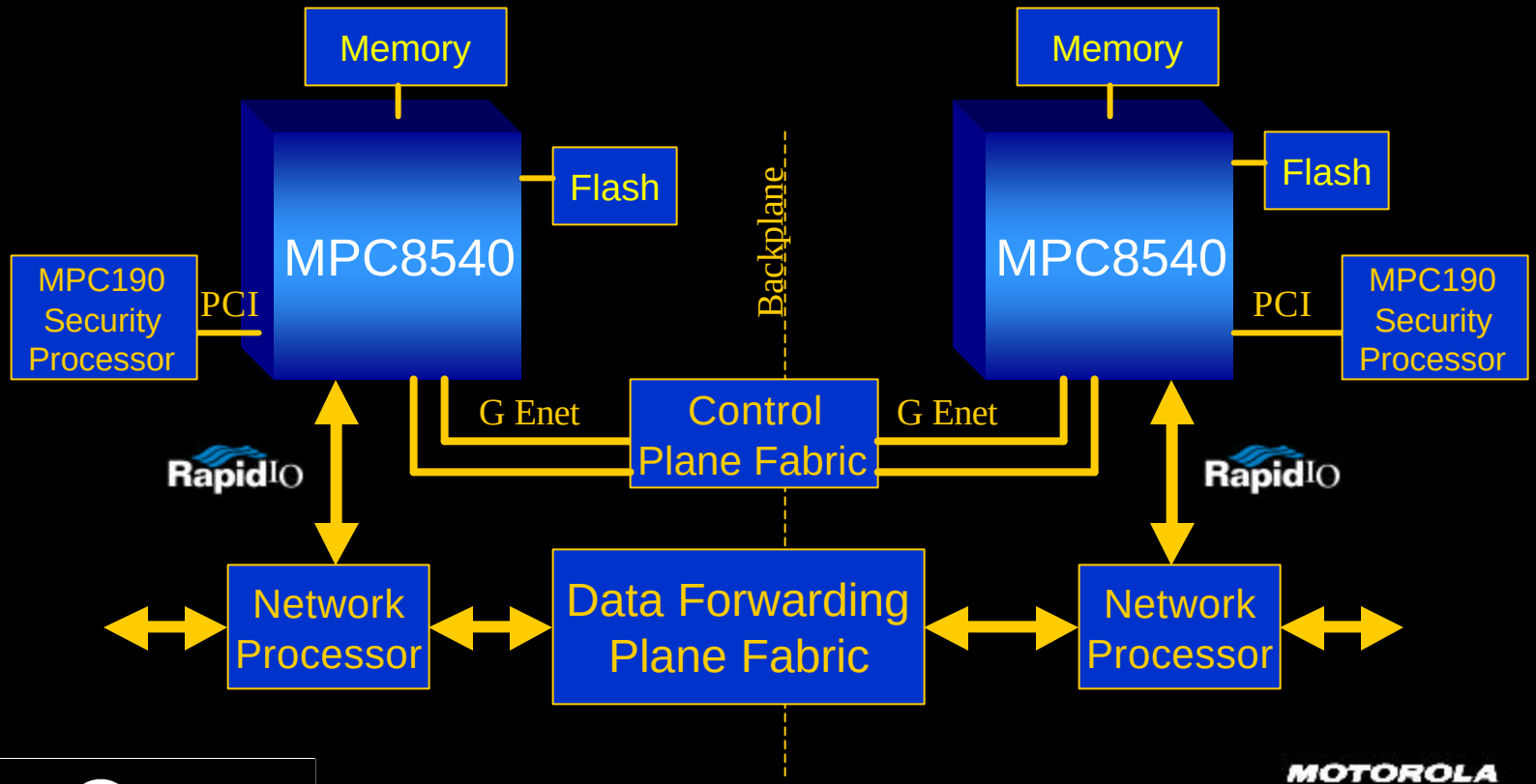


Error Management and Debug

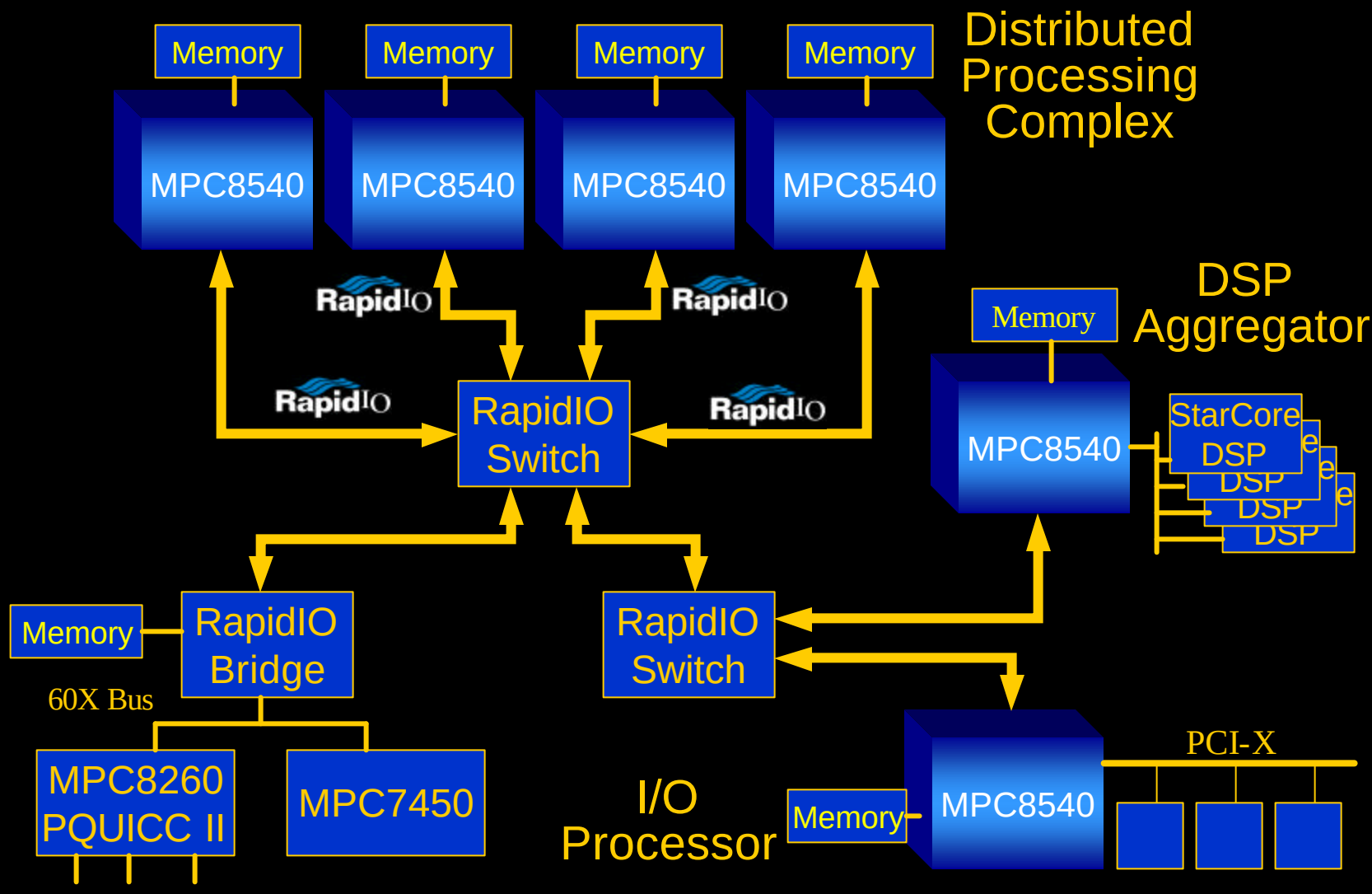
- Embedded Infrastructure Requires Robust Error Coverage
  - CPU Watchdog
  - L1 Caches - Parity, L2 Cache - ECC, Memory - ECC
  - RapidIO - transmission error detection and recovery, watchdog timers, diagnostic error injection logic
  - PCI, GPCM - parity
  - All Interfaces include a variety of error recording registers
- Debug Facilities
  - “Book E” enhanced processor debug facilities
  - IEEE 1149.1 complaint, JTAG boundary scan
  - 2 COPs (1 on core complex and 1 for system logic)
  - System Access Port - JTAG runtime access to system memory map
  - Memory interface attribute output pins
  - System logic watchpoint monitors with Input and output trigger pins

MPC8540 Applications

- Route Exception Processor
  - RapidIO for High Speed connection to forwarding plane
  - Gig-Ethernet for backplane control Communications (ex. SNMP)
  - PCI-X for legacy subsystem peripherals



MPC8540 Applications



Statistics

Architecture	PowerPC™ Book E Compatible
Performance (est.) (Dhrystone 2.1)	2315 MIPS @ 1 GHz 1385 MIPS @ 600MHz
Caches	L1:32KB I and D, L2: 256KB, 8-way
Power (est.)	6.5 W
Technology	0.13um Copper technology
Power Supply	1.5V
Package	575 pin PBGA

Summary

- Motorola's next generation e500 integrated processor provides a high performance control solution on an SoC platform optimized for MIPs / Watt / Packet / $
- Provide a platform for a family of Motorola ASSPs for Communications, Automotive, and Consumer applications

Thank you !