Layerscape in Automotive — Multicore Arm Processors for Telematics, Gateway and AD Sensor Fusion

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SECURE CONNECTIONS FOR A SMARTER WORLD

Agenda

- NXP Multicore Processor Families
- Digital Networking Layerscape Products
- Service Oriented Gateway
- ADAS/BlueBox
- Summary

NXP Automotive Microprocessors & Microcontrollers

BL DN
(Digital Networking)

High Performance Networking & Computing

- Highest networking & compute performance SoCs in NXP
- Experts in Linux, networking protocols, network security, virtualization

Products

QorIQ
Layerscape

BL Micros

Multimedia Processing

- HMI, Multimedia, Compute, Image Processing Leader
- GPUs with 1 to 16 Vec4 shaders, 8 to 256 GFLOPS
- With ML Framework
- Power efficiency, battery operation

Products

i.MX

BL AMP

ADAS
(Advanced Driver Assistance Systems)

Radar, LIDAR Vision Sensor Fusion

- #1 in Radar with strong IP and system knowledge
- High performance low power accelerators
- Scalable high performance roadmap for central processing

Products

S32R - Radar
S32V - Vision

C&S
(Connectivity & Security)

Gateway

- #1 in Vehicle Networking with leading networking and security IP
- #1 in Automotive HW Security with Strong IP and broad portfolio
- End to end portfolio of networking devices (MCU/MPU, TX/RX)

Products

MPC564xB/C
MPX574xG
S32

VDS
(Vehicle Dynamics & Safety)

Chassis & Safety Powertrain & Hybrid/EV

- Long term Innovator in Chassis and Powertrain Control.
- Significant Growth in Safety as Autonomous Control Drives Robust Fault Tolerant Systems

Products

MPC56xx
MPC57xx
S32S/P/H

GPIS
(General Purpose & Integrated Solutions)

Body Electronics Edge Nodes

- 500+ customers
- Broadest portfolio of integrated MCU+HV mixed-signal solutions
- Complete Tools & Software enablement

Products

S08/S12/PPC → ARM
KEA – S32K
S12 MagniV – S32M

DN Processors in Mission Critical Applications

Aerospace

Fuel Management, Main Flight Control, Secondary Flight Control, Aircraft Engine Management, Cockpit Display

Military and Defense

Rocket navigation, Artillery Control Computer, IFF

IFF, UAV Flight Computer, Defense Airborne Computer, Weapon Navigation System, Ground Control System

Factory Automation

Robotics Controllers, Motion Controllers, Multi-Axis Motor Controllers, Safety PLCs

Railway

Traction Control, Railway Signaling Controller, Railway Communications, Brake Controller

Power Grid

Power Distribution Relays, Smart Grid Communications

Layerscape Longevity

Industrial & Automotive applications require product longevity

- Long product lifecycles
- Special product certification required

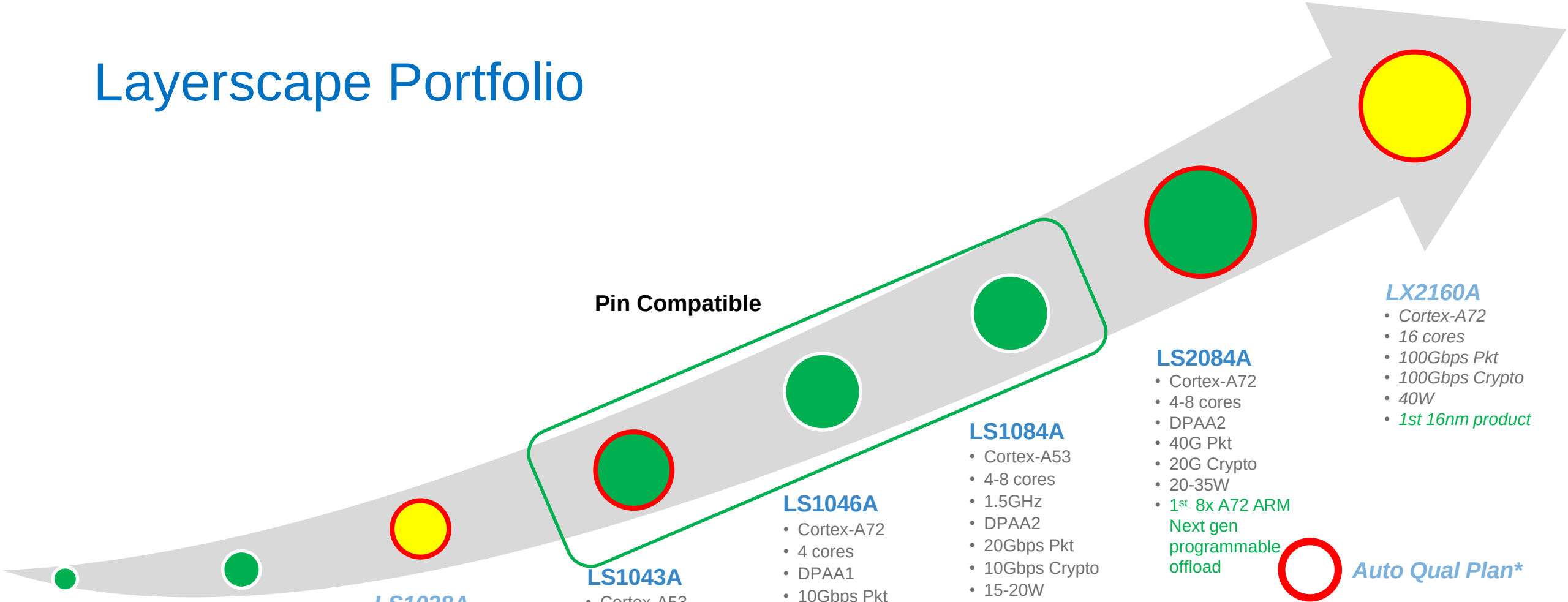
NXP Application Processors

- 10 and 15 year supply longevity options
- Formal program with products listed at www.nxp.com/productlongevity

Digital Networking is still selling the (Motorola) 68302, a processor which was introduced in 1989. Many other products are still shipping after >20 years.

Any Layerscape product selected for a production vehicle will be guaranteed 10yrs supply, regardless of official start date of 10-15 year guarantee in longevity program.

Layerscape Portfolio



LS1012A
- Cortex-A53
- 800MHz
- 2Gbps Packet
- 1Gbps Crypto
- 1-2W
- Lowest power 64-bit ARM

LS1021A
- Cortex-A7
- 2 cores
- 1GHz
- 2Gbps Pkt
- 1Gbps Crypto
- 2W

LS1028A
- *Cortex-A72*
- *2 cores*
- *5Gbps Pkt*
- *5Gbps Crypto*
- 4-9W
- *1st with TSN switch*
- *Integrated GPU*

LS1043A
- Cortex-A53
- 2-4 cores
- 10Gbps Pkt
- 5Gbps Crypto
- 4-8W
- 1st 64-bit ARM processor

LS1046A
- Cortex-A72
- 4 cores
- DPAA1
- 10Gbps Pkt
- 10Gbps Crypto
- 8-15W
- 1st Value Tier A72 ARM

LS1084A
- Cortex-A53
- 4-8 cores
- 1.5GHz
- DPAA2
- 20Gbps Pkt
- 10Gbps Crypto
- 15-20W
- 1st 8x A53 ARM Next gen programmable offload

LS2084A
- Cortex-A72
- 4-8 cores
- DPAA2
- 40G Pkt
- 20G Crypto
- 20-35W
- 1st 8x A72 ARM Next gen programmable offload

LX2160A
- *Cortex-A72*
- *16 cores*
- *100Gbps Pkt*
- *100Gbps Crypto*
- *40W*
- *1st 16nm product*

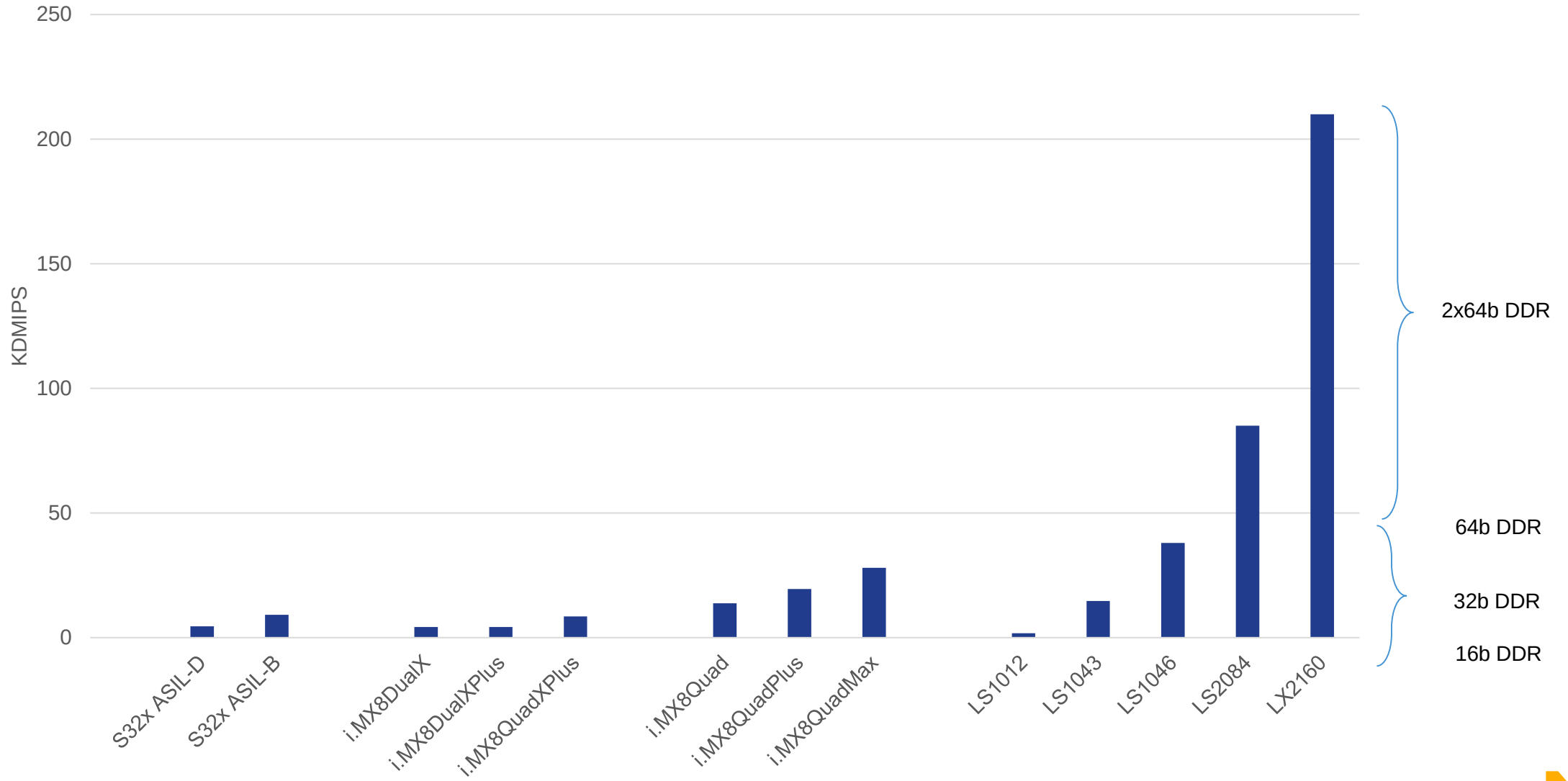
Auto Qual Plan*

Sampling

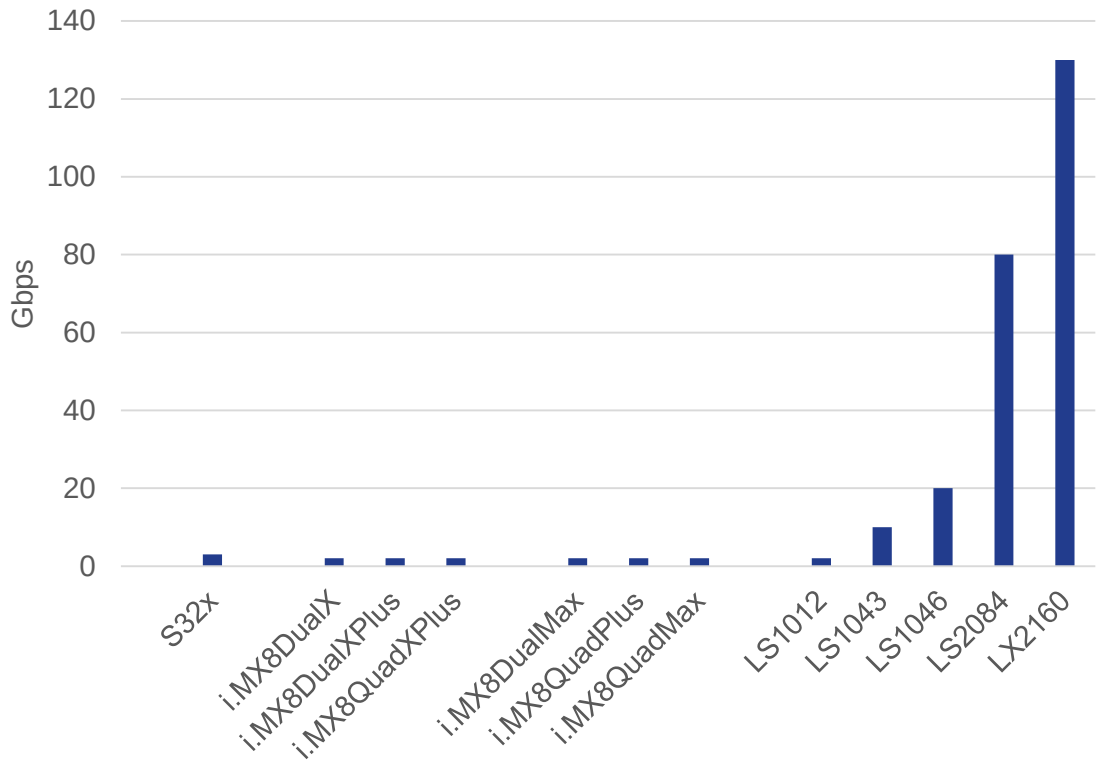
Production

* Additional products can be auto qualified with business justification

Comparative NXP ARM Processing Capacity



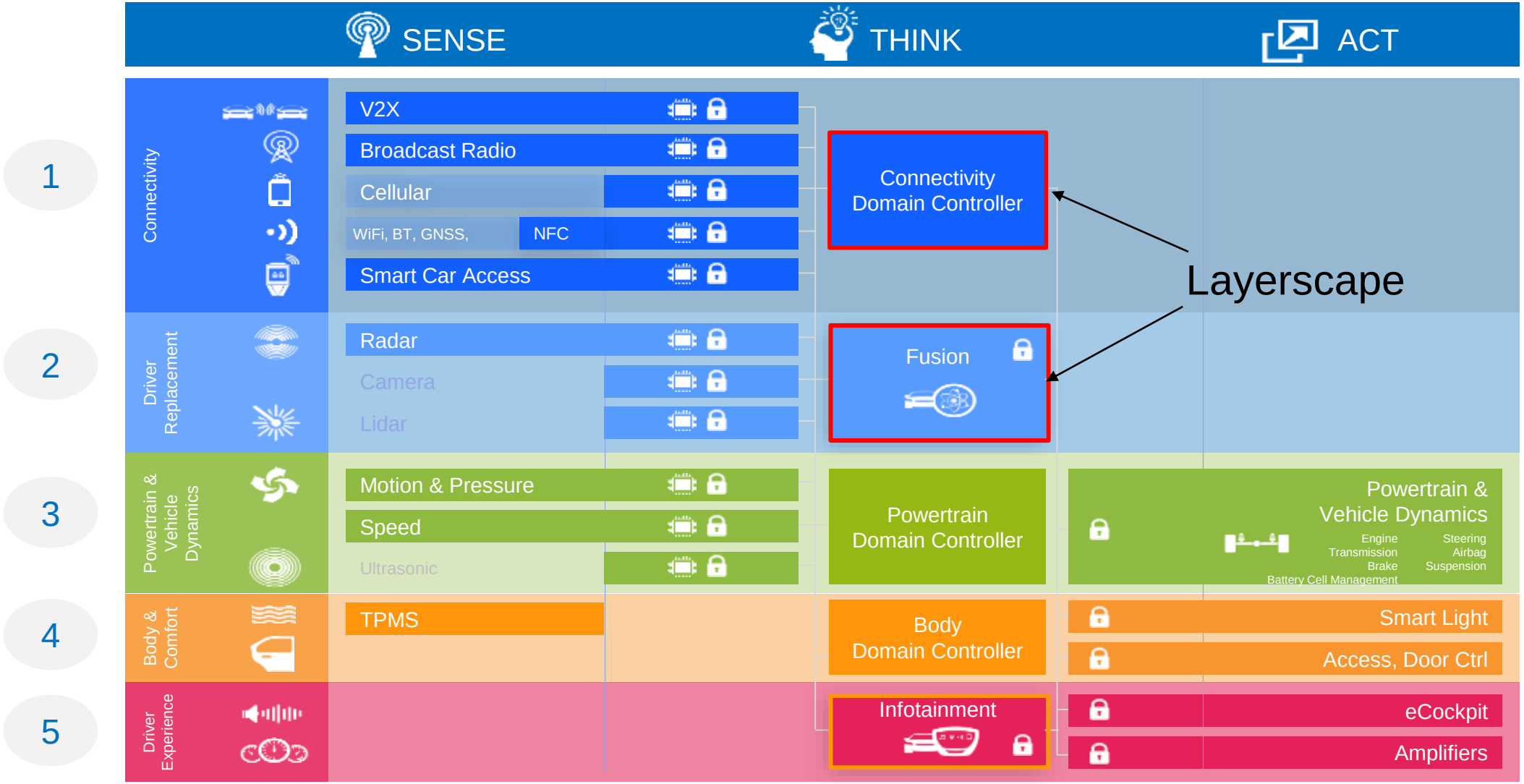
Comparative NXP ARM Packet Processing Capacity & High Speed IO



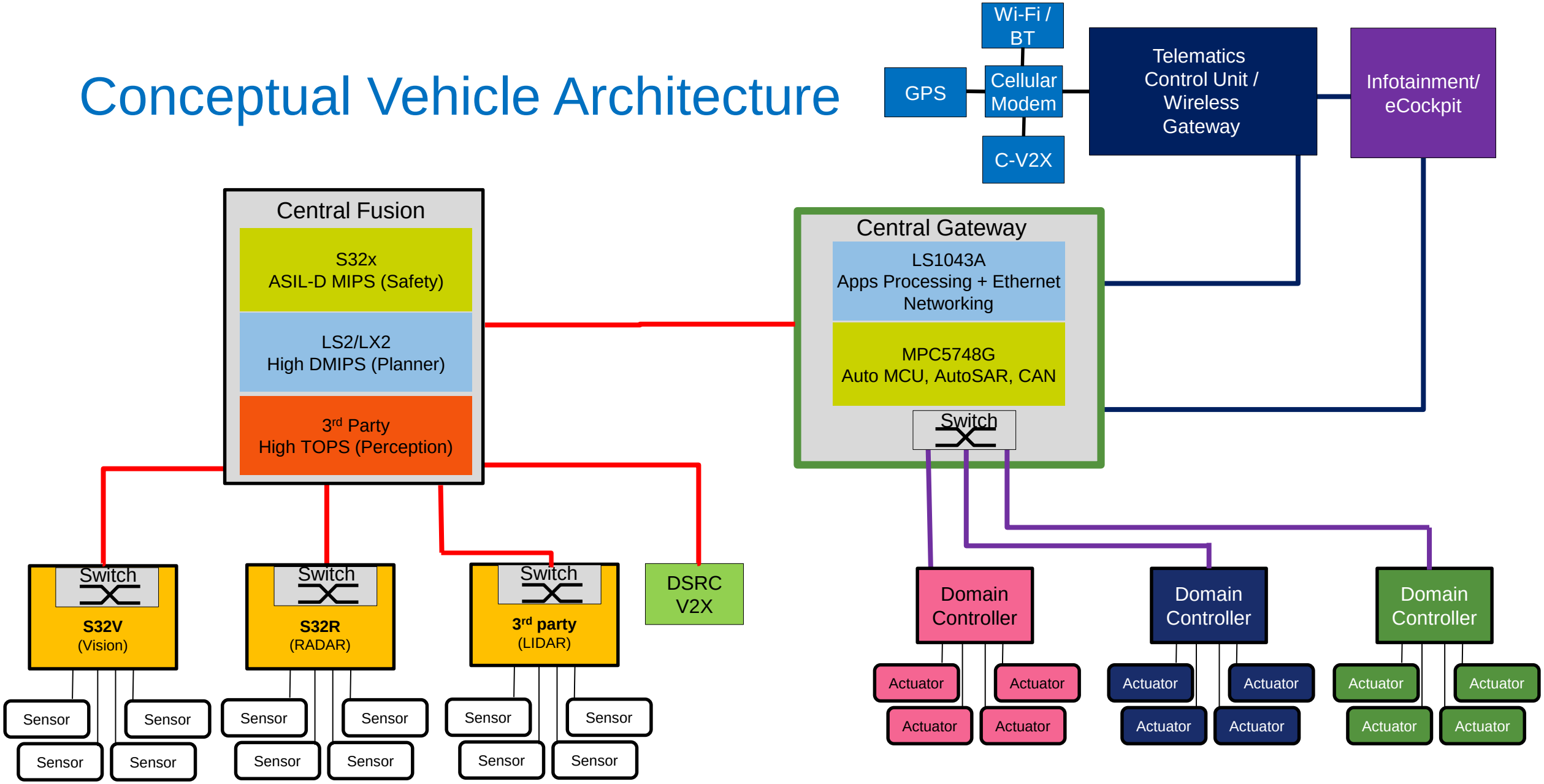
	Ethernet MAC (capable, not aggregate)			PCIe		USB	
Product	10G	2.5G	1G	Controllers	Max lanes	2.0	3.0
i.MX 8DualMax	0	0	1	2x 3.0	1	2	1
i.MX 8Quad	0	0	2	2x 3.0	1	2	1
LS1012A	0	2	2	1x 2.0	2	1	1
LS1043A	1	2	5	3x 2.0	4	0	3
LS1046A	2	2	5	3x 3.0	8	0	3
LS1084A	2	0	8	3x 2.0	8	0	3
LS2084A	8	8	8	3x 3.0	16	0	2
LX2160A	10	10	16	6x 3.0	24	0	2

Refer to product specific documents for exact features and performance

NXP Auto's View of Domains and Functions



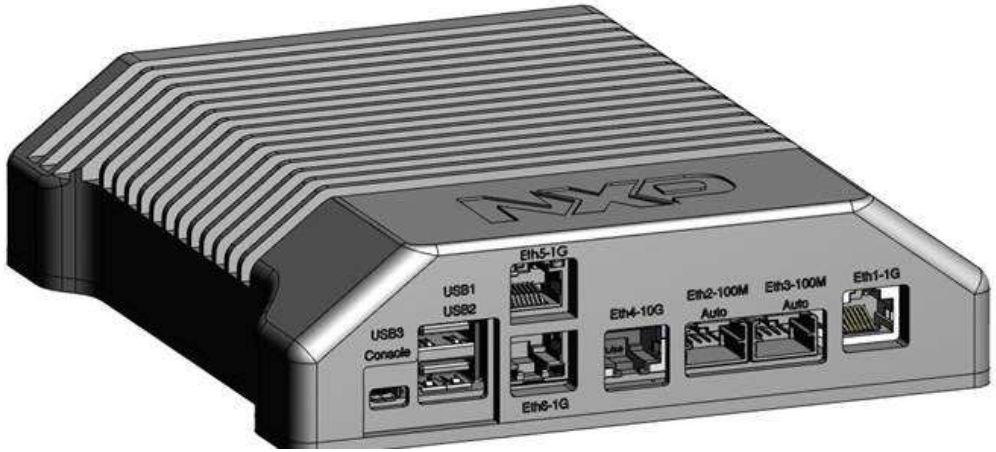
Conceptual Vehicle Architecture

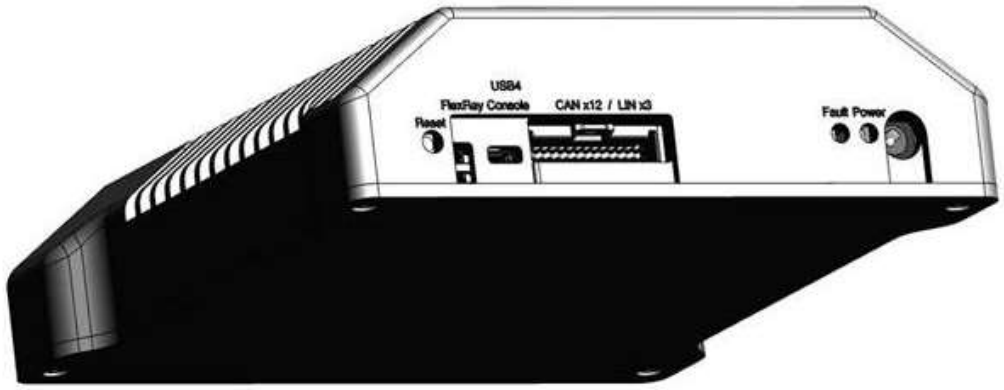


Gateway

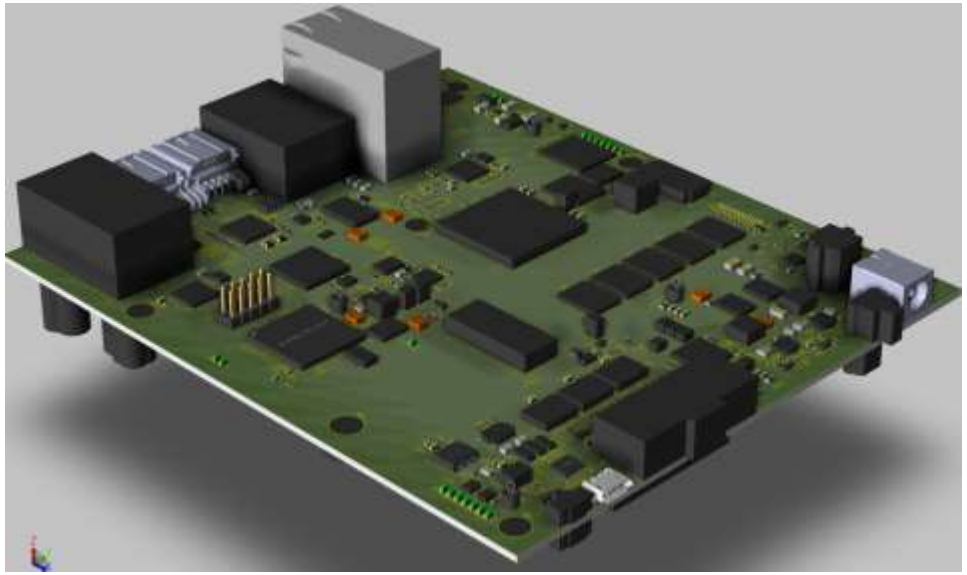
MPC-LS VNP Reference Design Board Preview

VNP Reference Design Board (RDB) provides value to customers with a more representative reference design schematics & layout for automotive MPC-LS solutions.

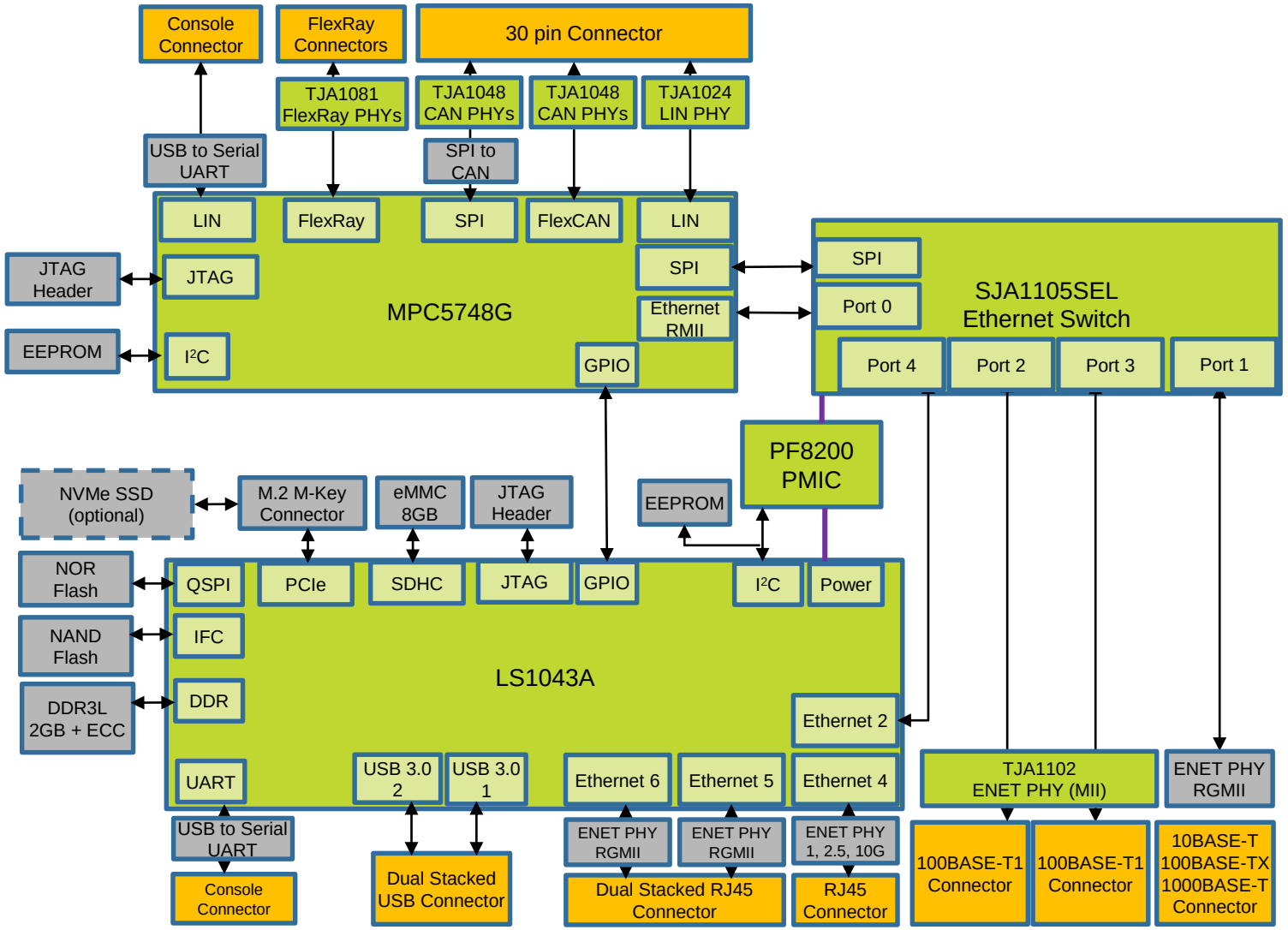




- Single 6-layer board ~ 6.1 x 6.4 x <2.0 inches
- 90% of the BOM is available in Automotive Grade



MPC-LS-VNP-RDB System Solution



MPC5748G Gateway Microcontroller

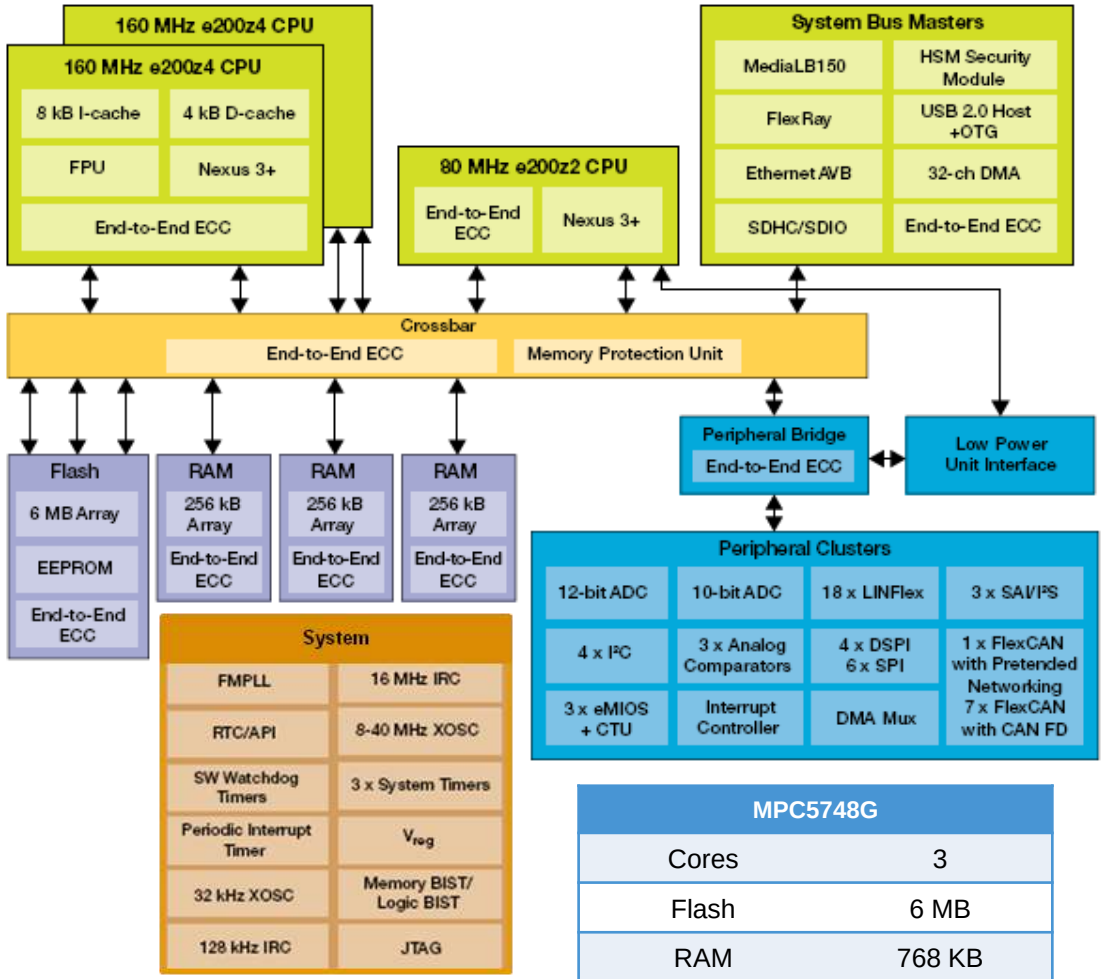
Multicore architecture

- Power Architecture cores
- 2x e200z4 @ 160MHz, with floating point unit
- 1x e200z2 @ 80MHz

Triple ported flash and multiple RAM for low memory latency

Safe Assure Functional Safety Program

- Designed for ISO 26262 ASIL B systems



MPC5748G	
Cores	3
Flash	6 MB
RAM	768 KB
Eth/FR/ML /SD/USB	2/1/1/1/2

Media Local Bus
Supports MOST for infotainment domain networking

Robust security
Hardware Security Module (HSM) option supports both SHE and EVITA low/medium security specifications

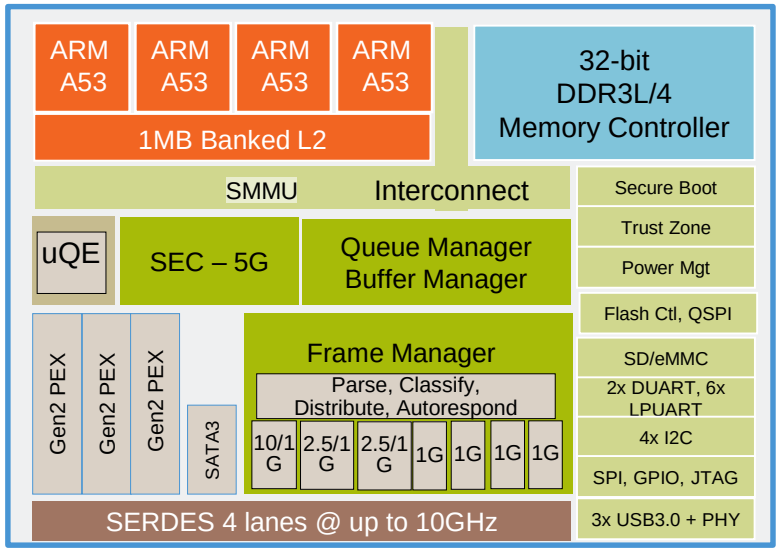
USB 2.0 (OTG and host module) supports interfacing to both wireless modems and infotainment domain

2 x Ethernet modules and **Ethernet Switch** support 10/100 Mb/s for diagnostics, backbone and AVB applications

Low-Power Unit (LPU)
provides CAN, LIN, SPI, ADC functionality in a new low power state

Broad Communications
Multiple CAN, LIN, I²C, I²S for integrated BCM & Gateway applications

QorIQ Layerscape LS1043ACE (Grade 3)



Major Milestone	Schedule
Engineering Samples Rev 1.1	Completed / October 4, 2016
Networking/Telecom Qualification	Completed / January 25, 2017
AECQ100 grade 3 Qual on Rev 1.1	Complete / Sept 12, 2017
PPAP Completion	June 2018 Updated PPAP (for new lidded package) Jan 2019

Auto Quality

- AEC Q100 Grade 3 (105 Tj max)
- 15 years product longevity
- ZD-like approach to reduce risk of DPPM or Life failures
- Expected Operating Life fail rate <10 FIT
- Mission Profile: 10 years, 90C Tj-effective

Process & Package

- 28HPM, ~5-9W Thermal Max @ 105C
- 23x23mm, Lidded FCBGA, .8mm pitch (780 pins)

Performance

- ARM A53 x 4 @ up to 1.6GHz (LS1023A: 2 cores)
  - 19.5K DMIPS
  - SpecInt2k6 – 5.95, Rate -15
  - Neon SIMD in all CPUs
- 1x36b (including ECC) DDR3L/4 up to 1.6GT/s
  - 6.4GB/s memory BW
- High Speed IO
  - Multiple PCIe Gen2 controllers
  - Multiple Ethernet MACs (up to 10G)

Functional Safety

- Target ASIL-B*
- ECC protected memories
- Fault localization, containment and recovery
- Soft lockstep with determinism
- Excellent support for virtualization, containerization

Security

- 5Gbps Crypto Acceleration
- IPsec, SSL
- Trust Architecture
  - Secure Boot
  - Secure Debug
  - Secure Storage
  - Tamper Detection
  - HW Enforced Partitioning
  - ARM Trust Zone

QorIQ Layerscape LS1043ACE (grade 3) Power Dissipation

4 cores

Table 10. LS1043A core power dissipation (V_{DD} = 1.0 V)

Core freq (MHz)	Platform freq (MHz)	DDR data rate (MT/s)	V_{DD} (V)	$S1V_{DD}$ (V)	Junction temp. (°C)	Power mode	Power (W)		Total Core and platform power (W)[1]	Notes
							V_{DD}	$S1V_{DD}$[8]		
1600	400	1600	1.0	1.0	65	Typical	3.79	0.39	4.18	2, 3
					105	Thermal	6.67	0.39	7.06	4, 7
						Maximum	7.41	0.39	7.80	5, 6, 7
1400	300	1600	1.0	1.0	65	Typical	3.30	0.36	3.69	2, 3
					105	Thermal	5.18	0.39	5.57	4, 7
						Maximum	5.77	0.39	6.16	5, 6, 7
1200	300	1600	1.0	1.0	65	Typical	3.18	0.36	3.57	2, 3
					105	Thermal	5.06	0.39	5.45	4, 7
						Maximum	5.65	0.39	6.04	5, 6, 7
1000	300	1600	1.0	1.0	65	Typical	3.06	0.36	3.45	2, 3
					105	Thermal	4.94	0.39	5.33	4, 7
						Maximum	5.48	0.39	5.87	5, 6, 7

1. Combined power of V_{DD} and $S1V_{DD}$ with platform at power-on reset default state, DDR controller and all SerDes banks active. Does not include I/O power.
2. Typical power assumes Dhrystone running with activity factor of 70% (for cores) and executing DMA on the platform with 100% activity factor.
3. Typical power based on nominal, processed device.
4. Thermal power assumes Dhrystone running with activity factor of 70% (for cores) and executing DMA on the platform at 100% activity factor.
5. Maximum power assumes Dhrystone running with activity factor at 100% (for cores) and executing DMA on the platform at 115% activity factor.
6. Maximum and Maximum power is provided for power supply design sizing.
7. Thermal and maximum power are based on worst case processed device.
8. Total $S1V_{DD}$ Power conditions:

a. SerDes Lane 1, XFI@ 10G

b. SerDes Lane 2 - 4, PCIe@ 5G

2 cores

Table 12. LS1023A core power dissipation (V_{DD} = 1.0 V)

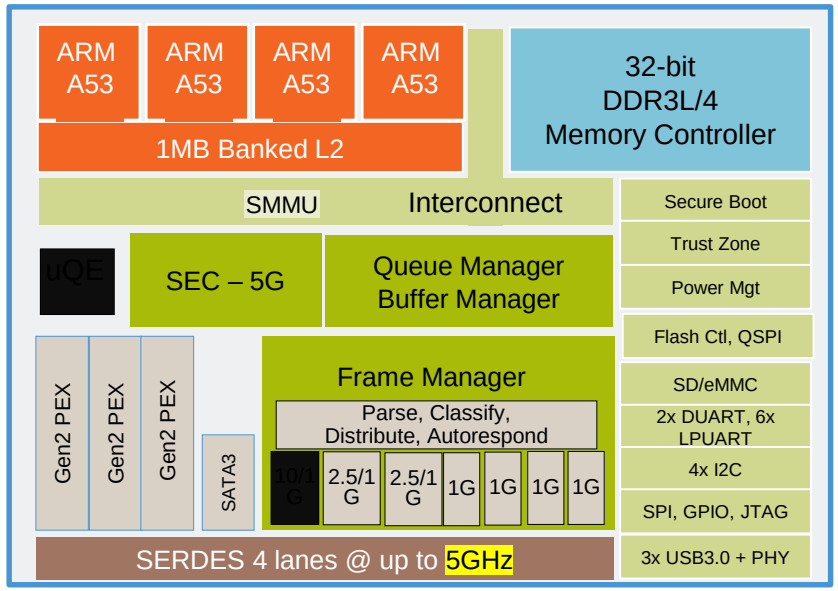
Core freq (MHz)	Platform freq (MHz)	DDR data rate (MT/s)	V_{DD} (V)	$S1V_{DD}$ (V)	Junction temp. (°C)	Power mode	Power (W)		Total Core and platform power (W)[1]	Notes
							V_{DD}	$S1V_{DD}$[8]		
1600	400	1600	1.0	1.0	65	Typical	3.30	0.39	3.69	2, 3
					105	Thermal	5.69	0.39	6.08	4, 7
						Maximum	6.16	0.39	6.55	5, 6, 7
1400	300	1600	1.0	1.0	65	Typical	2.86	0.39	3.25	2, 3
					105	Thermal	4.42	0.39	4.81	4, 7
						Maximum	4.80	0.39	5.19	5, 6, 7
1200	300	1600	1.0	1.0	65	Typical	2.78	0.39	3.17	2, 3
					105	Thermal	4.35	0.39	4.74	4, 7
						Maximum	4.73	0.39	5.12	5, 6, 7
1000	300	1600	1.0	1.0	65	Typical	2.71	0.39	3.10	2, 3
					105	Thermal	4.27	0.39	4.66	4, 7
						Maximum	4.64	0.39	5.03	5, 6, 7

1. Combined power of V_{DD} and $S1V_{DD}$ with platform at power-on reset default state, DDR controller and all SerDes banks active. Does not include I/O power.
2. Typical power assumes Dhrystone running with activity factor of 80% (for cores) and executing DMA on the platform with 100% activity factor.
3. Typical power based on nominal, processed device.
4. Thermal power assumes Dhrystone running with activity factor of 80% (for cores) and executing DMA on the platform at 100% activity factor.
5. Maximum power assumes Dhrystone running with activity factor at 100% (for cores) and executing DMA on the platform at 115% activity factor.
6. Maximum power is provided for power supply design sizing.
7. Thermal and maximum power are based on worst case processed device.
8. Total $S1V_{DD}$ Power conditions:

a. SerDes Lane 1, XFI@ 10G

b. SerDes Lane 2 - 4, PCIe@ 5G

QorIQ Layerscape LS1043ABE (Grade 2)



Auto Quality

- AEC Q100 Grade 2 (125 Tj max)
- 15 years product longevity
- ZD-like approach to reduce risk of DPPM or Life failures
- Expected Operating Life fail rate <10 FIT
- Mission Profile: 10 years, 90C Tj-effective

Major Milestone	Schedule
Engineering Samples	Completed / May 2018
AECQ100 grade 2 Qual	Completed / Oct, 2018
Grade 2 PPAP Completion	Jan 2019

Performance

- ARM A53 x 4 @ up to 1.4GHz (LS1023A: 2 cores)
  - 17K DMIPS
  - SpecInt2k6 – 5.2, Rate -13.1
  - Neon SIMD in all CPUs
- 1x36b (including ECC) DDR3L/4 up to 1.6GT/s
  - 6.4GB/s memory BW
- High Speed IO
  - Multiple PCIe Gen2 controllers
  - Multiple Ethernet MACs (up to 2.5G)

Functional Safety

- Target ASIL-B*
- ECC protected memories
- Fault localization, containment and recovery
- Soft lockstep with determinism
- Excellent support for virtualization, containerization

Security

- 5Gbps Crypto Acceleration
- IPsec, SSL
- Trust Architecture
  - Secure Boot
  - Secure Debug
  - Secure Storage
  - Tamper Detection
  - HW Enforced Partitioning
  - ARM Trust Zone

Process & Package

- 28HPM, up to 11W Thermal Max @ 125C
- 23x23mm, Lidded FCBGA, .8mm pitch (780 pins)

QorIQ Layerscape LS1043ABE (Grade 2) Power Dissipation

4 cores

Table 8. LS1043A core power dissipation (V_{DD} = 1.0 V)

Core freq (MHz)	Platform freq (MHz)	DDR data rate (MT/s)	V_{DD} (V)	$S1V_{DD}$ (V)	Junction temp. (°C)	Power mode	Power (W)		Total Core and platform power (W)[1]	Notes
							V_{DD}	$S1V_{DD}$[8]		
1400	300	1600	1.0	1.0	65	Typical	3.30	0.39	3.69	2, 3
					125	Thermal	8.69	0.40	9.09	4, 7
						Maximum	9.28	0.40	9.68	5, 6, 7
1200	300	1600	1.0	1.0	65	Typical	3.18	0.39	3.57	2, 3
					125	Thermal	8.57	0.40	8.97	4, 7
						Maximum	9.16	0.40	9.56	5, 6, 7
1000	300	1600	1.0	1.0	65	Typical	3.06	0.39	3.45	2, 3
					125	Thermal	8.45	0.40	8.85	4, 7
						Maximum	8.99	0.40	9.39	5, 6, 7

1. Combined power of V_{DD} and $S1V_{DD}$ with platform at power-on reset default state, DDR controller and all SerDes banks active. Does not include I/O power.

2. Typical power assumes Dhrystone running with activity factor of 70% (for cores) and executing DMA on the platform with 100% activity factor.

3. Typical power based on nominal, processed device.

4. Thermal power assumes Dhrystone running with activity factor of 70% (for cores) and executing DMA on the platform at 100% activity factor.

5. Maximum power assumes Dhrystone running with activity factor at 100% (for cores) and executing DMA on the platform at 115% activity factor.

6. Maximum power is provided for power supply design sizing.

7. Thermal and maximum power are based on worst case processed device.

8. Total $S1V_{DD}$ Power conditions:

a. SerDes Lane 1-4, PCIe@ 5G

2 cores

Table 9. LS1023A core power dissipation (V_{DD} = 1.0 V)

Core freq (MHz)	Platform freq (MHz)	DDR data rate (MT/s)	V_{DD} (V)	$S1V_{DD}$ (V)	Junction temp. (°C)	Power mode	Power (W)		Total Core and platform power (W)[1]	Notes
							V_{DD}	$S1V_{DD}$[8]		
1400	300	1600	1.0	1.0	65	Typical	2.86	0.39	3.25	2, 3
					125	Thermal	7.33	0.40	7.73	4, 7
						Maximum	7.71	0.40	8.11	5, 6, 7
1200	300	1600	1.0	1.0	65	Typical	2.78	0.39	3.17	2, 3
					125	Thermal	7.26	0.40	7.66	4, 7
						Maximum	7.64	0.40	8.04	5, 6, 7
1000	300	1600	1.0	1.0	65	Typical	2.71	0.39	3.10	2, 3
					125	Thermal	7.18	0.40	7.58	4, 7
						Maximum	7.55	0.40	7.95	5, 6, 7

1. Combined power of V_{DD} and $S1V_{DD}$ with platform at power-on reset default state, DDR controller and all SerDes banks active. Does not include I/O power.

2. Typical power assumes Dhrystone running with activity factor of 80% (for cores) and executing DMA on the platform with 100% activity factor.

3. Typical power based on nominal, processed device.

4. Thermal power assumes Dhrystone running with activity factor of 80% (for cores) and executing DMA on the platform at 100% activity factor.

5. Maximum power assumes Dhrystone running with activity factor at 100% (for cores) and executing DMA on the platform at 115% activity factor.

6. Maximum power is provided for power supply design sizing.

7. Thermal and maximum power are based on worst case processed device.

8. Total $S1V_{DD}$ Power conditions:

a. SerDes Lane 1-4, PCIe@ 5G

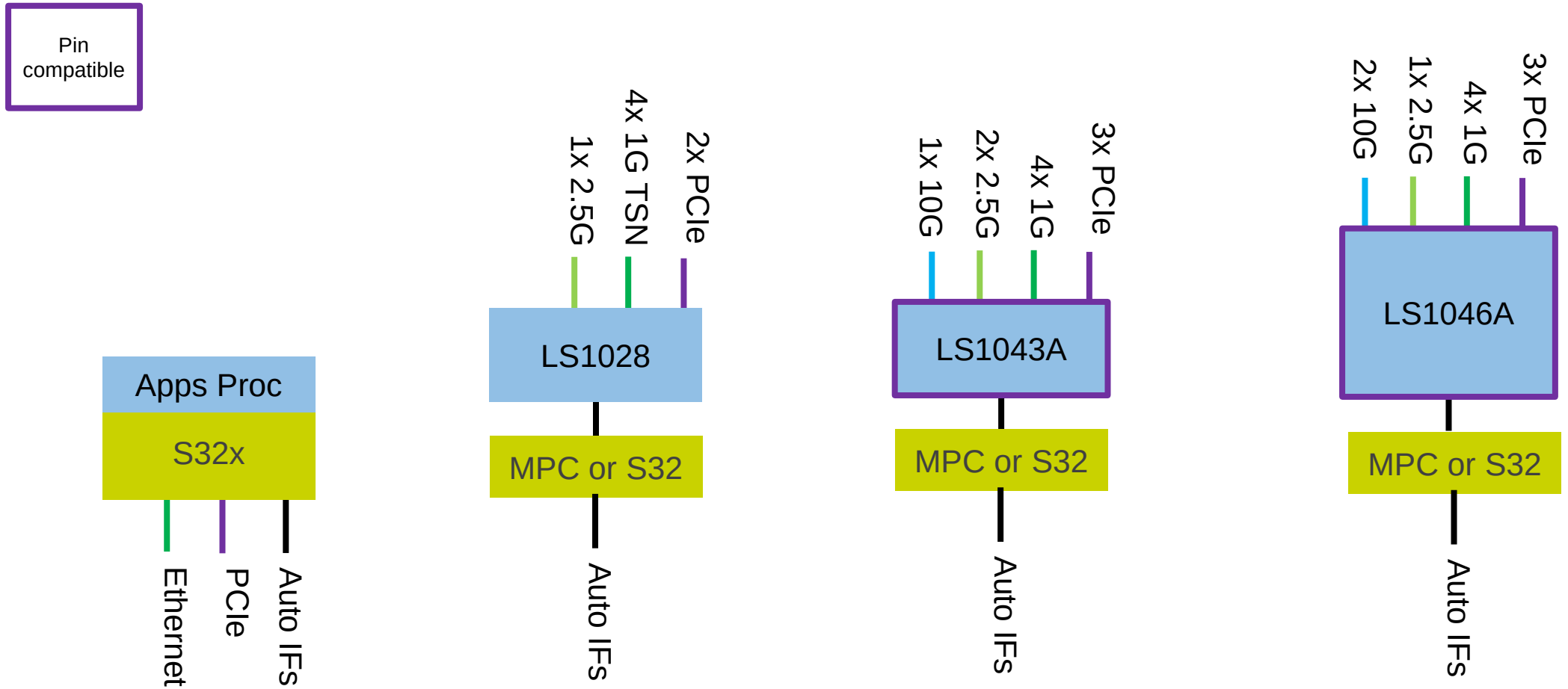
LS1043 SERDES Options

- Rows with green right edge are supported on grade 2 version
- Rows with black right edge are only supported on grade 3 version

LS1043 SERDES (4 lanes)

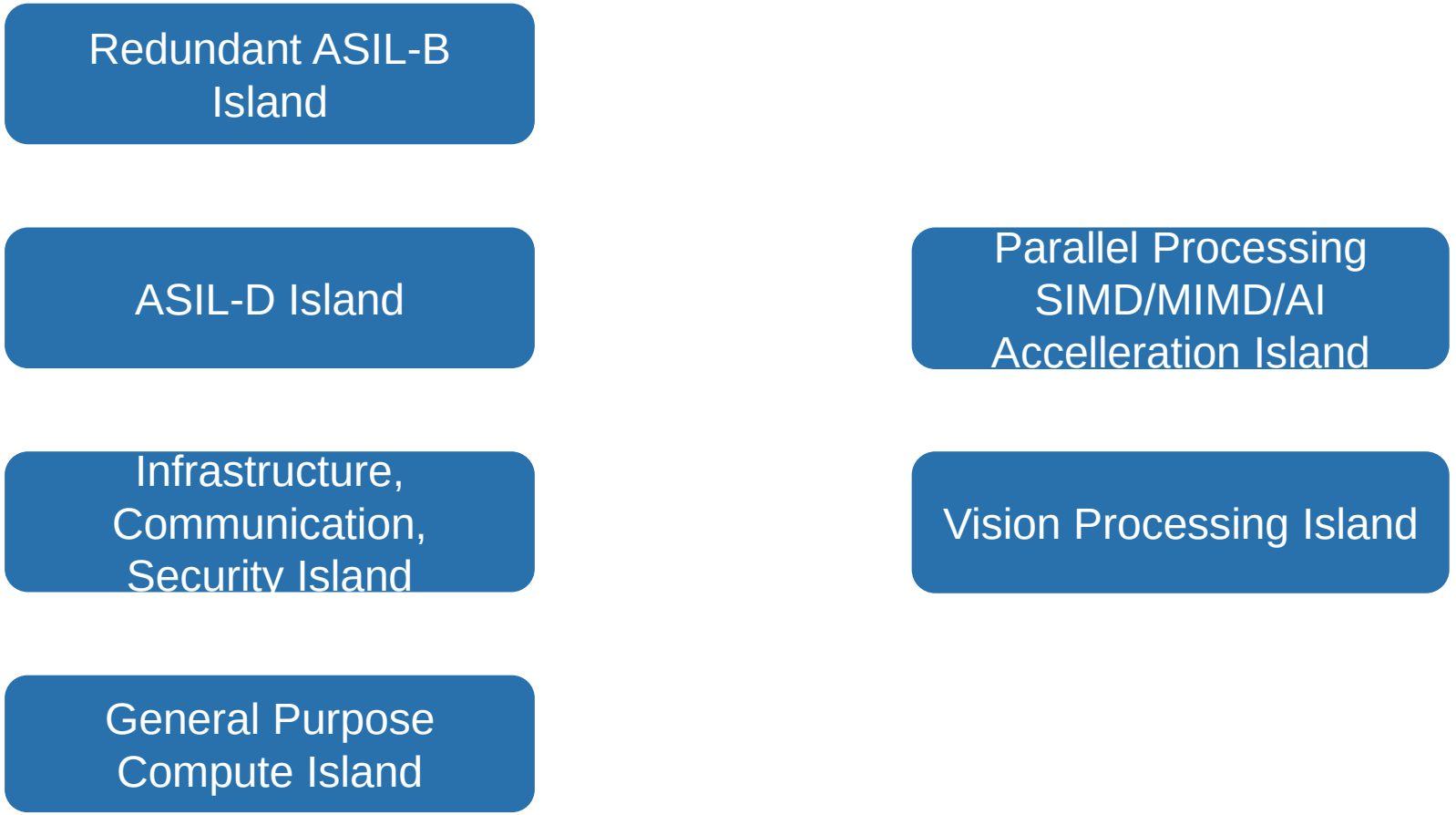
	Grade 3				Grade 2
	Serdes 1				
	0	1	2	3	
SERDES Prot	A	B	C	D	
0000	unused	unused	unused	unused	
1555	XFI	PCIe 1	PCIe 2	PCIe 3	
2555	SGMII 2.5G	PCIe 1	PCIe 2	PCIe 3	
4555	QSGMII	PCIe 1	PCIe 2	PCIe 3	
4558	QSGMII	PCIe 1	PCIe 2	SATA	
1355	XFI	SGMII 1G	PCIe 2	PCIe 3	
2355	SGMII 2.5G	SGMII 1G	PCIe 2	PCIe 3	
3335	SGMII 1G	SGMII 1G	SGMII 1G	PCIe 3	
3355	SGMII 1G	SGMII 1G	PCIe 2	PCIe 3	
3358	SGMII 1G	SGMII 1G	PCIe 2	SATA	
3558	SGMII 1G	PCIe 1	PCIe 2	SATA	
3555	SGMII 1G	PCIe 1	PCIe 2	PCIe 3	
7000	PCIe 1				
9998	PCIe 1	PCIe 2	PCIe 3	SATA	
6058	PCIe 1		PCIe 2	SATA	
1455	XFI	QSGMII	PCIe 2	PCIe 3	
2455	SGMII 2.5G	QSGMII	PCIe 2	PCIe 3	
2255	SGMII 2.5G	SGMII 2.5G	PCIe 2	PCIe 3	
3333	SGMII 1G	SGMII 1G	SGMII 1G	SGMII 1G	
1460	XFI	QSGMII	PCIe 3		
2460	SGMII 2.5G	QSGMII	PCIe 3		
3460	SGMII 1G	QSGMII	PCIe 3		
3455	SGMII 1G	QSGMII	PCIe 2	PCIe 3	
9960	PCIe 1	PCIe 2	PCIe 3		
2233	SGMII 2.5G	SGMII 2.5G	SGMII 1G	SGMII 1G	
2533	SGMII 2.5G	PCIe 1	SGMII 1G	SGMII 1G	

Gateway/Vehicle Server Scalability

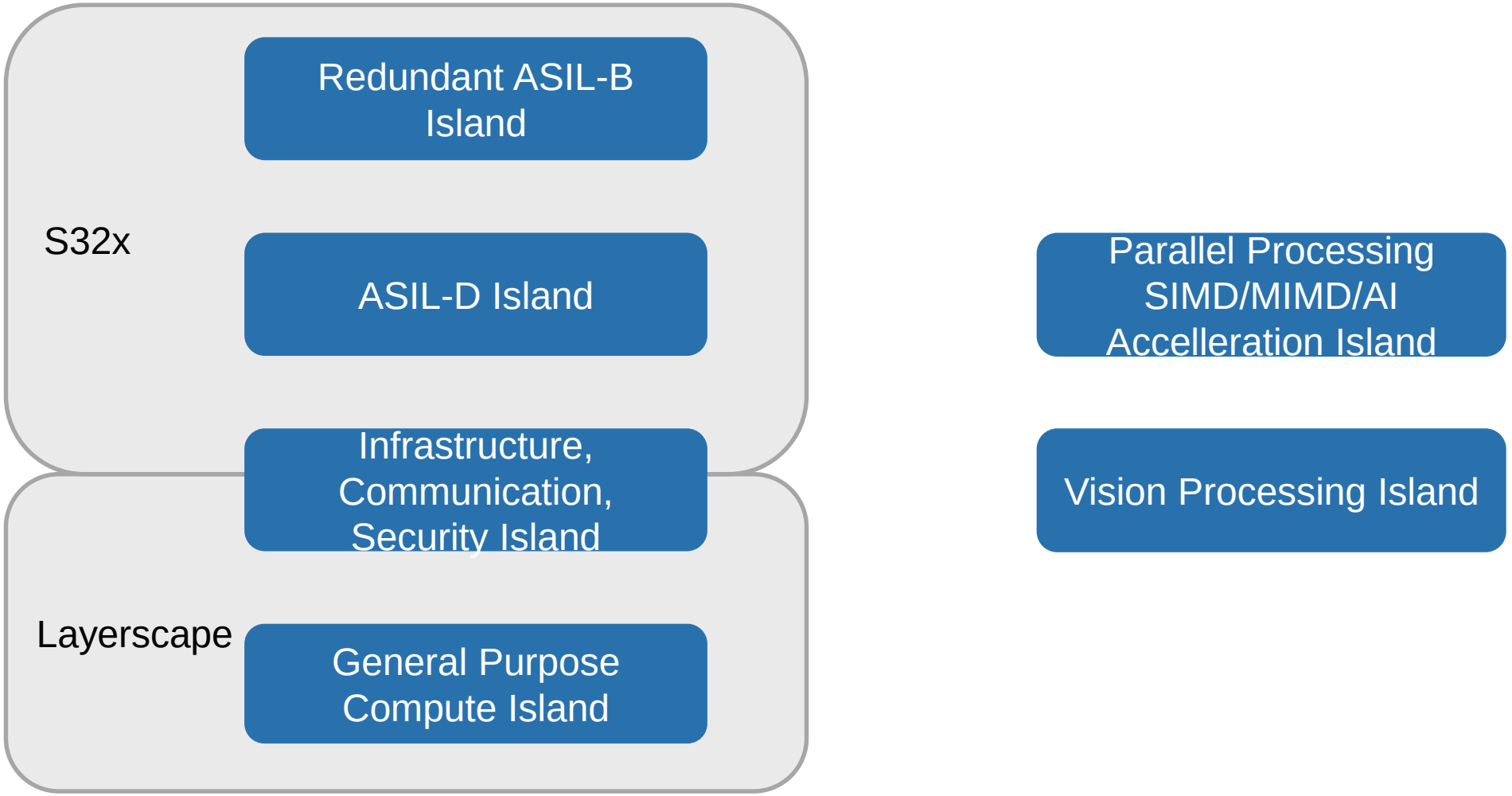


ADAS

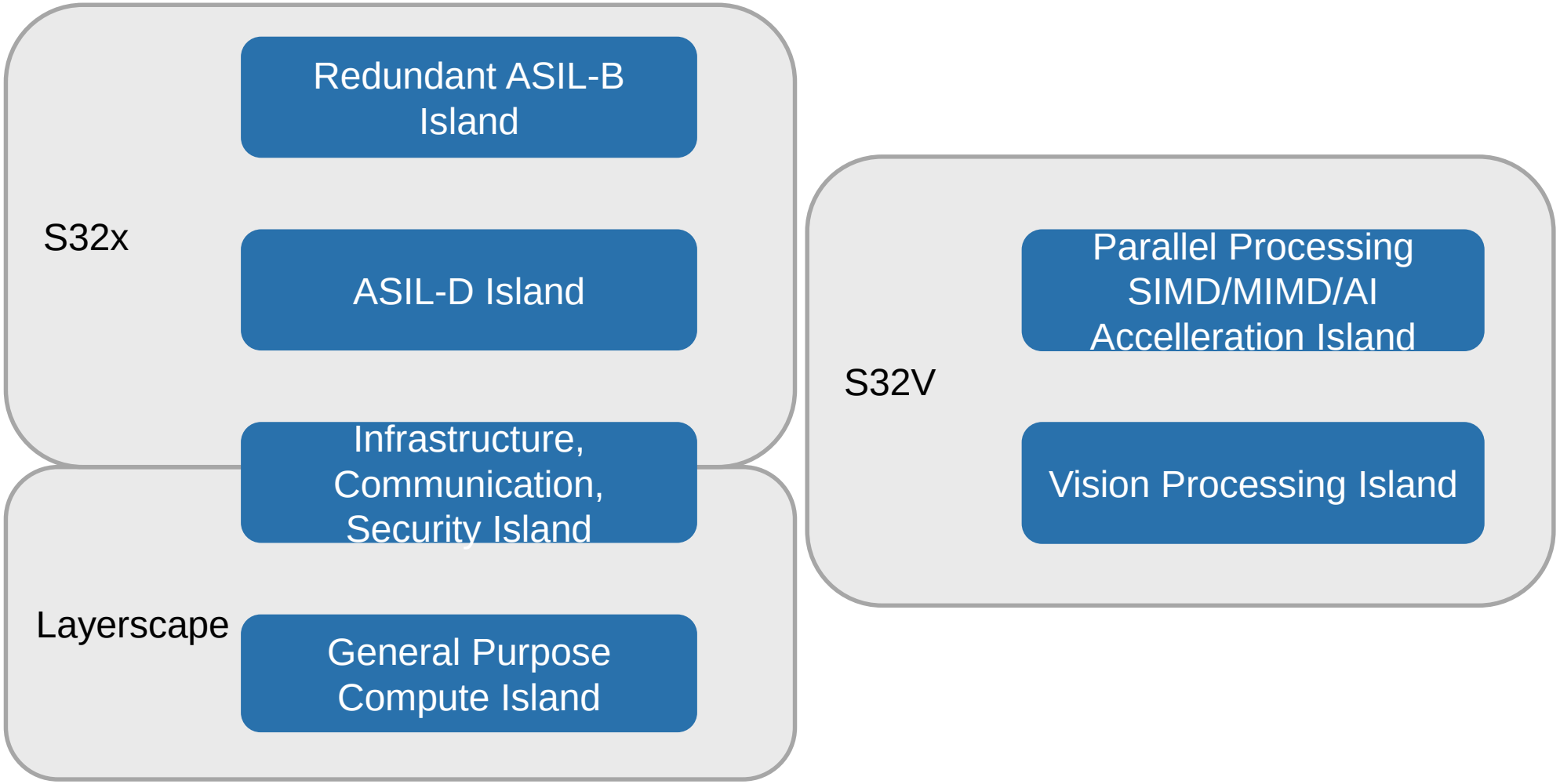
ADAS System Functional Building Blocks



Mapping of NXP Products to ADAS Functional Partitioning SOP 2022

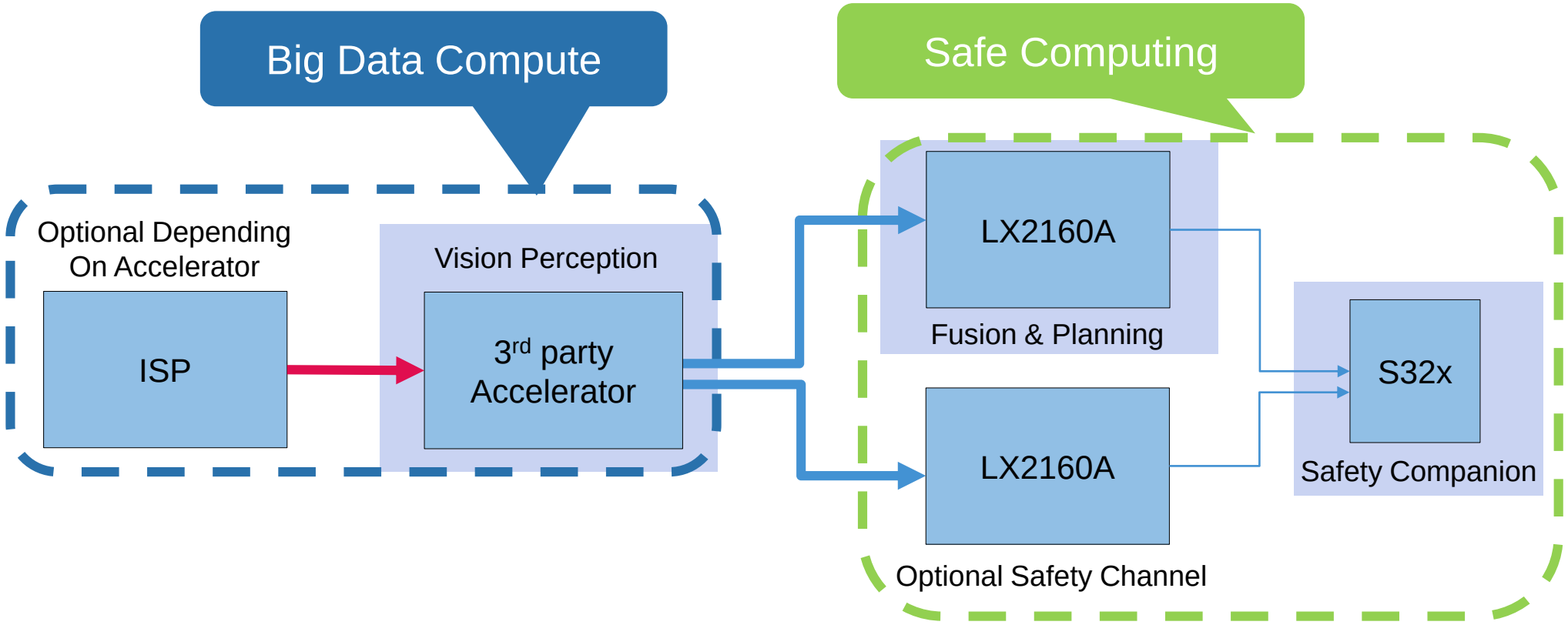


Mapping of NXP Products to ADAS Functional Partitioning SOP 2023



High Level Architecture

- Flexible architecture allowing various 3rd party accelerator based on customer needs
- Open SW standard based on proven embedded ARM architecture
- Expedite time to market

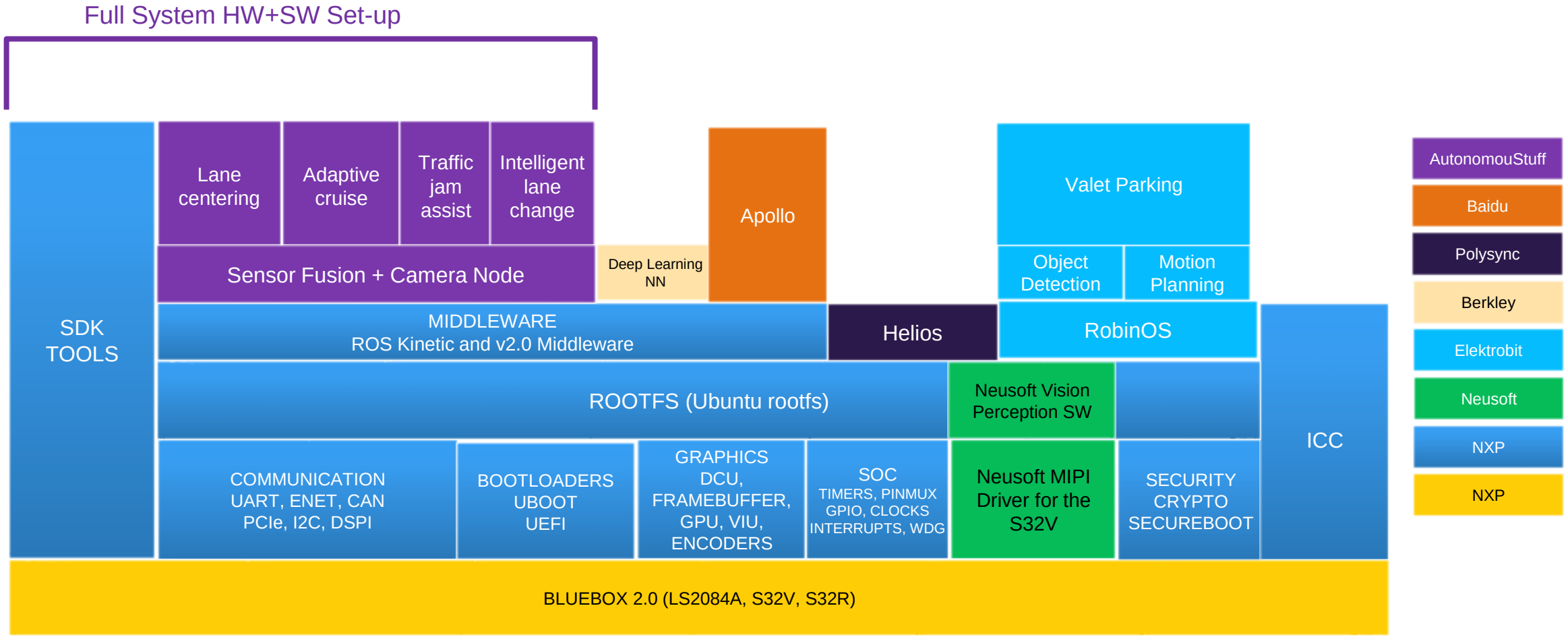


NXP BlueBox 2.0

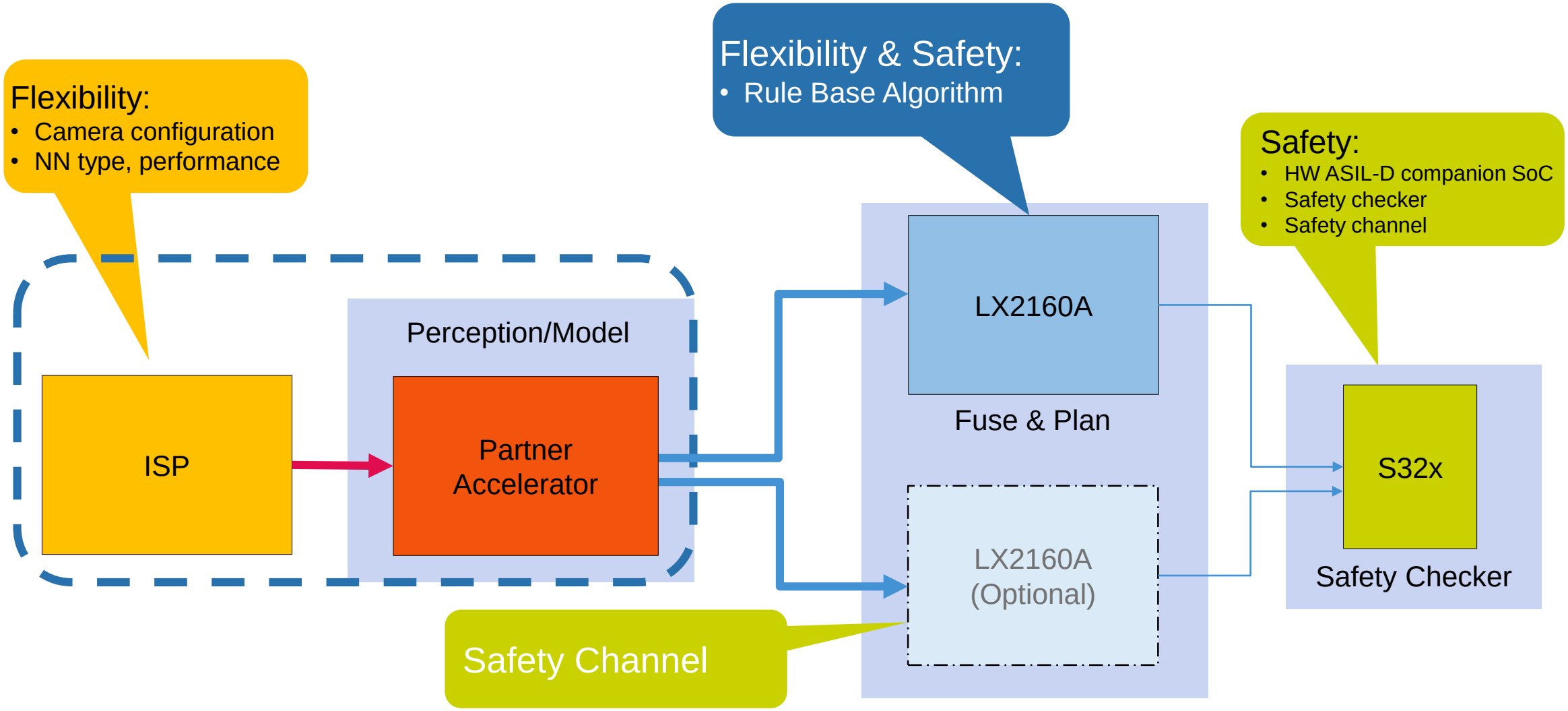
BlueBox 2.0 Inside

- LS2084A in the middle
- Two DIMM sockets
- S32V234 and camera i/f at top/left
- S32R275 at top right
- Automotive SSD
- IVN subsystem hidden under SSD

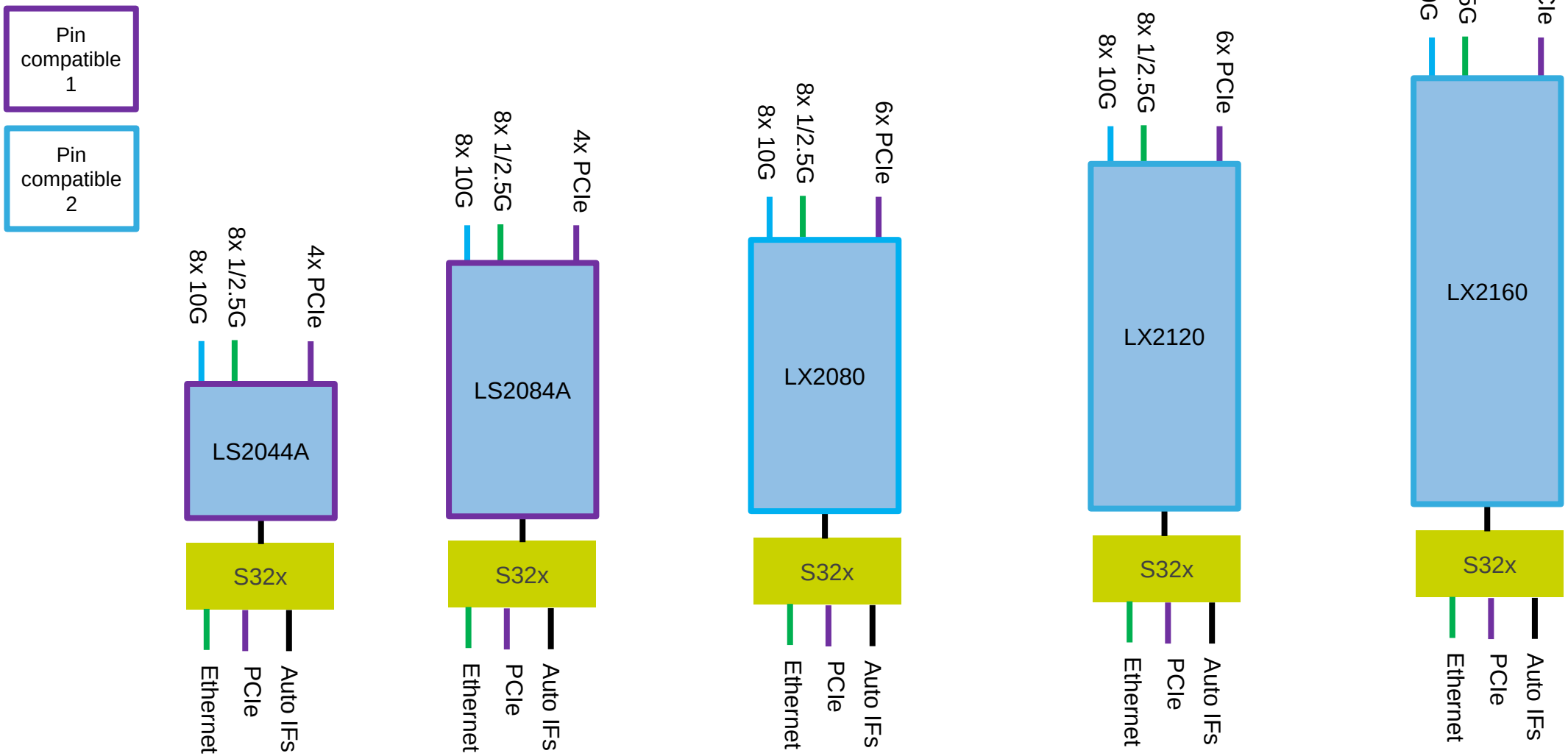
BlueBox 2.0 – NXP Software & Partners



BlueBox 3.0 High Level Concept



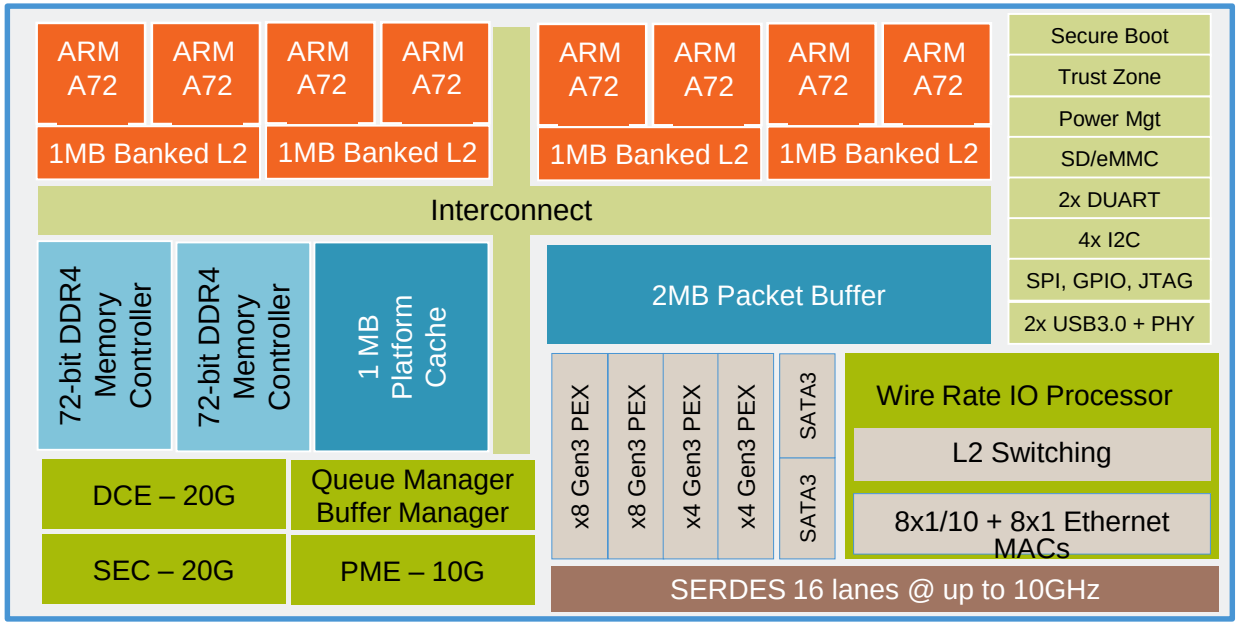
ADAS Planner Scalability



LS2/LX2 Scalability

	A72 Cores	Frequency	KDMIPS	SpecInt
LS2044	4	1.8GHz	43	SpecInt2k6 13.1, Rate 37.5
LS2084	8	1.8GHz	86	SpecInt2k6 13.1, Rate 75.1
LX2080	8	1.8GHz	86	SpecInt2k6 14.4, Rate 64.3
		2.0GHz	95	SpecInt2k6 16.0, Rate 71.5
		2.2GHz	105	SpecInt2k6 17.6, Rate 78.7
LX2120	12	1.8GHz	129	SpecInt2k6 14.4, Rate 96.5
		2.0GHz	143	SpecInt2k6 16.0, Rate 107
		2.2GHz	157	SpecInt2k6 17.6, Rate 118
LX2160	16	1.8GHz	172	SpecInt2k6 14.4, Rate 129
		2.0GHz	191	SpecInt2k6 16.0, Rate 143
		2.2GHz	210	SpecInt2k6 17.6, Rate 157

Layerscape LS2084A



Major Milestone	Schedule
Samples (Production Rev)	Dec 2017
Networking/Telecom Qualification	March 2018
AECQ100 grade 3 Qual on production rev	Nov 2018
PPAP Completion	Aug 2019

Auto Quality

- AEC Q100 Grade 3 (105C Tj)
- 15 years product longevity
- ZD-like approach to reduce risk of DPPM or Life failures
- Expected Operating Life fail rate <10 FIT
- Mission Profile: 10 years, 90C Tj-effective

Performance (Grade 3)

- ARM A72 x 8 @ 1.8 GHz
  - 86K DMIPS
  - SpecInt2k6 – 13.1, Rate -75.1
  - Neon SIMD in all CPUs
- 2x72b (w/ECC) DDR4 @ 1.8GT/s
  - 28.8GB/s memory BW
- High Speed IO
- Multiple PCIe Gen3 controllers
- Multiple Ethernet MACs (up to 10G)

Functional Safety

- Target ASIL-B*
- ECC protected memories
- Fault localization, containment and recovery
- Soft lockstep with determinism
- Excellent support for virtualization, containerization

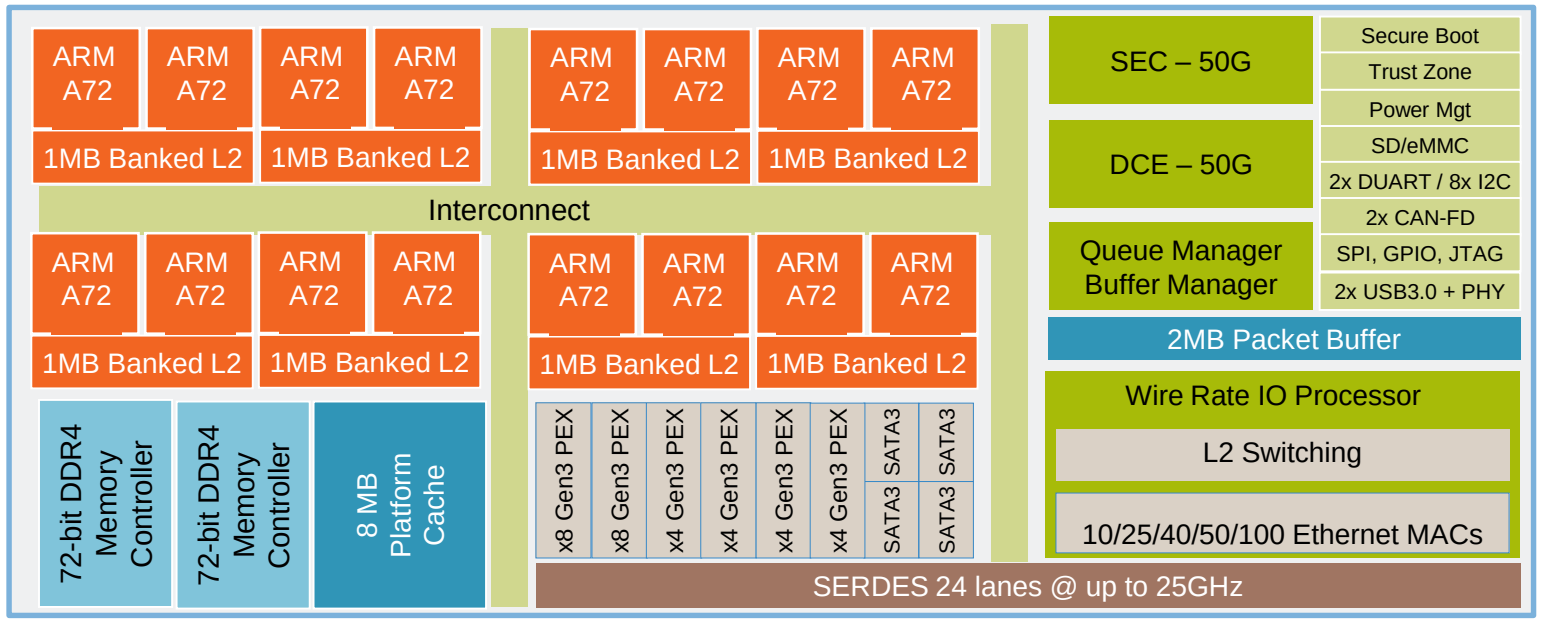
Process & Package

- 28HPM, ~40W Thermal Max @ 105C
- 37.5 x 37.5 mm, lidded FCBGA, 1mm pitch, 1292 pins

Security

- 20Gbps Crypto Acceleration
- MACSEC, IPsec, SSL
- Trust Architecture
  - Secure Boot
  - Secure Debug
  - Secure Storage
  - Tamper Detection
  - HW Enforced Partitioning
  - ARM Trust Zone

Layerscape LX2160A



Samples (Rev1): Now
Samples (Rev2): April 2020 (fully tested)
Telecom Production: May 2020
Auto Grade 3 & PPAP: Oct 2020

Auto Quality

- AEC Q100 Grade 3 (105 Tj)
- 15 years product longevity
- ZD-like approach to reduce risk of DPPM or Life failures
- Expected Operating Life fail rate <10 FIT
- Mission Profile: 10 years, 90C Tj-effective

Performance

- ARM A72 x 16 @ 2.2 GHz
  - ~201K DMIPS
  - SpecInt2k6 – 17.6, Rate -157
  - Neon SIMD in all CPUs
- 2x72b (including ECC) DDR4 up to 3.2GT/s
  - 51GB/s memory BW
- High Speed IO
- Multiple PCIe Gen3 controllers
- Multiple Ethernet MACs (up to 100G)

Functional Safety

- Target ASIL-B*
- ECC protected memories
- Fault localization, containment and recovery
- Soft lockstep with determinism
- Excellent support for virtualization, containerization

Process & Package

- 16FFC, ~25W Thermal Max @ 105C – 2.0GHz
- 40x40mm, Lidded FCBGA, 1mm pitch (1517 pins)

Security

- 50Gbps Crypto Acceleration
- MACSEC, IPsec, SSL
- Trust Architecture
  - Secure Boot
  - Secure Debug
  - Secure Storage
  - Tamper Detection
  - HW Enforced Partitioning
  - ARM Trust Zone

Layerscape in Automotive

- Highest CPU and IO performance SoCs in NXP
- Scalability – 1-16 ARM core SoCs
- Quality & Longevity – Best quality available in high performance processing. Many devices already on 15 year longevity program.
- Safety – We've demonstrated safety for mil/aero and other critical infrastructure applications. Working to prove ASIL-B equivalence with auto-centric collateral (FMEDA, Safety Manual).
- Security – Secure Boot, Secure Debug, Hardware Enforced Partitioning & Virtualization
- Software – SDKs with a very PC-like look & feel. Broad support in Linux, history of working with WindRiver, GHS, and QNX.

SECURE CONNECTIONS
FOR A SMARTER WORLD