MPC8569E-MDS-PB
HW User Guide

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MPC8569E-MDS-PB

Moduled Development System Processor Board

HW User Guide
Version 1.0

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Chapter 1:
General Information

1.1 Introduction

The MPC8569E MDS Processor Board (PB) is an application development system. The PB, used to verify the operation of the MPC8569E integrated communications processor, provides a high level of system performance characterization.

The MPC8569E-MDS-PB is used to demonstrate design-focused, electrical, circuit, and logical testing reflective of most customer applications. The PB enables the simultaneous operation and verification of interfaces and protocols found in specific market applications.

The MPC8569E integrates an e500v2 processor core (based on Power Architecture™ technology) with the system logic required for networking, telecommunications, and wireless infrastructure applications.

The terms PEX and PCIe are interchangeable. However, as the modules are stamped “PEX”, the document uses this term.

The MPC8569E is characterized by the following:

- High-performance e500v2 Power Architecture core with 36-bit physical addressing
- 512 KB of Level-2 cache
- HW and SW debug support
- 4 GETH interfaces (maximum of two with SGMII)
- IEEE 1588 v2 support
- Two DDR3/2 SDRAM memory controllers
- Enhanced Local Bus Controller (eLBC)
- High Speed Serial Interface (HSSI): two x1 (with message unit) and one x4 SRIO; x4/x2/x1 PEX; two SGMII
- Integrated Security Engine with XOR acceleration
- Programmable Interrupt Controller (PIC)
- I^2C buses: I2C1 & I2C2
- 4-channel Direct Memory Access (DMA) controller
- Debug port
- DUART (with optional QE UART)
- Full-speed USB 2.0 compatible interface
- QUICC Engine™ Block; four RISC processors support ETH, ATM, POS, T1/E1, and associated inter-workings

- Secure Digital card (SD) interface
- SPI interface

The MPC8569E is a member of the PowerQUICC™ family of devices. These devices combine system-level support for industry-standard interfaces with processors that implement Power Architecture technology.

The board support package (BSP) is built using the Linux operating system (OS). Developers using MPC8569E-MDS-PB onboard resources and debugging devices can perform the following:

- upload and run code,
- set breakpoints,
- display memory and registers,
- connect proprietary hardware for incorporation into a target system that uses MPC8569E as a processor, and
- use the MPC8569E-MDS-PB as a demonstration tool, i.e., developer application software can be programmed into the FLASH memory and run in exhibitions.

A SW application developed for the MPC8569E processor can run as a "bare bones" operation or with various input/output data streams, e.g., GETH, PEX, or SGMII connections.

Results can be analyzed using the *CodeWarrior*® debugger or with other methods that directly analyze input/output data streams.

1.2 Related Documentation

The MPC8569E-MDS-PB Hardware Getting Started Guide is required reading. A media copy is included in the HW Development Kit.

Table 1 lists documents available in the Freescale website to those with NDA Agreement access; the website is found at http://www.freescale.com/.

Table 1. Related Reading

Document	Description
CodeWarrior™ Kit Configuration Guide	Complete HW setup. The Kit Configuration Guide explains how to set up and use each SW component in the development kit.
MPC8569E PowerQUICC™ III Integrated Processor Hardware Specifications	MPC8569EEC
MPC8569E PowerQUICC™ III Integrated Processor Reference Manual	MPC8569ERM

1.3 Document Terminology

Table 2 provides a comprehensive list of MPC8569E-MDS-PB User Guide terminology.

Table 2. Definitions, Acronyms, and Abbreviations

Usage	Description
ADDR	Address
ADS	Application Development System
BCSR	Board Control and Status Register
BVDD	Local Bus Volt Direct Current
CCB	Platform Clock
CKE	DDR Clock Enable
CLKIN	Clock Input; interchangeable with SYSCLK
CLKOUT	Clock Output
CNTR ISP	Control PLD Integrated SW Programming
COP	Common On-Chip Processor
CPU	Central Processing Unit
CS	Component Side
DDR	Double Data Rate
DIP	Dual-in-Line Package (switches)
DUART	Dual Universal Asynchronous Receiver/Transmitter
e500	CPU Core Name
ECC	Error Detection and Correction
EEPROM	Electrical Erasable Programmable Memory
eLBC	Enhanced Local Bus Controller
EN	Enable
EP	End Point
ETH	Ethernet
FCM	NAND Flash Control Machine
FSL	Freescale Semiconductor
GETH	Gigabit Ethernet (also GbE)
GPCM	General Purpose Chip-Select Machine
Host	MPC8569E

Table 2. Definitions, Acronyms, and Abbreviations

Usage	Description
HRESET	Hard Reset
HW	Hardware
I^2C	Inter-Integrated Circuit multi-master serial computer bus
IDE	Integrated Development Environment
IO	Input/Output
IRSENSE	Service Voltage Drop Testing
JTAG	Joint Test Access Group (IEEE® Std. 1149.1™)
LED	Light-emitting Diode
LYNX	Internal terminology; interchangeable with SerDes
LVDD	QUICC Engine Block UCC1-UCC4 Voltage
MCK(E)	DDR Master Clock
MDIC	DDR Memory Driver Impedance Calibration
MEMC	Memory Controller
MMC	Multi Media Card
MPI	Metallized Particle Interconnect Matrix
NAND	FLASH Memory
NMI	Non-Maskable Interrupt
nMVRST	Marvell PHY Reset Signal
NOR	Flash Memory
PB	MPC8569E-MDS Processor Board
PCI	Peripheral Components Interconnect
PCIe	PCI Express = PCIe = PEX
PEX	PCI Express = PEX = PCIe
PHY	Physical Layer
PIB	Platform I/O Board
PLD	Programmable Logic Device
PLL	Phased Lock Loop
POST FA_AND	Service Failure Analysis
PRESET	Power-on-Reset
PS	Print Side

Table 2. Definitions, Acronyms, and Abbreviations

Usage	Description
PS ISP	PS Control PLD Integrated SW Programming
PTP	Precision Time Protocol
QE	Quick Engine
RC	Root Complex
RCW	Reset Configuration Word
REG CFG	Configuration Register
RGMII	Reduced General Media Independent Interface
RMII	Reduced Media Independent Interface
ROM	Read Only Memory
RTBI	Reduced 10-bit Interface
RTC	Real Time Clock
SD	Secure Digital Card
SDHC	Secure Digital High Capacity Card
SerDes	• Serializer/Deserializer • High Speed Serial Communication Lines; e.g., PEX (PCIe), SRIO, SGMII, etc.
SGMII	Serial Gigabit Media Independent Interface
SHMOO	Graphical representation of selected test parameters in an electronic circuit.
SMII	Serial Media Independent Interface
SODIMM	Mini DIMM Form Factor
SRESET	Soft Reset
SRIO	Serial RapidIO
SW	Switch
SYSCLK	System Clock; interchangeable with CLKIN
TAP	e.g., USB or ETH TAP
TDM	Time Division Multiplexing
TRIG OUT	Signal Trigger_Out
UART	Universal Asynchronous Receiver/Transmitter
UCC	Universal Communication Controller
UEM	Universal Ethernet Module

Table 2. Definitions, Acronyms, and Abbreviations

Usage	Description
UPC	Universal Programmable Controller
USB	Universal Serial Bus
V	Volt
VDD	Common Power Supply Terminals

1.3.1 Bit and Byte Definitions

Table 1-3. Bit and Byte Terminology

Bit		Byte	
Binary digit with a single binary value, 1 or 0. Commonly used for measuring the amount of data transferred in one second between two telecommunication points.		A unit of data, eight binary units long, that is used as a measure of computer processor storage and real and virtual memory.	
Kbps = Kbit	Kilobit per second (1 Kbps = 1000 bits)	Kbyte = KB = KByte	1 Kilobyte = 1024 bytes
Mbps = Mbit	Megabit per second (1 Mbps = 1,000,000 bits)	Mbyte = MB = MByte	1 Megabyte = ~ 1,000,000 bytes
Gbps = Gbit	Gigabit per second (1 Gbps = “billions of bits”)	Gbyte = GB = GByte	1 Gigabyte = ~ 1 billion bytes

1.3.2 Attributes Legend

Table 1-4. Attributes Legend

Attributes					
Options			Signals		Driver
R	W	Q	I	O	OD
Read	Write	Quiesce	Input	Output	Open Drain

1.4 MPC8569E-MDS Processor Board

1.4.1 Working Environment

See the Hardware Getting Started Guide or Kit Configuration Guide for HW preparations.

Table 1-5 features MPC8569E-MDS-PB working environment modes, configurations, and power options.

Table 1-5. MPC8569E-MDS-PB Working Environment Modes

Mode	Optional Expansion	Description
Standalone PEX RC	Includes the noted modules: • GETH3 & 4 UEM • SerDes Lane e, f SRIOx1 or UEM (SGMII mode) • SerDes Lane a, b SRIOx1 • SerDes Lane a, b PEXx2 • 1xDDR3 SODIMMx64 or 2xDDR3x32 SODIMM	• PB powered, via P2, by an external 5V power supply (included in kit). • [Option] PEX EP powered, via P2 of PEXx2, by an external 12V power supply.
PIB-combined Mode MPC9569-MDS-PB on PIB	Includes the noted modules: • GETH3 & 4 UEM • SerDes Lane e, f SRIOx1 or UEM (SGMII mode) • SerDes Lane a, b SRIOx1 • SerDes Lane a, b PEXx2 • 1xDDR3 SODIMMx64 or 2xDDR3x32 SODIMM	• PB powered from PIB via bottom riser connectors. • [Option] PEX EP powered, via P2 of PEXx2, from an external 12V power supply.

1.4.2 Board Features

The MPC8569E-MDS-PB supports an MPC8569E characterized by the following:

- runs at a maximum of 1.33 GHz
- 1.1V core voltage
- maximum QUICC Engine frequency of 667 MHz.

The device package is a 783-pin, Flip-Chip PBGA of 29x29 mm pitch; its estimated power will not exceed 7W.

Table 1-6. MPC8569E-MDS-PB Features List

Feature	Description
DDR2/3 SDRAM	• One SODIMMx64 of 1GB • OR, two SODIMMx32 at 512MB each
Debug Port	• Access via dedicated 16-pin COP connector or a PCI port
eLBC Interface	• 32 MB (expandable) NOR FLASH with 8-bit port size in a socket • 32 MB NAND FLASH with 8-bit port size in a socket • Address Latch, Mux, Data, and control buffers • CPLD-mapped Board Control and Status Register (BCSR)
High-speed Risers	• Connect to an add-on communication board PIB or PCI-PEX adaptor.
I^2C Buses: I2C1 & I2C2	• I^2C Bus 1: 256 KB Boot EEPROM, real-time clock (RTC), DAC for Power SHMOO, and SODIMM SPD EEPROM • I^2C Bus 2: 1 KB BRD EEPROM and UEM optional control
RTC	• On-board battery-powered
SD	• Connector

SerDes Connectors	• High-speed
	• Connected to the following:
	  • Two SRIO x1(with message unit) OR one x4 interface
	  • PEX (x4/x2/x1)
	  • Two SGMII

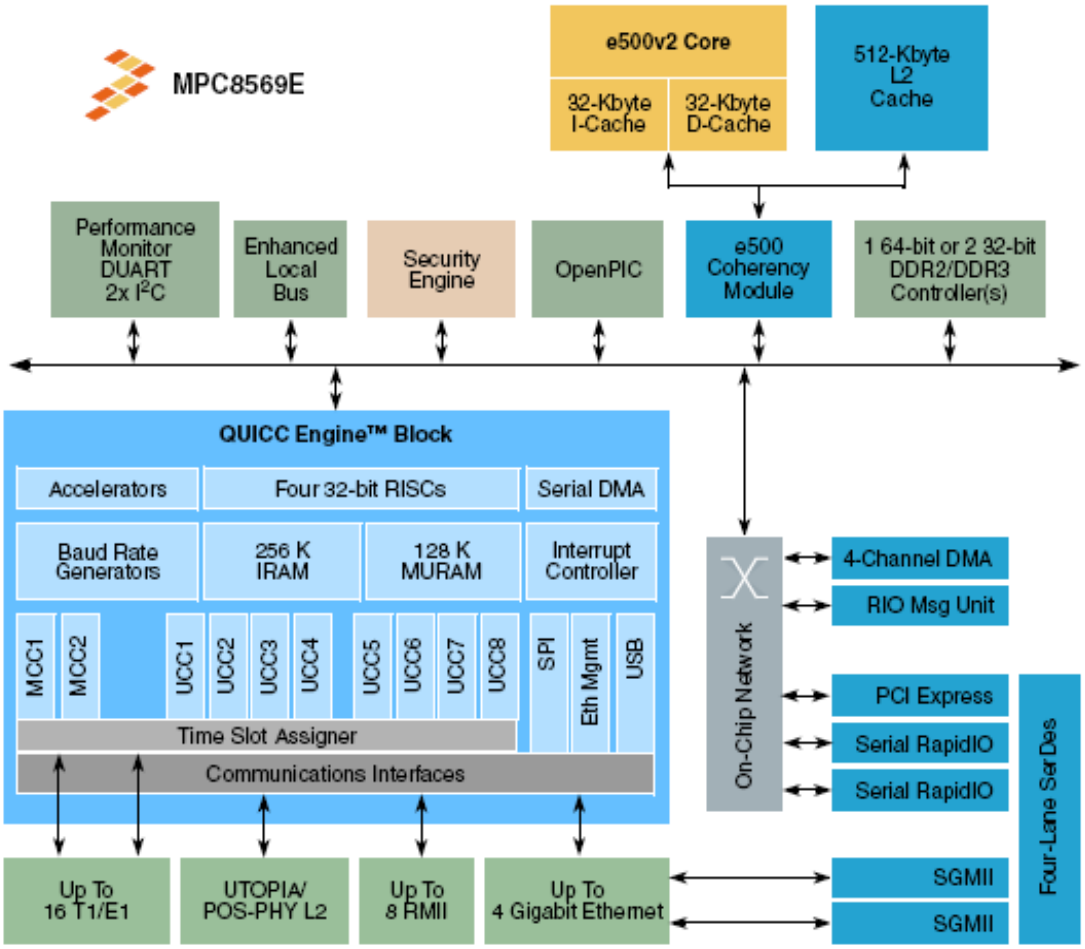
SHMOO	• Automatic testing capabilities provide core voltage, and clock changing; clock is PIB-controlled.
SPI FLASH	• 4 Mbit
Transceiver: Dual RS232	• DUART port with optional QE UART interconnection
Transceiver: USB Serial	• Low-speed 1.5 Mbit • Full-speed 12 Mbit

1.5 Block Diagrams

1.5.1 MPC8569E Processor

Figure 1-1 illustrates the MPC8569E processor block diagram.

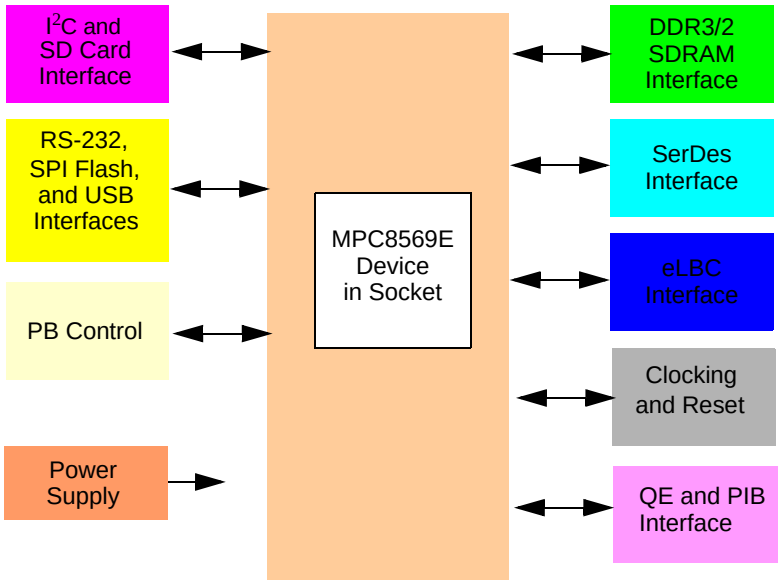
Figure 1-1. MPC8569E Processor Block Diagram



1.5.2 MPC8569E MDS Processor Board Block Diagram

Figure 1-2 illustrates the MPC8569E-MDS-PB block diagram; its interfaces and functions are detailed in Chapter 4, Functional Description.

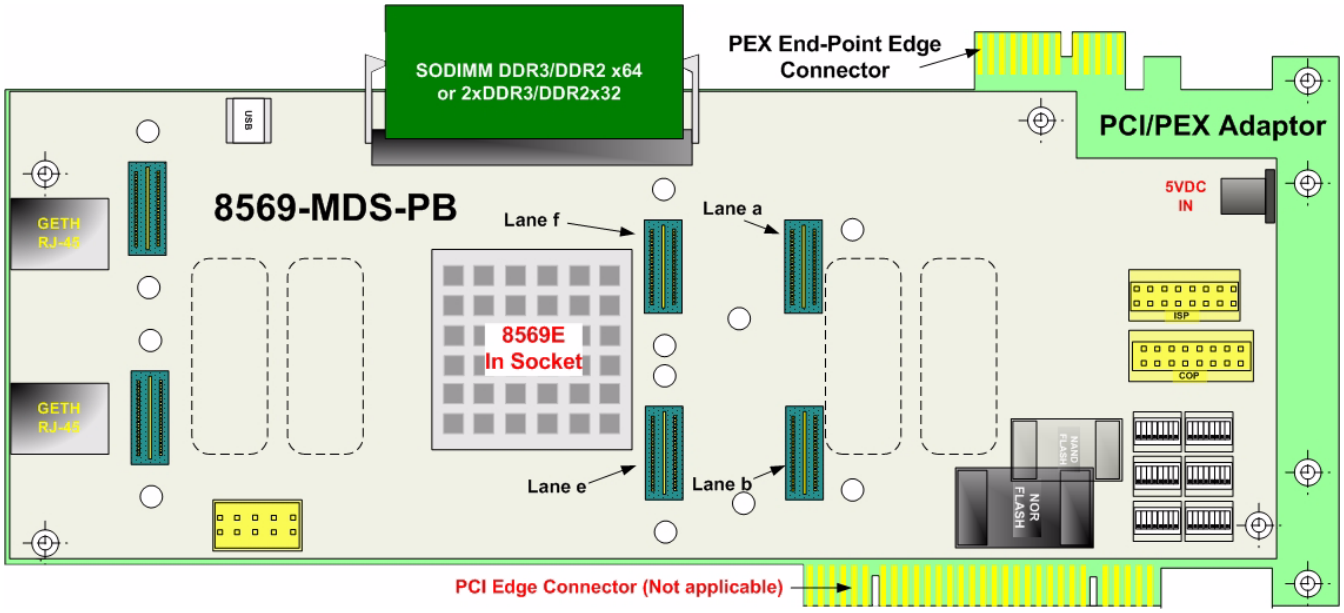
Figure 1-2. MPC8569E-MDS-PB Block Diagram



1.6 PB Component Placement

Component placement, using a piggyback form-factor set-up, complies with the current PIB-PB concept. Use the existent PCI/PEX adaptor, 084-00331-2, to provide PEX EP device functionality.

Figure 1-3. Preliminary PB Component Placement



1.7 Specifications

Table 1-7 lists PB specifications.

Table 1-7. MPC8569E MDS Processor Board Specifications

FEATURE	SPECIFICATION	DESCRIPTION
Process Technology[a]	SOI	• 45-nm
Package[b]	Flip-Chip PBGA	• 783-pin • 29x29 mm pitch
Power Requirements	Standalone	• Independent Host, or as PEX or Agent (not in PC): 5V @ 8A external DC power supply.
	PIB-combined Mode	• PIB-powered
	PC Mode	• PC-supplied power
Power Consumption	Core	• Less than 7 W at 800MHz at VDD=1.0V
Supply Voltages	Core	• 1.0 V and 1.10 V
	PEX and SRIO	• 1.0 V and 1.10V
	Ethernet	• 3.3 or 2.5 V • Subject to protocol
	Local bus	• 3.3 V
	DDR2	• 1.8 V (conforms to JEDEC standard)
	DDR3	• 1.5 V (conforms to JEDEC standard)
Processor	MPC8569E	• Internal clock runs at 1.33 GHz @ 1.1V core voltage • Maximum QUICC Engine frequency of 667 MHz
Memory	DDR3/2 Bus	• 1 GB space, 64-bit wide in one SODIMM-204 DDR3, OR 2x512KB, 32-bit wide on two SODIMM-204 DDR3 • Data rate 800 MHz
Local Bus	Buffered Memory: NOR FLASH on socket	• 32 MB space, 8-bit wide
	Buffered Memory: NAND FLASH on socket	• 32 MB space, 8-bit wide
	BCSR on CPLD	• 18-registers, 8-bit wide
	Expansion	• Four banks: 16-bit address bus and 16-bit data bus connected to riser connectors

Table 1-7. MPC8569E MDS Processor Board Specifications

FEATURE	SPECIFICATION	DESCRIPTION
Environmental Conditions	Operating Temperature	• 0°C to 70°C
	Operating Junction Temp (Tj)[c]	• 0°C to 105° C
	Storage Temperature	• -25°C to 85°C
	Relative Humidity	• 5% to 90% (non-condensing)
Dimensions (without heat-sink): per PCI 64-bit add-in card form factor	Length	• 285 mm
	Width	• 110 mm
	Height	• 45 mm

[a] Relates to the processor, not the processor board.
[b] Same as above footnote.
[c] Same as above footnote.

Chapter 2:
Hardware Getting Started

2.1 General

The MPC8569E-MDS-PB Getting Started Guide explains and verifies PB basic operations in a step-by-step format. The Getting Started Guide is required reading and is found in the HW Development Kit in CD-ROM media format.

Switch, connector, push button, and LED settings are illustrated and described in the Getting Started Guide. Instructions for connecting peripheral devices are also included.

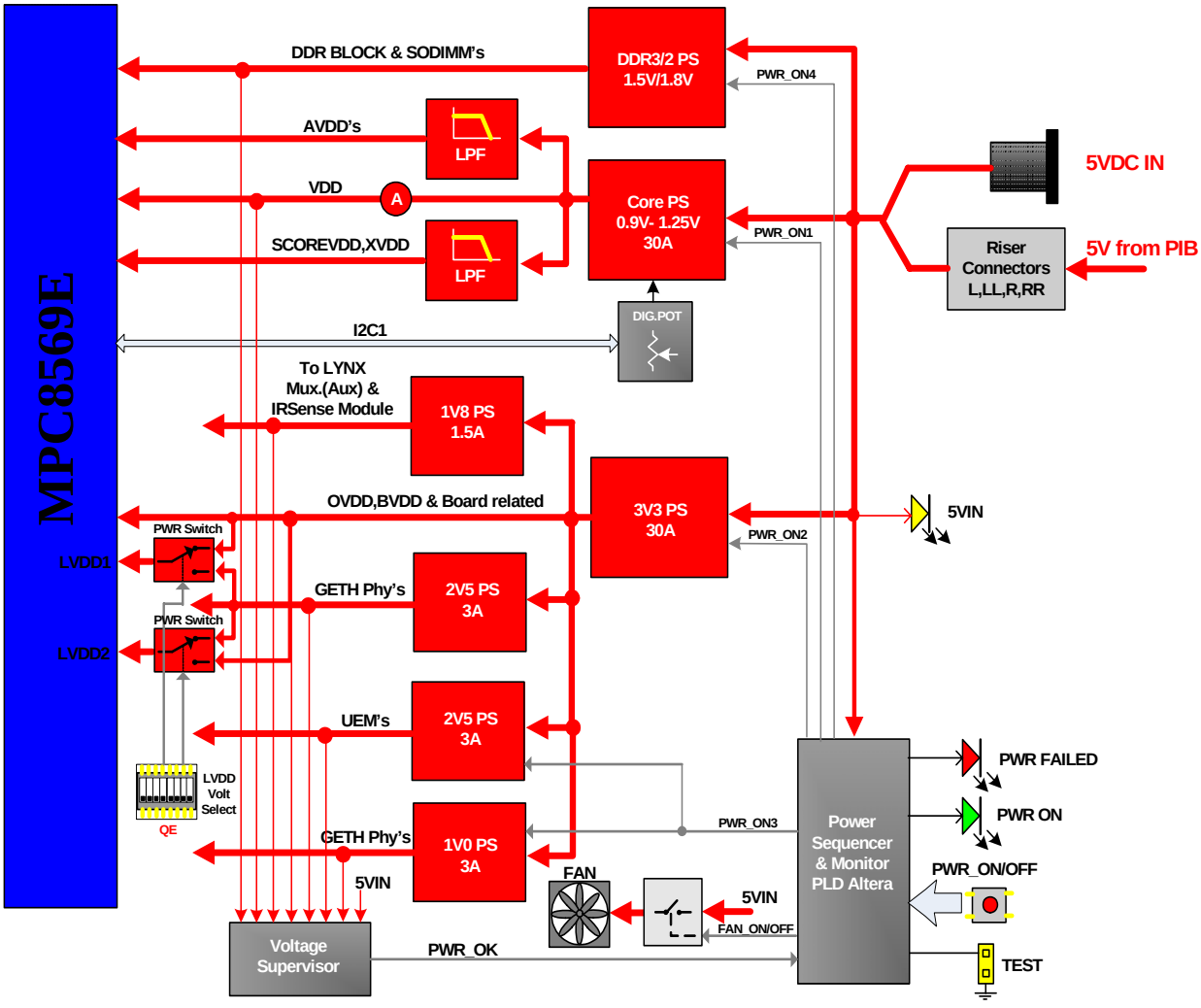
The MPC8569E MDS Processor Board functions with an integrated development environment (IDE), such as Freescale's *CodeWarrior*™.

Instructions for working with an IDE are beyond the scope of this document.

Chapter 3:
Power Supply

The MPC8569E-MDS-PB power supply provides all the voltages necessary for correct operation of the MPC8569E and all onboard peripherals. Figure 3-1 illustrates the power supply block diagram.

Figure 3-1. Power Supply Block Diagram



3.1 Primary Power Supply

Table 3-1 outlines MPC8569E-MDS-PB power supply options while Table 3-2 notes Sceptre external power supply specifications.

Table 3-1. Power Supply Options

Set-up	Power	Description
PB Standalone	40W	• standard CE/UL-approved 40W primary power supply
PB on PIB	5V	• PIB onboard power supply provides primary 5V voltage to the PB
External Power Supply	5V DC input	• required by PB-mounted secondary power supplies • Sceptre PS-5080APL05

Table 3-2. Sceptre 5V External Power Supply

Power Supply	Description
External 5V standard	• Vin = 100 - 250V AC • Fin frequency = 47 - 63Hz • Iin $\leq$ 1.5A • OUTPUT 40W max. = 5V DC out ± 5% @ 8A

3.2 PB Power Supply Structure

Table 3-3 lists power supply devices. Devices include visual indications and power sequence functions.

Table 3-3. MPC8569E-MDS-PB Power Supply Devices

Power Supply Device	Description
Texas Instruments: PTH05T210WAD (U5)	Programmable Power DC/DC module produces MPC8569E core/PLL voltages: • V_{DD} = 0.9 -1.25V with step 2mV • Rated voltage = 1.2V • Iout <=30A
Texas Instruments: PTH05T210WAD (U13)	Power DC/DC module produces 3V3 voltage for MPC8569E and general on-board components: • OVDD, BVDD, etc. = 3.3V • Iout <=30A
Texas Instruments: TPS51116PWP (U75)	Synchronous DC/DC converter produces all required DDR3 SDRAM voltages: • GV_{DD} = 1.8/1.5V and Iout <=10A • Vtt = 0.9/0.75V and Iout <=3A • Vref = 0.9/0.75V and Iout <=10mA

Table 3-3. MPC8569E-MDS-PB Power Supply Devices

Power Supply Device	Description
Linear Tech: • LT1764-2.5 Micrel: • MIC49300WR • MIC37139-1.8YS	Set linear regulators provide all necessary ETH PHYs, UEMs, and corresponding MPC8569E voltages: • 2.5V DC @3A • 1.0V DC @3A • 1.8V DC @1.5A
Texas Instruments: TPS2115 (U98, U109)	Two power switches select 2.5V or 3.3V for MPC8569E LVDD1 and LVDD2 power inputs.
Maxim: MAX16006_TG+ (U80)	Octal voltage supervisor determines “power-good” status of all onboard secondary supply voltages.
Altera: EPM7064STC44-10N PLD (U84)	Control circuits based on this power supply device provide: • Needed quantity of onboard secondary PS ON/OFF signals. • Additional heat sink fan ON/OFF signal. • Visual indication. • Power sequence functions. • Auxiliary test mode identifies non-functioning onboard power supplies. • Auxiliary test mode cancels “power-good” signal monitoring. • Start/Stop Power-ON condition watchdog. • Added time interval, between Power-OFF and Power-ON cycles, that discharges bulk capacitors located on all secondary onboard power supplies outputs.

3.3 Power Supply Operation

3.3.1 Power-ON

The primary power source provides 5V0 voltage when connected to an AC power outlet. The voltage powers onboard power supply PLD control circuits (U84).

Power-ON process steps are described in Table 3-4 and illustrated in Figure 3-2.

Table 3-4. Power-ON Process

Step	Stage	Description
1	Supplied Voltage	• 5V0
2	Auxiliary Reset Controller (U12)	• produces a reset signal that resets the PLD
3	Yellow LED “5VIN”	• indicates power supply ready status • no other voltages are present on the PB
4	ON/OFF Button	• push button
5	PLD	• sends a PS_ON signal to all onboard power supplies to produce all voltages • see Table 3-3

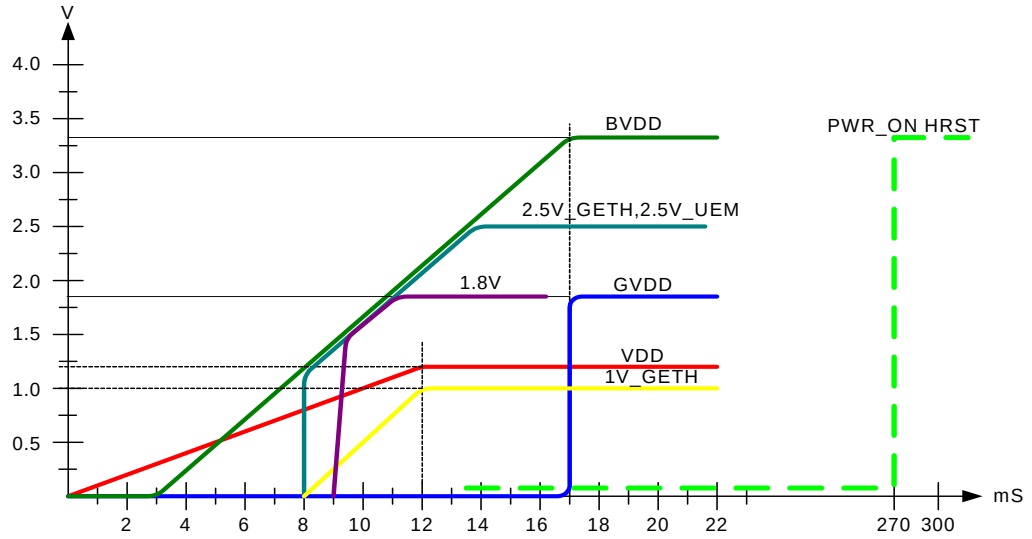
Table 3-4. Power-ON Process

Step	Stage	Description
6	Transients	• completes all transients
7	Octal Voltage Supervisor	• produces PWR_OK signal • informs PLD-mapped control circuits that all output voltages are in good condition

8	MPC8569E Power Rails	• must be applied in a given sequence to ensure proper device operation
		• all power supplies reach stable values within 18ms
		• concurrently, PLD-mapped WatchDog circuits begin (T~20mS) monitoring the Power-ON condition
		• power-up requirements are as follows:
		  • VDD
		  • AVDD_*n*
		  • BVDD
		  • LVDD*n*
		  • OVDD
		  • SVDD
		  • XVDD
		  • GVDD

9	Success	• each power supply's "power-good" signal stops the WatchDog • green "PWR_ON" LED is illuminated
	Failure	• WatchDog sets the power-failed flip-flop (PLD-mapped) • indicated by the red "PWR_Failed" LED • resets Power-ON/OFF flip-flop (PLD-mapped) that cancels the PS_ON signal to the onboard power supplies; the latter are switched off
	Repeat ON Switching	• only after reconnecting the external power supply to the AC outlet

Figure 3-2. Power-Up Voltage Sequence



3.3.2 Power-OFF

Power switches off when,

- PB is in Power-ON status (“PWR_ON” LED is illuminated), and
- ON/OFF button is activated, as
- PLD-mapped Power-ON/OFF flip-flop cancels PS_ON signal to all on-board power supplies.

3.3.3 Over-Current, Voltage, and Temperature Protection

The external primary power supply and all onboard power supply regulators have embedded, over-current, over-voltage, and over-temperature protection.

3.3.4 Current Measurement

Allegro’s Bidirectional 1.5 mohm Hall-Effect-Based Linear Current Sensor (ACS712ELCTR-20A-T) measures the amount of current consumed by the core.

The Allegro sensor is characterized by the following:

- precision, low-offset, linear, Hall sensor circuit;
- sensor circuit with a copper conduction path located near the die surface;
- applied current flows through the copper conduction path and generates a magnetic field that is sensed by the integrated Hall IC and converted into a proportional voltage; and,
- measurement results represented by the following formula,
  Icore(A)=[Vout(mV)-2500]/100; Tolerance <=10%

3.3.5 Auxiliary Function

The optional auxiliary function is remote PB Power-ON/OFF functionality—with each “short”, the PB toggles between Power-ON/OFF.

Activate the function as follows:

- connect J8 pins with any “dry” contact-like relay; or,
- connect J8 pins (J8/1: GND and J8/2: "+") with any NPN or FET transistors.

3.4 Voltage Regulation

3.4.1 Core and PLL Voltage

Simultaneously adjust V_{DD} and AV_{DD} voltages, within the range of 0.9-1.25V, as follows:

- Manually adjust the potentiometer (R5); this change creates a new default value that is unaffected by Power-ON/OFF.
- Software-related voltage adjustments, made via the I^2C1-mapped digital potentiometer (U73), revert to the factory default (1.1V) following each Power-ON.

3.4.2 DDR Voltage

DDR SDRAM GV_{DD}, termination (V_{TT}), and reference (V_{REF}) voltages are automatically set within the following limits:

- DDR3 default GV_{DD} value is 1.5V.

Voltages are automatically set to appropriate values after Power-ON.

3.4.3 GETH Voltage

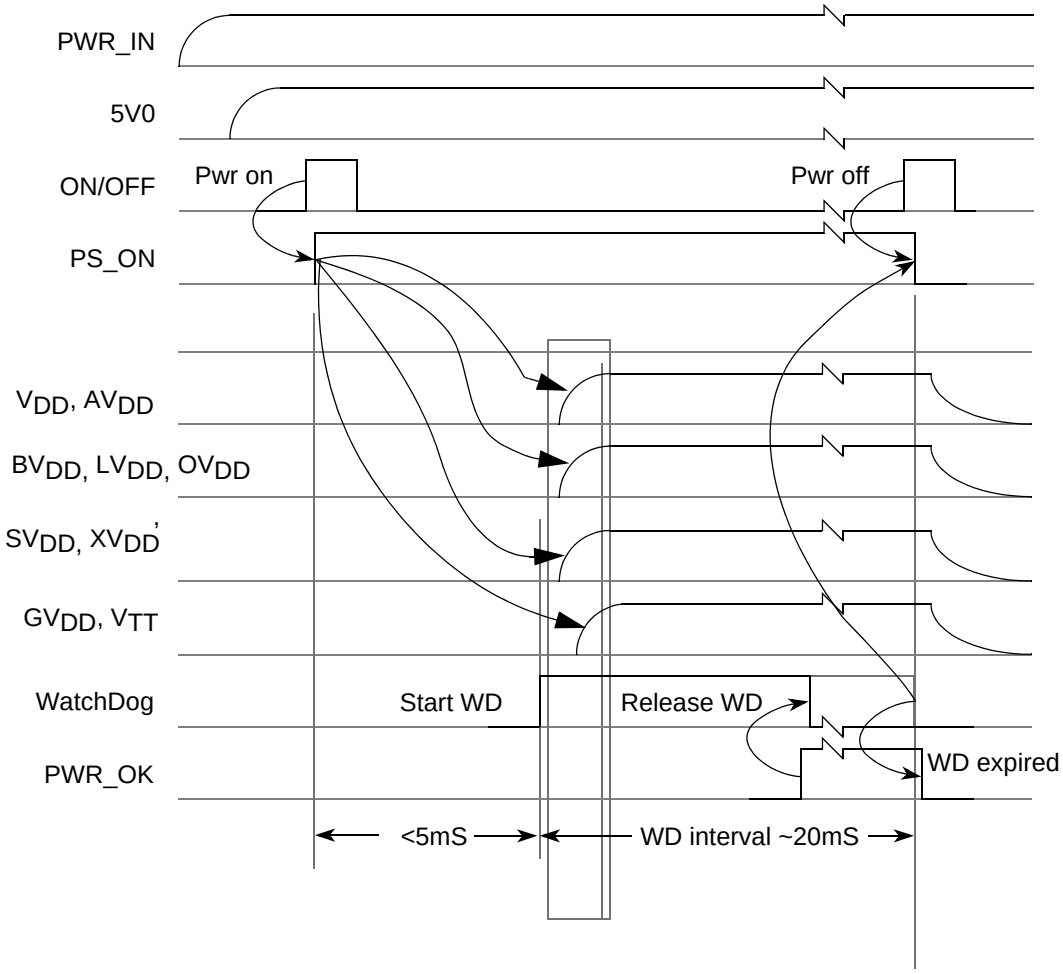
Each MPC8569E GETH pin (LVDD1 and LVDD2) voltage can be switched to 2.5V or 3.3V.

- Onboard DIP switches (SW6/7 and 6/8) control the TI TPS2115 (U98, U109) power switch.
- TI power switch (U109 or U98) selects the voltage.

3.4.4 Power Sequence

Figure 3-3 illustrates the power supply power sequence.

Figure 3-3. Power Supply Power Sequence



Chapter 4:
Functional Description

4.1 Clocking

4.1.1 Clock Architecture

Figure 4-1 illustrates a detailed PB clocking system block diagram.

Figure 4-1. PB Clocking System Block Diagram

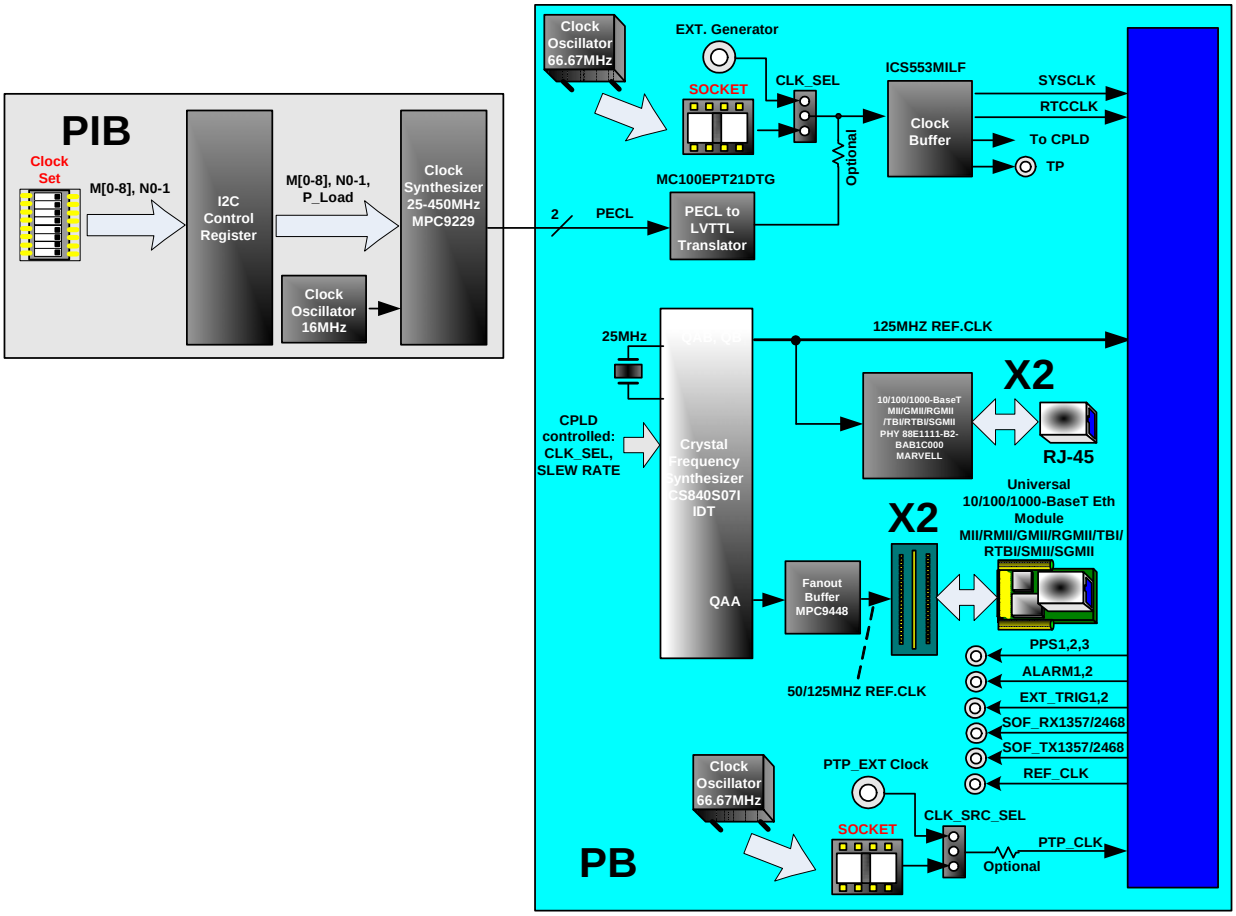


Figure 4-2 shows how the PB clocking system sends required clock signals to the MPC8569E clock subsystem.

Figure 4-2. MPC8569E Clock Subsystem Block Diagram

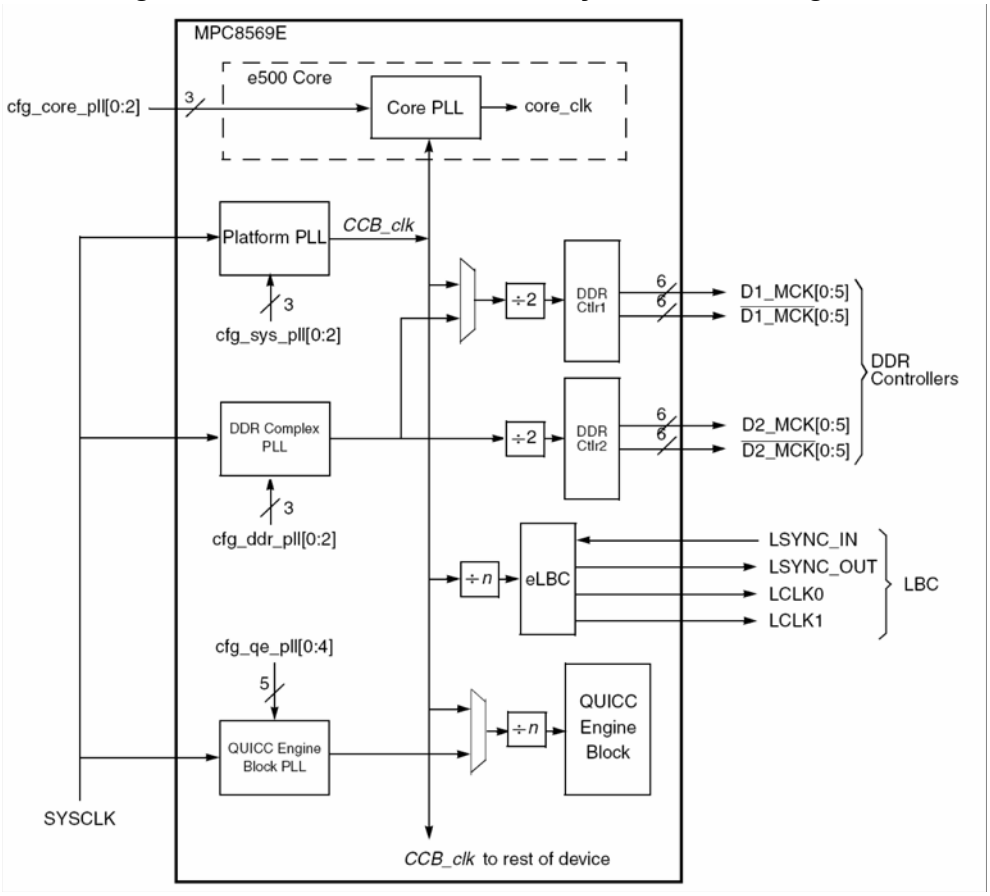


Table 4-1 describes two MDS clock distribution options, PB-on-PIB and standalone modes.

Table 4-1. MDS Clock Distribution Options

Clock Mode	Hardware	Description
PB on PIB	IDT MPC9229 (PIB-assembled)	1. Clock synthesizer supplies system clock to the PB within the 25 - 450 MHz range. 2. Synthesizer output (differential PECL) clock is routed to an On-Semi Translator (U104). 3. Clock output is converted to CMOS and distributed to MPC8569E auxiliary inputs (SYSCLK and RTC) via an IDT (U50) low skew, fan-out buffer with a maximum frequency of 200MHz.
	On-Semi MC100EPT21DTG Differential LVPECL to LVTTL Translator (U104)	
	IDT ICS553MILF (U50)	

Table 4-1. MDS Clock Distribution Options

Clock Mode	Hardware	Description
Standalone	MTRON socketable clock oscillator (66.66-133.33 MHz)	• [Option] Use an external clock generator if the CLK SEL jumper is set to the appropriate position. • Measure the clock using the clock signal test point. • IDT Frequency Synthesizer supplies both onboard GETH PHYs and the MPC8569E with reference clock signals of 125MHz with cycle-to-cycle jitter below +/-100ps. • UEM modules receive reference clocks (50/125MHz) from the same synthesizer via another fanout buffer (U103).
	External Clock Generator	
	IDT ICS840S07I (U21) Crystal-to-LVCMOS/LVTTL Frequency Synthesizer	

- Use an additional socketable clock oscillator to provide PTP IEEE1588 functionality.
- All corresponding 1588 RTC signals have service access via corresponding test points; see Table 4-4 for all related PTP signals.
- Use an external clock generator if J18 (CLK_SRC_SEL) is set with pins 1-2 shortened.

4.1.2 Clock Control

PIB-assembled clock synthesizer programs its output through an 11-bit parallel interface. This PIB-enabled function is achieved by setting DIP-switches to a desired value or via the I2C2 bus.

The PB-assembled GETH Frequency Synthesizer is mode-programmed via a BCSR that is mapped onto the onboard CPLD.

4.1.3 Clock-Out Parameters

The PIB-assembled clock synthesizer produces clock signals with a period jitter of $\leq \pm 25$ pS; see Table 4-2.

Table 4-2. Clock-out Parameters

Output Frequency Range (MHz)	Frequency Step (MHz)
25 – 56.25	0.125
50 – 112.5	0.25
100 – 225	0.5
200 – 450	1.00

The clock fanout buffer (U50) supplies clock signals to the MPC8569E. The clock signals have the following parameters:

Table 4-3. Clock Signal Parameters

Output Frequency Parameters	Values
Output Clock Frequency Range	• 0 – 200 MHz
Clock Skew	• ≤ 50 pS
Cycle-to-Cycle Worst Case Jitter (defined by clock oscillator)	• <110 pS
Output	• each output drives a 50 ohm series terminated transmission line
Output Rise/Fall Time	• <0.7 nS
GETH Clock Synthesizer with Output Clock Jitter	• (at any frequency) of <100pS

Table 4-4 details PTP signals.

Table 4-4. PTP Signals (1588 RTC External Signals)

Signal Name	I/O	Timing	Description	Parallel Port Signal Pins
PTP_PPS1	Output	Transitions synchronously in phase & frequency with respect to PTP_REF_CLK.	• PPS output signal generated by configuring the TMR_FIPER1 register. • Every time the FIPER1 value expires, one RTC clock period pulse is generated.	CE_PE24
PTP_PPS2	Output	Transitions synchronously in phase & frequency with respect to TP_REF_CLK.	• PPS output signal generated by configuring the TMR_FIPER2 register. • Every time the FIPER2 value expires, one RTC clock period pulse is generated.	CE_PC23
PTP_PPS3	Output	Transitions synchronously in phase & frequency with respect to PTP_REF_CLK.	• PPS output signal generated by configuring the TMR_FIPER3 register. • Every time the FIPER3 value expires, one RTC clock period pulse is generated.	CE_PB31
PTP_ALARM1	Output	Asynchronous signal	• Alarm output trigger: set if the timer value reaches the TMR_ALARM1 register value.	CE_PE25
PTP_ALARM2	Output	Asynchronous signal	• Alarm output trigger: set if the timer value reaches the TMR_ALARM2 register value.	CE_PB30
PTP_REF_CLK	Output	-	• Divided output clock is generated by dividing the timer clock. • TMR_PRSC register is configured to the division factor.	CE_PC29
PTP_EXT_TRIG1	Input	Asynchronous signal	• Input trigger to capture time stamps. • Captured time stamp value is stored in TMR_ETTS1L/TMR_ETTS1H.	CE_PE26

Signal Name	I/O	Timing	Description	Parallel Port Signal Pins
PTP_EXT_TRIG2	Input	Asynchronous signal	• Input trigger to capture time stamps. • Captured time stamp value is stored in TMR_ETTS2L/TMR_ETTS2H.	CE_PB28
PTP_CLK	Input	-	• External oscillator RTC.	CE_PC28
PTP_SOF_RX1357	Input	Transitions synchronously with respect to the RX Serial Clock.	• Input trigger to capture time stamps for each frame received in one of UCC1/UCC3/UCC5/UCC7 instead of time stamping according to SFD detection. • Captured time stamp value is stored in TMR_UC1_RXTS_L/TMR_UC1_RXTS_H.	CE_PB26
PTP_SOF_TX1357	Input	Transitions synchronously with respect to the TX Serial Clock.	• Input trigger to capture time stamps for each frame transmitted by one of UCC1/UCC3/UCC5/UCC7 instead of time stamping according to SFD detection. • Captured time stamp value is stored in TMR_UC1_TXTS_L/TMR_UC1_TXTS_H.	CE_PB27
PTP_SOF_RX2468	Input	Transitions synchronously with respect to the RX Serial Clock.	• Input trigger to capture time stamps for each frame received in one of UCC2/UCC4/UCC6/UCC8 instead of time stamping according to SFD detection. • Captured time stamp value is stored in TMR_UC2_RXTS_L/TMR_UC2_RXTS_H.	CE_PF13
PTP_SOF_TX2468	Input	Transitions synchronously with respect to the TX Serial Clock.	• Input trigger to capture time stamps for each frame transmitted by one of UCC2/UCC4/UCC6/UCC8 instead of time stamping according to SFD detection. • Captured time stamp value is stored in TMR_UC2_TXTS_L/TMR_UC2_TXTS_H.	CE_PF14

4.2 Reset

Figure 4-3 illustrates a detailed PB RESET Unit block diagram. The RESET Unit acts as follows:

- resets the MPC8569E and all periphery onboard components; and,
- provides Power-ON, HRESET, and SRESET signals in compliance with MPC8569E hardware specifications.

Figure 4-3. RESET Unit Block Diagram

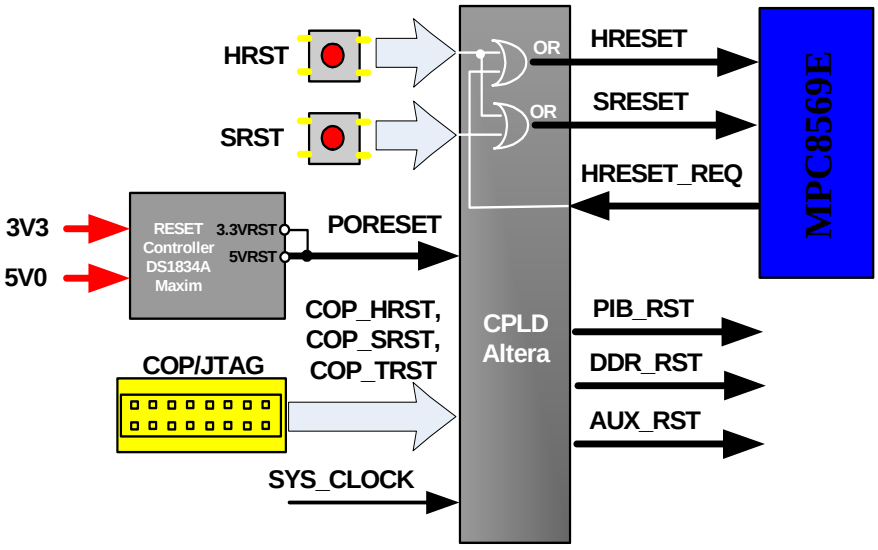
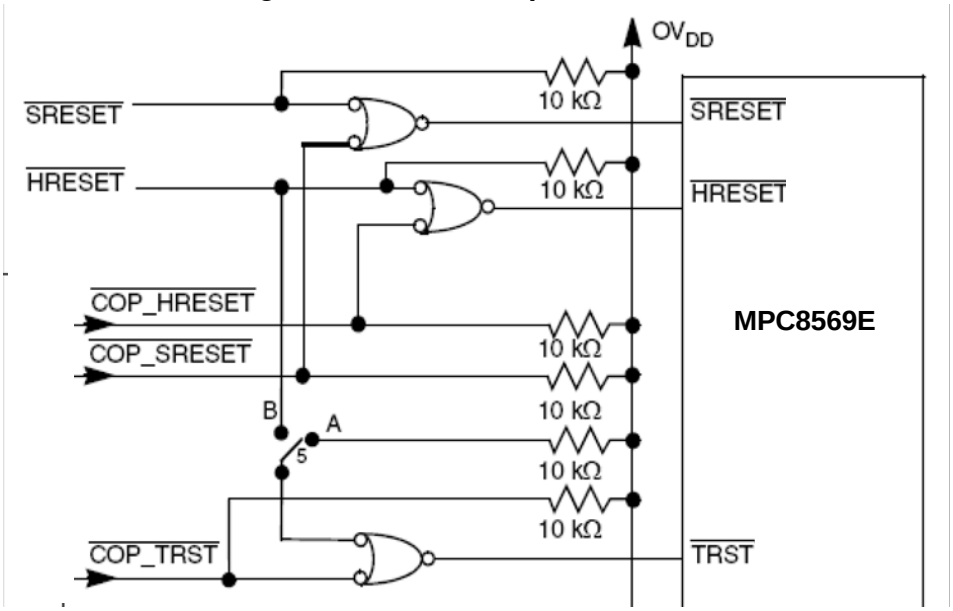


Figure 4-4 illustrates the interconnection between HRESET, SRESET, and COP reset signals.

Figure 4-4. RESET Implementation



HRESET switch is included as a BSDL testing precaution. Set to position A (closed) to avoid asserting TRST during BSDL testing. When not testing BSDL then set the switch to position B.

4.2.1 Power-ON

Power_ON RESET stages:

1. Stabilizes 3.3V and 5V DC input voltages.
2. Dallas/Maxim DS1834A (U87) reset controller drives (low) the $\overline{3.3VRST}$ and $\overline{5VRST}$ output signals for approximately 350ms.
3. PLL locking: system clock runs at 100KHz while the internal counter waits 16,384 clock cycles.

4.2.2 HRESET

HRESET push button provides manual reset control by starting a one-shot circuit (with debounce flip-flop) that sends a pulse to the Altera CPLD-mapped reset controller.

Reset controller output is combined with MPC8569E $\overline{HRESET\_REQ}$ output and routed to MPC8569E $\overline{HRESET}$ input.

Routed input acts in two manners:

- Creates a Power-ON or HRESET push button reset.
- Stops reset when the MPC8569E is ready to operate (auto-cancelling).

4.2.3 SRESET

$\overline{SRESET}$ unit implements a one-shot circuit (with debounce flip-flop) that sends a pulse to MPC8569E $\overline{SRESET}$ input. Tsrst ≥ 10mS is sufficient even if the system clock is as low as 100kHz.

SRESET is asserted at the same time as HRESET. However, SRESET remains asserted for eight system clocks following negation of the HRESET signal.

4.3 PB Control

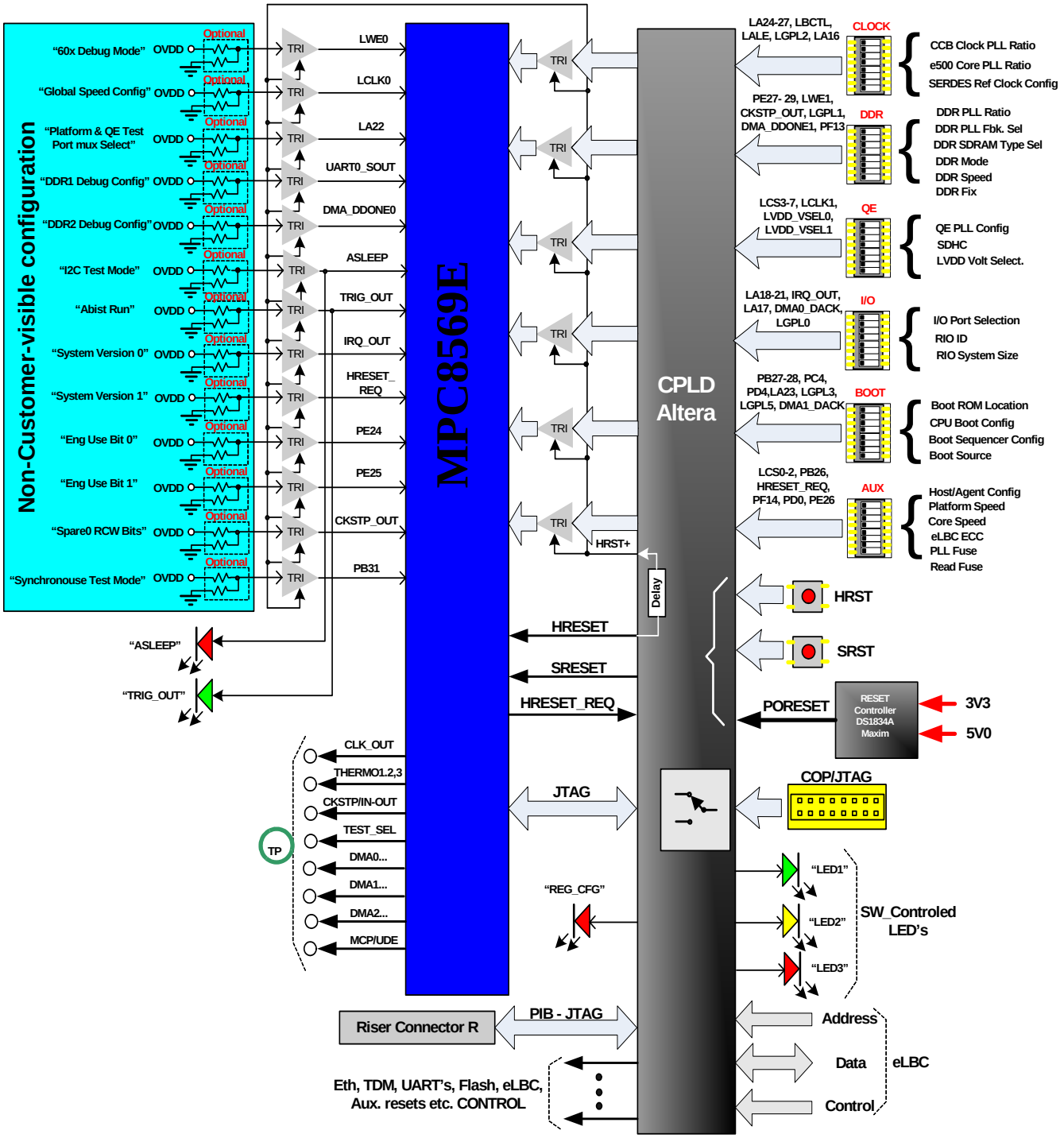
MPC8569E provides numerous configuration options when reset configuration signals are driven during device HRESET.

This PB functionality, as well as various other control functions, are provided with the eLBC-mapped CPLD. The mapping contains a software accessible set of registers (BCSR) and logic networks that actualize required auxiliary functions like HRESET and SRESET generation, etc.

4.3.1 PB Control Block Diagram

Figure 4-5 is a detailed block diagram of the PB control system and debug signals.

Figure 4-5. PB Control Block Diagram



4.3.2 System Control

At Power-ON it is necessary to configure the MPC8569E and define system interface parameters; e.g., SerDes configuration, PLL setting, etc.

At reset the MPC8569E reads the status of the corresponding reset configuration pins.

4.3.3 Reset Configurations

Every MPC8569E reset configuration pin is connected to a corresponding TRI-state buffer output; the latter provides, after a short delay, required settings to the MPC8569E and the basic periphery.

Every signal is set by a corresponding DIP-switch or sampled from a corresponding pre-programmed CPLD register. Alternative MPC8569E pin mode settings are listed in Table 4-1 to Table 4-6.

A number of auxiliary non-customer configuration signals with onboard optional pull-up/down resistors are available for assembly. Table 4-7 and Table 4-8 list alternative pin functions.

4.3.3.1 DIP-Switches

4.3.3.1.1 “CLOCK” DIP-Switches

Table 4-1. “CLOCK” DIP-Switch Block

Main Function	eLBC							
	LA24	LA25	LA26	LA27	LBCTL	LALE	LGPL2	LA16
Reset Config Setting	CCB Clock PLL Ratio				e500 Core PLL Ratios			SERDES Ref Clock Config
	cfg_sys_pll[0]	cfg_sys_pll[1]	cfg_sys_pll[2]	cfg_sys_pll[3]	cfg_core_pll[0]	cfg_core_pll[1]	cfg_core_pll [2]	cfg_srds_refclk

4.3.3.1.2 “DDR” DIP-Switch Block

Table 4-2. “DDR” DIP-Switch Block

Main Function	QE			eLBC	Debug	eLBC	DMA	QE
	PE27	PE28	PE29	LWE1	CKSTP_OUT	LGPL1	DMA_DDONE 1	PF13
Reset Config Setting	DDR Complex Clock PLL Ratio			DDR PLL Feedback Select	DDR DRAM Type	DDR DRAM Mode	DDR Speed	DDR Fix
	cfg_ddr_pll[0]	cfg_ddr_pll[1]	cfg_ddr_pll[2]	cfg_ddr_pll_ fdbk_sel	cfg_dram_type	cfg_dram_ mode	Cfg_ddr_ speed	Cfg_ddr_fix_ dis

4.3.3.1.3 "QE" DIP-Switch Block

Table 4-3. "QE" DIP-Switch Block

Main Function	eLBC					eLBC	Misc.	
	LCS3	LCS4	LCS5	LCS6	LCS7	LCLK1	LVDD VSEL0	LVDD VSEL1
Reset Config Setting	QE Multiplier					SDHC_CD_ Polarity	QUICC Engine Block UCC1-4 Voltage Select	
	cfg_qe_pll[0]	cfg_qe_pll[1]	cfg_qe_pll[2]	cfg_qe_pll[3]	cfg_qe_pll[4]	Cfg_sdhc_cd_ pol_sel	-	-

4.3.3.1.4 "I/O" DIP-Switch Block

Table 4-4. "I/O" DIP-Switch Block

Main Function	eLBC				MPIC	eLBC	DMA	eLBC
	LA18	LA19	LA20	LA21	IRQ_OUT	LA17	DMA0_ DACK	LGPL0
Reset Config Setting	I/O Port Selection				RapidIO Device ID			RapidIO System Size
	cfg_IO_port [0]	cfg_IO_port[1]	cfg_IO_port[2]	cfg_IO_port[3]	cfg_device_ ID5	cfg_device_ ID6	cfg_device_ ID7	cfg_rio_sys_ size

4.3.3.1.5 "BOOT" DIP-Switch Block

Table 4-5. "BOOT" DIP-Switch Block

Main Function	QE				eLBC			Misc.
	PB27	PB28	PC4	PD4	LA23	LGPL3	LGPL5	DMA1_ DACK
Reset Config Setting	Boot ROM Location				CPU Boot Config	Boot Sequencer Configuration		RCW Source
	cfg_rom_loc[0]	cfg_rom_loc[1]	cfg_rom_loc[2]	cfg_rom_loc[3]	cfg_cpu_boot	cpu_boot_seq [0]	cpu_boot_seq [1]	cfg_rcw_ source

4.3.3.1.6 "AUX" DIP-Switch Block

Table 4-6. "AUX" DIP-Switch Block

Main Function	eLBC			QE	Misc.	QE		
	LCS0	LCS1	LCS2	PB26	HRESET_REQ	PF14	PD0	PE26
Reset Config Setting	Host/Agent Configuration			Platform Speed	Core Speed	eLBC POR ECC Enabled	PLL FUSE	READ FUSE
	cfg_host_agt [0]	cfg_host_agt [1]	cfg_host_agt [2]	Cfg_plat_ speed	Cfg_core_ speed	Cfg_lb_por_ ecc_en	Cfg_Pll_fuse_ ovrd_dis	Cfg_fuse_read _en

4.3.3.2 Non-Customer Configuration Signals

4.3.3.2.1 Non-Customer Configuration Signals 1

Table 4-7. Non-Customer Configuration Signals 1

Main Function	eLBC			Misc.	DMA	Misc.		
	LWE0	LCLK0	LA22	UART0_SOUT	DMA_DDONE 0	ASLEEP	TRIG_OUT	nIRQ_OUT
Reset Config Setting[a]	60x Debug Mode	Global Speed Configuration	Platform and QE Test Port MUX Select	DDR1 Debug Config	DDR2 Debug Config	I2C Test Mode	Abist Run	System Ver. Number 0
	Cfg_60x_ debug	Cfg_global_ sfto	Cfg_test_port_ dis	Cfg_DDR1_ Debug	Cfg_DDR2_ Debug	Cfg_I2C_test	Cfg_abist_en	Cfg_svr0

[a] [Optional] Pull-up/down resistors

4.3.3.2.2 Non-Customer Configuration Signals 2

Table 4-8. Non-Customer Configuration Signals 2

Main Function	Misc.	QE		Misc.	QE	
	HRESET_REQ	PE24	PE25	CKSTP_OUT	PB31	PB7
Reset Config Setting[a]	System Ver. Number 1	Eng Use Bit 0	Eng Use Bit 1	Spare0 RCW Bits	Synchronous Test Mode Enable	Global WAITR Enabled (Debug Mode)
	Cfg_svr1	Cfg_eng_use0	Cfg_eng_use1	Cfg_spare	Cfg_slave_ mode_dis	Cfg_Global_ waitr

[a] [Optional] Pull-up/down resistors.

4.4 JTAG COP Connection

MPC8569E JTAG connection capability is enabled via a direct connection to the J13 header connector.

4.4.1 JTAG-COP Header

J13 JTAG header connects between the MPC8569E and an external, compatible JTAG converter such as the CodeWarrior USB TAP; this is the default converter. Table 4-9 shows JTAG dual-in-row header pin-outs.

Table 4-9. JTAG-COP Header J13 Pinout

Pin Number															
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
TDO	NC	TDI	TRST	RUN/ STOP	3.3V	TCK	CHKSTP _IN	TMS	GND	SRST	GND	HRST	HRESET# _OUT	CHKSTP _OUT	GND

4.5 Interrupts

The MPC8569E has seven external interrupts. See Table 4-10 for interrupt connections

Table 4-10. Interrupts

Name	Alternative function	Interrupt source	Note
IRQ0	-	DDR3 EVENT, USB VCC PWR	-
IRQ1	-	GETH1	UCC1
IRQ2	-	GETH2	UCC2
IRQ3	-	GETH3, RTC	UCC3
IRQ4	SRCID3	GETH4, PIB	UCC4
IRQ5	SRCID4	PIB	-
IRQ6	DVAL	PIB	-

4.6 Debugging

Chip debugging is done through the MPC8569E JTAG port. Dedicated MPC8569E pins are connected to specified test points to enable PB testing.

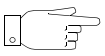
See the TP grouping in Figure 4-5; it is marked by a green circle.

4.7 POSt Module

The POSt module is operated via a serial shift register protocol. Using a defined FA test/visibility mode, six module inputs and one module output are routed to IO pins. This mode is invoked by configuring PPAR register bits to 01.

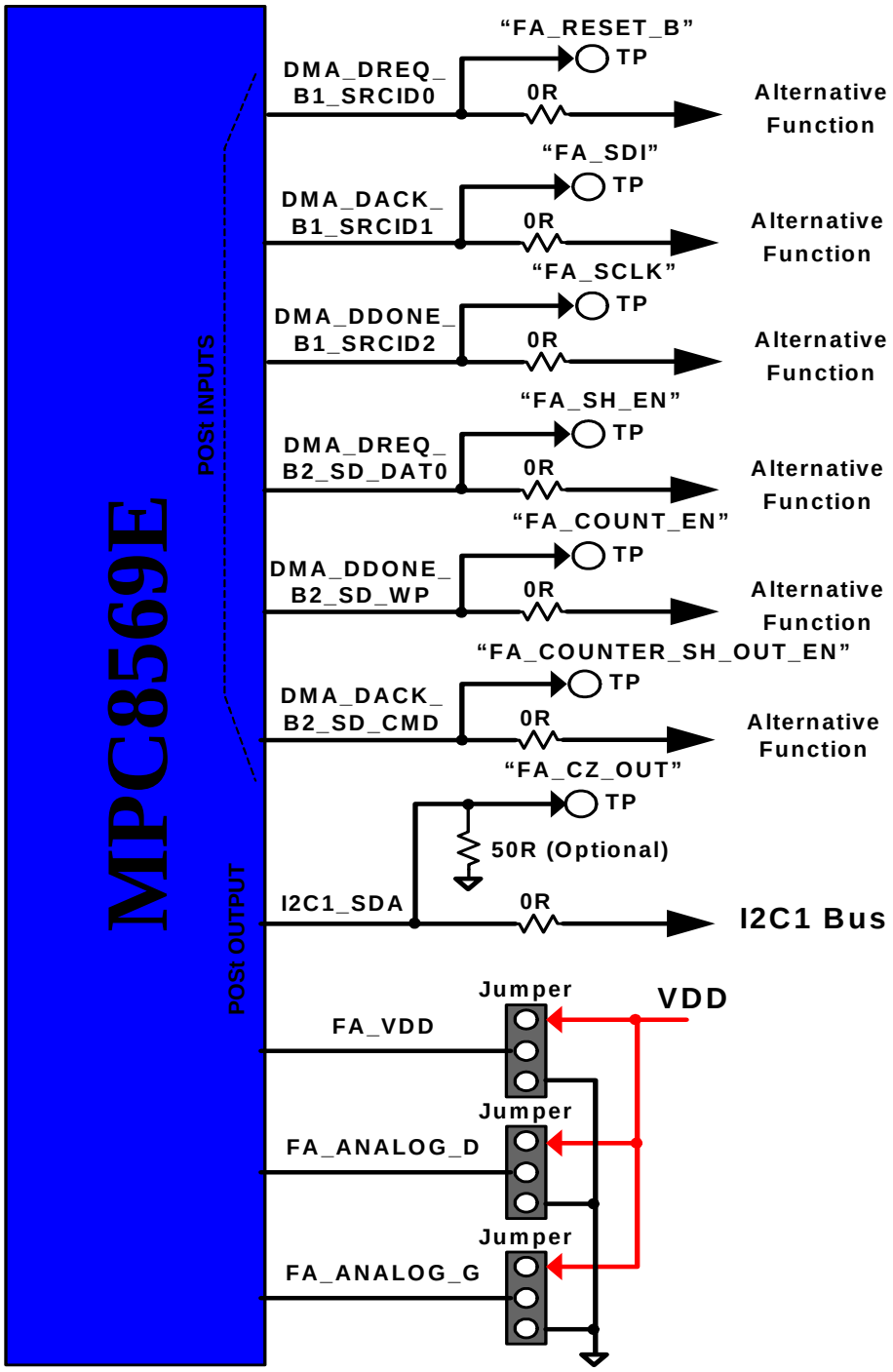
The POSt module is powered by a dedicated supply pin (FA_VDD) and two dedicated analog pins (FA_ANALOG_D and FA_ANALOG_G.).

FA POSt module operations are enabled using dedicated MPC8569E pins connected to a set of PB jumper and test points; see Figure 4-6.



The default customer mode has pins—FA_VDD, FA_ANALOG_D, and FA_ANALOG_G—connected to the GND.

Figure 4-6. POSt Module Interconnections



4.8 IRSense Module

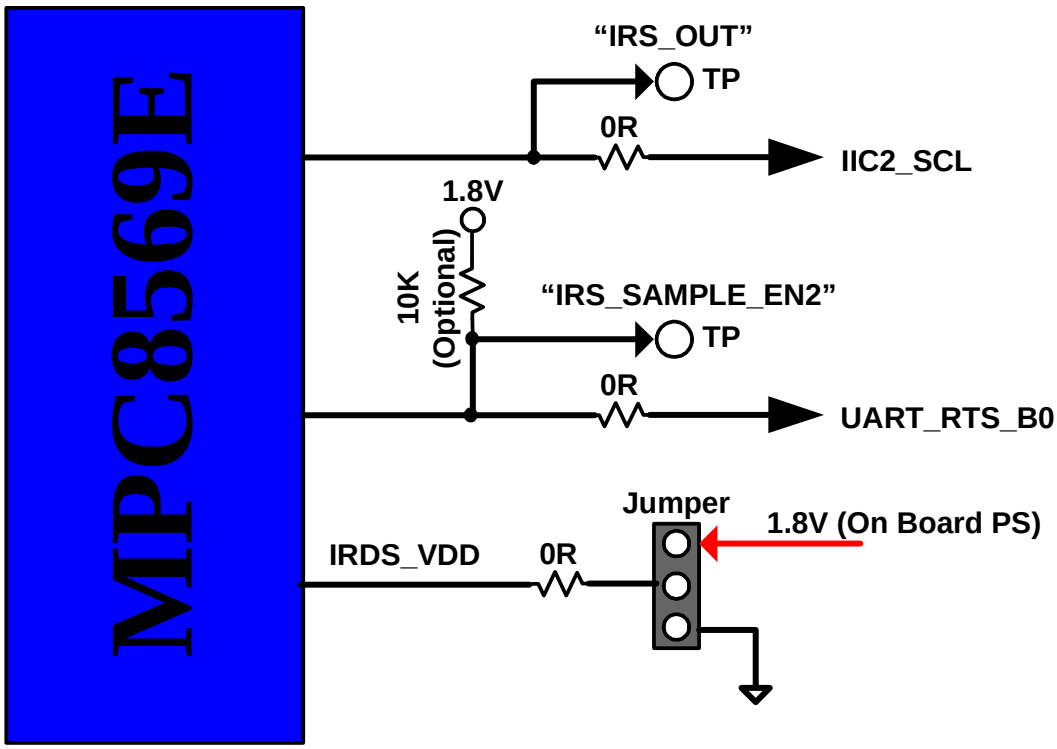
The IRSense module provides a digital indication of internal voltage (IR) drop; it is configured by a programming register (TBD).

The module's digital input/output is routed to IO pins in the defined FA test/visibility mode; the mode is invoked by configuring PPAR register bits to 01.

FA IRSense module operation is enabled using dedicated MPC8569E pins connected to the PB; see Figure 4-7.

Default customer mode: IRDS_VDD pin is connected to the GND.

Figure 4-7. IRSense Module Interconnections



Chapter 5:
Board Control Status Registers (BCSR)

The CPLD U86 incorporates BCSRs that are accessed through the eLBC. The BCSRs use the CS1 region at addresses 0xF8000000-0xF8007FFF. Address lines A[27:23] are decoded for BCSR register selection.

5.1 BCSR Features

BCSRs are characterized by the following features:

- implemented on an Altera CPLD device that provides register and logic functions for some MPC8569E-MDS-PB signals;
- 8-bit wide read/write register module;
- 32-register modules (maximum) control/monitor various MPC8569E MDS PB operations;
- maximum of 18 registers are accessible from the local bus;

5.2 BCSR Functions

BCSRs control/monitor the functions noted in Table 5-1.

Table 5-1. Functions Controlled/Monitored by BCSR

BCSR-controlled Function	Description
BCSRx Status Registers	In the following state: • Board Revision Code (BCSR-REV, BCSR-SUBREV)
Board Clocking Configuration Control	• Onboard signal multiplexers • SerDes clock synthesizer • GETH PHY reference clock source
Configuration Settings	• Processor $\overline{\text{PORESET}}$ • Boot configuration settings
Enable/Disable	• Switch/BCSR boot configuration select on $\overline{\text{HRESET}}$ • Transceiver: Dual RS232 • Transceivers: GETH 1/2/3/4 • Transceiver: USB • SD Card functionality
Hardware Configuration	GETH transceivers (QE HW configurations).
HW Write Protection	FLASH and BRD I^2C EEPROM.
LEDs (3)	Providing SW signaling.
Push Buttons	$\overline{\text{HRESET}}$ and $\overline{\text{SRESET}}$ push buttons with debounce function.

BCSR bit status functions are noted in Table 5-2.

Table 5-2. BCSR Control Register Mnemonics

Bit Status	Description
'1'	High (active) function.
'0'	Low active function.
R	Read-only.
W	Write-only.
R, W	Read and write.

5.3 BCSR Reprogramming

BCSRs are reprogrammable using USB TAP. The following section explains BCSR reprogramming procedure.

5.3.1 USB TAP

Follow the below steps to reprogram the BCSR using the USB TAP.

1. Turn off board power.
2. Insert the interconnection header into the 16-pin header firmware programming socket (U29, "CNTR-ISP").
3. Connect USB TAP to the header.
4. Turn on board power.
5. Launch CCS by following the instructions noted below:

Launch CCS	CCS Commands
Windows Host Machine • launching CCS	• Run the command <CodeWarrior Installation>\ccs\bin\ccs.exe • Add a CCS icon () to the task bar. • • Double-click the icon to open the command window.
Linux Host Machine • launching CCS	• Run the command: <CodeWarrior Installation>/ccs/bin/ccs • Command window automatically opens.

6. Follow the CCS commands noted below to load the program:

CCS Steps	CCS Commands
Initialize USB TAP	Type (from the root directory) the following: • ccs> delete all • ccs> config cc utap
Move to BCSR Directory	Type: • ccs> cd <path> • ccs> ::svf::burn bcsr_top.svf
Program Output	• "0: USB TAP (JTAG) (utap:01001762) Loader software ver. {1.8}" • "Sending code to USB TAP - please wait"

7. Wait until BCSR completes reprogramming.
8. After the status light stops flashing, only then disconnect the USB TAP.

5.4 BCSR Register Tables

5.4.1 BCSR0

Table 3. BCSR0 Register

Bit	Config Signals	Function	Default	Att
[0:3]	CFG_SYS_PLL[0:3]	Establishes clock ratio between SYSCLK and CCB.	SW7[1:4] sampled at HRESET. [1000]	R,W
[4:6]	CFG_CORE_PLL[0:2]	Sets ratio between e500 Core PLL clock and CCB.	SW7[5:7] sampled at HRESET [100]	R,W
[7]	CFG_SRDS_REFCLK	• 0: SerDes expects 125 MHz reference clock frequency. • 1 (Default): SerDes expects 100 MHz reference clock frequency.	SW7[8] sampled at HRESET [1]	R,W

5.4.2 BCSR1

Table 4. BCSR1 Register

Bit	Config Signals	Function	Default	Att
[0:2]	CFG_DDR_CLK_PLL[0:2]	Configure DDR PLL ratio.	SW5[1:3] sampled at HRESET. • DDR2 [100] • DDR3 [110]	R,W
[3]	CFG_DDR_FB_SEL	DDR QE and Platform PLL Feedback Select • 0: gclk-matched/long DDR, QE, and Platform PLLs feedback path. • 1 (Default): local/short DDR PLL feedback path.	SW5[4] sampled at HRESET [1]	R,W

[4]	CFG_DDR_TYPE	DDR Dram Type (DDR2 or DDR3) • 0: DDR3 of 1.5V and low CKE at reset. • 1 (Default): DDR2 of 1.8V and low CKE at reset.	SW5[5] sampled at HRESET. • DDR3 [0] • DDR2 [1]	R,W
[5]	CFG_DDR_MODE	DDR Dram Mode (1x64 or 2x32) • 0: Primary and Secondary DDR is enabled (32-bit width data bus). • 1 (Default): Primary DDR is enabled (64-bit width data bus) but secondary DDR is disabled.	SW5[6] sampled at HRESET [1]	R,W
[6]	CFG_DDR_SPEED	DDR speed configuration input configures internal logic for proper operation of the DDR. • 0: DDR clock frequency < 500MHz. • 1: DDR clock frequency is > or = 500MHz.	SW5[7] sampled at HRESET [0]	R,W
[7]	DDR_FIX	• 1: At reset, DDR disables both MCK and MCKE. • 0: DDR disables MCKE at reset; a few cycles later MCK is disabled.	SW5[8] sampled at HRESET [1]	R,W

5.4.3 BCSR2

Table 5. BCSR2 Register

Bit	Config Signals	Function	Default	Att
[0:4]	CFG_QE_PLL[0:4]	• A multiplier and divisor, applied to SYSCLK input, define the QE clock: – QE Clock=SYSCLK*(CFG QE PLL[0:4]/CFG_QE_CLK)	SW6[1:5] sampled at HRESET [01000]	R,W
[5]	SDHC	SDHC Card Detect Polarity Select • 0: SDHC card-detect polarity is inverted. • 1 (Default): SDHC card-detect polarity isn't inverted.	SW6[6] sampled at HRESET [1]	R,W
[6:7]	CFG_LVDD_VSEL[0:1]	Voltage Select Dedicated Pins • QE UCC1 and UCC3 Voltage Select • QE UCC2 and UCC4 Voltage Select	SW6[6:7] sampled at HRESET [11]	R,W

5.4.4 BCSR3

Table 6. BCSR3 Register

Bit	Config Signals	Function	Default	Att
[0:3]	CFG_PORT_SEL[0:3]	IO Select Configuration for SerDes.	SW8[1:4] sampled at HRESET [0111]	R,W
[4:6]	CFG_RIO_ID[5:7]	RapidIO Device ID [5:7].	SW8[5:7] sampled at HRESET [000]	R,W

Bit	Config Signals	Function	Default	Att
[7]	CFG_RIO_SYS_SIZE	RapidIO System Size • 0: Large system size with a maximum of 65,536 devices. • 1: Small system size with a maximum of 256 devices.	SW8[8] sampled at HRESET [1]	R,W

5.4.5 BCSR4

Table 7. BCSR4 Register

Bit	Config Signals	Function	Default	Att
[0:3]	CFG_ROM_LOC[0:3]	Selects physical location of boot ROM.	SW9[1:4] sampled at HRESET [1101]	R,W
[4]	CFG_BOOT_CPU	Specifies Boot Configuration Mode: • 0: CPU Boot Hold-off Mode; e500 core boots after configuration by an external master. • 1 (Default): e500 core boots without being configured by an external master.	SW9[5] sampled at HRESET [1]	R,W
[5:6]	CFG_BOOT_SEQ[0:1]	Boot Sequencer • Allows Boot Sequencer to load serial ROM (on I^2C1 port) configuration data before the host configures the MPC8569E.	SW9[6:7] sampled at HRESET [11]	R,W
[7]	CFG_SOURCE	Reset Configuration Source bit lets users select RCW source. • 0: RCW is read through I^2C. • 1: RCW is read through IO pin sampling.	SW9[8] sampled at HRESET [1]	R/W

5.4.6 BCSR5

Table 8. BCSR5 Register

Bit	Config Signals	Function	Default	Att
[0:2]	CFG_HOST_AGT[0:2]	MPC8569E configured to act as a host or agent to another interface master (PEX and SRIO).	SW10[1:3] sampled at HRESET [111]	R,W
[3]	CFG_PLAT_SPEED	Platform speed configuration input configures internal logic for proper operation with CCB frequencies. • 0: CCB frequency < 333 MHz • 1: CCB frequency > or = 333 MHz.	SW10[4] sampled at HRESET [1]	R,W
[4]	CFG_CORE_SPEED	Core speed configuration input configures internal logic for proper operation with core clock frequencies. • 0: Core clock frequency < or = to 1000MHz. • 1: Core clock frequency > 1000MHz.	SW10[5] sampled at HRESET [1]	R,W

Bit	Config Signals	Function	Default	Att
[5]	CFG_ELBC_ECC	POR configuration input enables eLBC ECC checking on booted external local bus interface. • 0: eLBC ECC disabled after POR. • 1: eLBC ECC enabled after POR.	SW10[5] sampled at HRESET [0]	R,W
[6]	CFG_FUSE_OVR_DIS	• 0: Fuse PLL override is enabled. • 1: Fuse PLL override is disabled.	SW10[6] sampled at HRESET [1]	R,W
[7]	CFG_FUSE_READ	Fuse Read Enable • 0: Fuse reads are disabled during reset sequence. • 1 (Default): Fuse reads are enabled during reset sequence.	SW10[7] sampled at HRESET [1]	R,W

5.4.7 BCSR6

Table 9. BCSR6 Register description

Bit	Config Signals	Function	Default	Att
[0]	UPC1_EN	• 1: Enable UPC1, ATM, or POS • 0: Disable UPC1 **OR** enable TDM1A, TDM1B, TDM1E, TDM1F, TDM1G, TDM1H, TDM2A, TDM2C, TDM2D, TDM2E, RMII5, RMII7, RMII8, TDM2G, TDM2F, and RMII6	[1]	R,W
[1]	RUPC1POS_EN	• 1: Enable UPC1POS • 0: Disable UPC1POS **OR** enable TDM2A and TDM1B	[1]	R,W
[2]	RUPC1ADDR_EN	• 1: Enable UPC1ADDR, ATM, or POS • 0: Disable UPC1ADDR (Unsupported: SMII8 and SMII6)	[1]	R,W
[3]	RUPC1DEV2	• 1: Enable UPC1DEV2, ATM, or POS • 0: Disable UPC1DEV2 **OR** enable TDM2C and UCC3	[1]	R,W
[4]	SD_CARD_1bit	• 1: Enable SD serial mode **AND** disable I^2C2 • 0: Disable SD serial mode **AND** enable I^2C2	[0]	R,W
[5]	SD_CARD_4bits	• 1: Enable SD Card nibble mode (SD_CARD_1bit should be “1”) **AND** disable DUART0 and I^2C2 bus • 0: Enable DUART0 **AND** disable SD Card nibble mode	[0]	R,W
[6]	TDM2G	• UPC1_EN = 0(BCSR6[7], disable) • If bit =1, TDM2G is enabled • RMII7(BCSR6[7] should be = 0	[1]	R,W
[7]	RMII7	• UPC1_EN = 0((BCSR6[7], disable) • If bit =1, RMII7 is enabled • TDM2G(BCSR6[6] should be = 0)	[1]	R,W

5.4.8 BCSR7

Table 10. BCSR7 Register description

Bit	Config Signals	Function	Default	Att
[0]	UCC1_GETH	• 1: Enable UCC1_GETH, RGMII, or RTBI • 0: Disable UCC1_GETH **OR** enable UCC1_RMII (RMII1) on PIB	[1]	R,W
[1]	UCC1_RGMII	• 1: Enable RGMII • 0: Disable RTBI **AND** enable RMII on PIB	[1]	R,W
[2]	UCC1_RTBI	• 1: Enable RTBI • 0: Disable RGMII **AND** enable RMII on PIB	[0]	R,W
[3]	G1DIS_125	• 1: Disable PHY1 clock_out 125MHz • 0: Enable	[0]	R,W
[4]	G1ENA_XC	• 1: Enable • 0: Disable	[0]	R,W
[5]	UCC1/UCC2 GETHRST	• 1: Normal operation • 0: Reset (nMVRST) Marvel UCC1 and UCC2	[1]	R,W
[6]	BRDWP	• BRD (EEPROM I^2C Memory): write protected for I^2C Flash • 0: Not protected	[1]	R,W
[7]	BOOTWP	• 1: Not protected. • Boot write protected	[0]	R,W

5.4.9 BCSR8

Table 11. BCSR8 Register

Bit	Config Signals	Function	Default	Att
[0]	UCC2_GETH	• 1: Enable UCC2_GETH, RGMII, or RTBI • 0: Disable UCC2_GETH **OR** enable UCC2_RMII (RMII2) on PIB	[1]	R,W
[1]	UCC2_RGMII	• 1: Enable RGMII • 0: Disable RTBI **AND** enable RMII on PIB	[1]	R,W
[2]	UCC2_RTBI	• 1: Enable RTBI • 0: Disable RGMII **AND** enable RMII on PIB	[0]	R,W
[3]	G2DIS_125	• 1: Disable PHY2 clock_out 125MHz • 0: Enable PHY2 clock_out 125MHz	[0]	R,W
[4]	G2ENA_XC	• 1: Enable • 0: Disable	[0]	R,W

Bit	Config Signals	Function	Default	Att
[5]	CS_NOR	• 1: Boot from NAND_FLASH • 0: Boot from NOR_FLASH	[0]	R,W
[6]	UEM Marvell PHY RESET	• 1: RESET UEM3 (UCC3) and UEM4 (UCC4) • 0: Normal operation	[0]	R,W
[7]	DDRDRV_SEL	• 1: MEMC1,2: MDIC0,1=36.5OHm • 0: MEMC1,2: MDIC0,1=18OHm	[1]	R,W

5.4.10 BCSR9

Table 12. BCSR9 Register

Bit	Config Signals	Function	Default	Att
[0]	UCC3_GETH	• 1: Enable UCC3_GETH – Use UEM module on PB for RGMII or RTBI. • 0: Disable UCC3_GETH **OR** enable (depending upon UCC3_RMII bit) UCC3_RMII (RMII3) on PIB or TDM1C	[1]	R,W
[1]	UCC3_RGMII	• 1: Enable RGMII on UEM • 0: Disable RTBI on UEM **AND** enable RMII3 on PIB	[1]	R,W
[2]	UCC3_RTBI	• 1: Enable RTBI on UEM • 0: Disable RGMII on UEM **AND** enable RMII3 on PIB	[0]	R,W
[3]	UCC3_RMII	• If UCC3_GETH = 0 – then bit = 1 enables UCC3_RMII on PIB – then bit =0 enables TDM1C and UPC1_DEV2 • If UCC3_GETH = 1 – then bit has no effect	[0]	R,W
[4]	RMII3__nSMII3	• 1: Enable RMII on PB (UEM) • 0: Enable SMII on PB (UEM) UCC6 (SMII unsupported)	[1]	R,W
[5]	R_SMII3_nRMII3	• 1: Enable SMII on PB (UEM) UCC6 (SMII unsupported) • 0: Enable RMII on PB (UEM)	[0]	R,W
[6]	RESERVED	RESERVED	[1]	R,W
[7]	nMVPHY_MICPHY3	Select UEM-assembled Marvell PHY or Micrel PHY. • 1: Micrel • 0: Marvel	[0]	R,W

5.4.11 BCSR10

Table 13. BCSR10 Register

Bit	Config Signals	Function	Default	Att
[0]	UCC4_GETH	• 1: Enable UCC4_GETH Use UEM module on PB for RGMII or RTBI. • 0: Disable UCC4_GETH **OR** enable UCC4_RMII (RMII4) on PIB or TDM1C	[1]	R,W
[1]	UCC4_RGMII	• 1: Enable RGMII on UEM • 0: Disable RTBI on UEM **AND** enable RMII3 on PIB	[1]	R,W
[2]	UCC4_RTBI	• 1: Enable RTBI on UEM • 0: Disable RGMII on UEM **AND** enable RMII3 on PIB	[0]	R,W
[3]	RMII4__nSMII4	• 1: Enable RMII on PB (UEM) • 0: Enable SMII on PB (UEM) UCC8 (SMII unsupported)	[1]	R,W
[4]	R_SMII4_nRMII4	• 0: Enable RMII on PB (UEM) • 1: Enable SMII on PB (UEM) UCC8 (SMII unsupported)	[0]	R,W
[5]	nMVPHY_MICPHY4	Select UEM assembled Marvell PHY or Micrel PHY.	[0]	R,W
[6]	RnMICRST	• 0: Micrel PHY Reset on both UCC3- & UCC4-connected UEMs • 1: Normal operation	[0]	R,W
[7]	RMV_SEL_FREQ_34	• 1: Marvell PHY, UCC3 & UCC4 have 25MHz input on UEM • 0: Marvell PHY, UCC3 & UCC4 have 125MHz input on UEM	[0]	R,W

5.4.12 BCSR11

Table 14. BCSR11 Register

<table>
<tr><th>Bit</th><th>Config Signals</th><th>Function</th><th>Default</th><th>Att</th></tr>
<tr><td>[0]</td><td>REGISTER_CONFIG</td><td>• 0: Board configured through DIP-switches
• 1: Board configured through BCSR registers</td><td>[0]</td><td>R,W</td></tr>
<tr><td>[1]</td><td>LED1</td><td>1: LED ON</td><td>[0]</td><td>R,W</td></tr>
<tr><td>[2]</td><td>LED2</td><td>1: LED ON</td><td>[0]</td><td>R,W</td></tr>
<tr><td>[3]</td><td>LED3</td><td>1: LED ON</td><td>[0]</td><td>R,W</td></tr>
<tr><td>[4]</td><td>R_SLEW0</td><td rowspan="2">Select slew rate for GETH input clock.
<table><tr><th colspan="2">Setting</th><th>Slew Rate</th></tr><tr><th>SLEW0</th><th>SLEW1</th><th>(V/ns)</th></tr><tr><td>0</td><td>0</td><td>4</td></tr><tr><td>1</td><td>0</td><td>3</td></tr><tr><td>0</td><td>1</td><td>2</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table></td><td>[0]</td><td>R,W</td></tr>
<tr><td>[5]</td><td>R_SLEW</td><td>[1]</td><td>R,W</td></tr>
<tr><td>[6]</td><td>SSC0</td><td rowspan="2">Select SerDes clock synthesizer spread spectrum mode.
<table><tr><th>SSC0</th><th>SSC1</th><th>SPREAD%</th></tr><tr><td>0 (ON)</td><td>0 (ON)</td><td>CENTER +/- 0.25</td></tr><tr><td>1 (OFF)</td><td>0 (ON)</td><td>DOWN -0.5</td></tr><tr><td>0 (ON)</td><td>1 (OFF)</td><td>DOWN -0.75</td></tr><tr><td>1 (OFF)</td><td>1 (OFF)</td><td>NO SPREAD</td></tr></table></td><td>[1]</td><td>R,W</td></tr>
<tr><td>[7]</td><td>SSC1</td><td>[1]</td><td>R,W</td></tr>
</table>

5.4.13 BCSR12

Table 15. BCSR12 Register

Bit	Config Signals	Function	Default	Att
[0]	PCIE_CLKDIS	• 1: Enable PEX clock • 0: Disable PEX clock	[1]	R,W
[1]	TRIGIN	For internal use only (0)	[Z]	R,W
[2]	RMII6	• 1: Enable RMII6 (on PIB) and TDM2F[a] • 0: Disable RMII6 **AND** enable ATM or POS	[0]	R,W
[3]	RMII8	• 1: Enable RMII8 (on PIB) • 0: Disable RMII8 **AND** enable TDM1H	[0]	R,W
[4]	TDM2D_2F_DIS	• 1: For RMII6 on PIB • 0: For UPC1 or TDM2D or TDM2F	[0]	R,W
[5]	RGETH_CLKSEL	• 1: UEM ref clk = 125MHz • 0: UEM ref clk = 50MHz	[1]	R,W
[6]	RESET_PIB	• 1: RESET RMII PHY, TDM framer, and/ or ATM PHY • 0: Normal operation for RMII PHY, TDM framer, and/ or ATM PHY	[0]	R,W
[7]	ISOLATE_GPIO	• 1: For RMII6 and RMII7 operation • 0: For UPC1 operation	[0]	R,W

[a] I^2C PCA9555 address 26H should drive output register 1[0] to 1.

5.4.14 BCSR13

Table 16. BCSR13 Register

Bit	Config Signals	Function	Default	Att
[0:7]	R_PS[0:7]	Internal Use Only	[1:1]	R,W

5.4.15 BCSR14

Table 17. BCSR14 Register

Bit	Config Signals	Function	Default	Att
[0:4]	R_PS[8:12]	Internal Use Only	[11111]	R,W
[5]	TDM1G_EN	• 1: TDM1G_EN enabled • 0: TDM1G_EN disabled	[0]	R,W
[6]	PRESENCE 3	UEM inserted into J15 • 1: Present • 0: Not present	[X]	R
[7]	PRESENCE 4	UEM inserted into J5 • 1: Present • 0: Not present	[X]	R

5.4.16 BCSR15

Table 18. BCSR15 Register

Bit	Config Signals	Function	Default	Att
[0]	G3ENA_XC	• 1: Enable • 0: Disable	[0]	R,W
[1]	G4ENA_XC	• 1: Enable • 0: Disable	[0]	R,W
[2]	G3DIS_125	• 1: Disable PHY3 clock_out 125MHz • 0: Enable PHY3 clock_out 125MHz	[0]	R,W
[3]	G4DIS_125	• 1: Disable PHY4 clock_out 125Mhx • 0: Enable	[0]	R,W
[4]	SMII6 DIS	• 1: Disable SMII6 **AND** enable RMII6, TDM1C, UPC1 Dev2, and UCC3 • 0: Enable SMII6 and TDM2D (SMII unsupported)	[1]	R,W
[5]	SMII8 DIS	• 1: Enable UCC8 RMII on PIB and TDM1H **AND** disable SMII8. • 0: Enable SMII8 (SMII unsupported)	[1]	R,W
[6]	TDM1F	• 1: Enable TDM1F • 0: Disable TDM1F	[1]	R,W
[7]	RUART1_nQEUART	• 1: Enable QE_UART • 0: Enable UART1, TDM1D, and TDM2B	[0]	R,W

5.4.17 BCSR16

Table 19. BCSR16 Register

Bit	Config Signals	Function	Default	Att
[0]	PORESET	PWR_ON Reset/HRESET • 0: Active	[1]	R,W
[1]	TSEC0MST	Reserved	[1]	R,W
[2]	TSEC1MST	Reserved	[1]	R,W
[3]	TSEC2MST	Reserved	[1]	R,W
[4]	TSEC3MST	Reserved	[1]	R,W
[5]	TSEC4MST	Reserved	[1]	R,W
[6]	TDM1C_DEV2	• 1: Enable UPC1 Device2 • 0: Disable UPC1 Device 2 **OR** enable RMII3 on PIB,TDM1C and TDM2C • If bit = 0 then RMII3 is enabled • Dev2- RxEN_B[2] • TDM2c-TSYNC • TDM1c	[0]	R,W
[7]	RESERVED	-	[0]	R,W

5.4.18 BCSR17

Table 20. BCSR17 Register

Bit	Config Signals	Function	Default	Att
[0]	RnUSBEN	• 1: Disable USB **AND** enable TDM1B • 0: Enable USB	[1]	R,W
[1]	RnUSBLOWSPD	• 1: USB full-speed (12Mb/s) • 0: USB low-speed (1.5Mb/s)	[0]	R,W
[2]	RnUSBVCC	• 1: USB acts as Device – USB powered from an external host – Enables RMII6 and TDM1G • 0: USB acts as Host – USB supplies power to external device	[1]	R,W
[3]	RUSB_MODE	USB Mode • 0: Host • 1: Device	[0]	R,W

Bit	Config Signals	Function	Default	Att
[4]	RPRESENCE_F	UEM inserted into J7 • 1: Present • 0: Not present	[x]	R
[5]	RPRESENCE_E	UEM inserted into J16 • 1: Present • 0: Not present	[x]	R
[6]	RFLASH_RDY	• 1: Ready • 0: Busy	[x]	R
[7]	FLASH_nWP	• 0: FLASH Write Protect • 1: FLASH normal operation	[0]	R,W

5.4.19 BCSR18

Table 21. BCSR18 Register

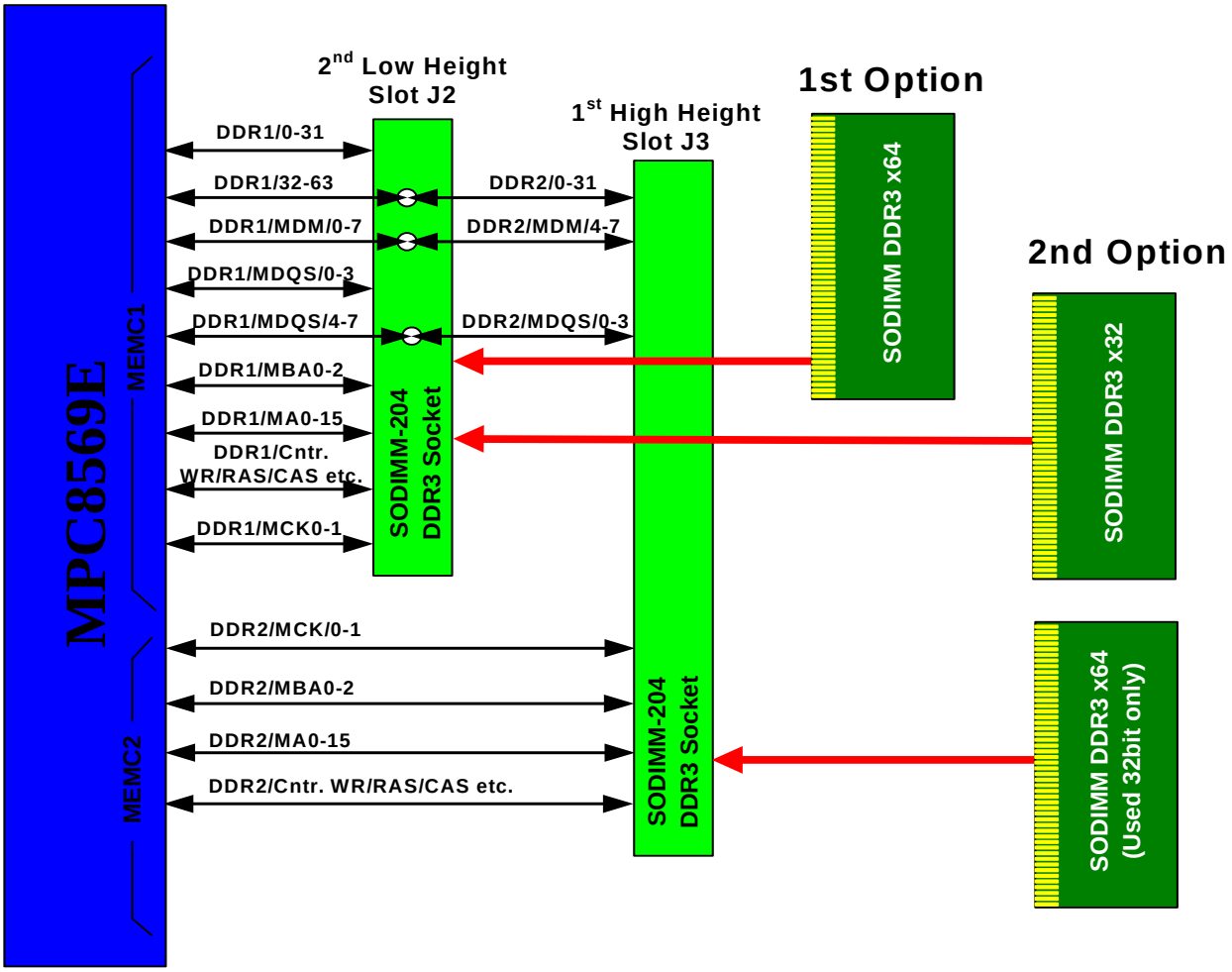
Bit	Config Signals	Function	Value	Att
[0:3]	REV	• BCSR revision • Four bit revision coding	current version	R,W
[4:7]	SUBREV	• BCSR SUB revision • Four bit revision coding	sub version	R,W

Chapter 6: Interfaces

6.1 DDR SDRAM Interface

Figure 6-1 is a detailed block diagram of the DDR SDRAM interface.

Figure 6-1. DDR Interface



6.1.1 DDR Interface Overview

The DDR interface is characterized by the following characteristics:

Table 6-1. DDR Interface

DDR3 Interface	Description
Features	• Ready-for-operation. • 204-pin standard SODIMM sockets (2). • Supports a maximum of two unbuffered DDR3 SODIMM modules.
Interface	• Ensures SPD functioning of DDR SODIMMs. • Enables correct DDR SODIMM operations. • Maximum clock rate of 400 MHz (800 Mbits for DDR3/2). • DDR HSSI-recommended layout guarantees performance.
Configuring MPC8569E	DDR Interface Options: • [Default] DDR3 x64 SODIMM: inserted into low-height J2 slot • DDR3 x32 SODIMM (2): inserted into high- and low-height slots respectively

Figure 6-2 lists pin configurations for the 204-pin DDR3 SODIMM socket.

Table 6-2. DDR3 SODIMM (204-pin) Pin Configurations

204-Pin DDR3 SODIMM Front								204-Pin DDR3 SODIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREFDQ	53	DQ19	105	VDD	157	DQ42	2	VSS	54	VSS	106	VDD	158	DQ46
3	VSS	55	VSS	107	A10	159	DQ43	4	DQ4	56	DQ28	108	BA1	160	DQ47
5	DQ0	57	DQ24	109	BA0	161	VSS	6	DQ5	58	DQ29	110	RAS#	162	VSS
7	DQ1	59	DQ25	111	VDD	163	DQ48	8	VSS	60	VSS	112	VDD	164	DQ52
9	VSS	61	VSS	113	WE#	165	DQ49	10	DQS0#	62	DQ3#	114	S0#	166	DQ53
11	DM0	63	DM3	115	CAS#	167	VSS	12	DQS0	64	DQ3	116	ODT0	168	VSS
13	VSS	65	VSS	117	VDD	169	DQS6#	14	VSS	66	VSS	118	VDD	170	DM6
15	DQ2	67	DQ26	119	A13	171	DQS6	16	DQ6	68	DQ30	120	NC	172	VSS
17	DQ3	69	DQ27	121	NC	173	VSS	18	DQ7	70	DQ31	122	NC	174	DQ54
19	VSS	71	VSS	123	VDD	175	DQ50	20	VSS	72	VSS	124	VDD	176	DQ55
21	DQ8	73	CKE0	125	NC	177	DQ51	22	DQ12	74	NC	126	VREFCA	178	VSS
23	DQ9	75	VDD	127	VSS	179	VSS	24	DQ13	76	VDD	128	VSS	180	DQ60
25	VSS	77	NC	129	DQ32	181	DQ56	26	VSS	78	NC	130	DQ36	182	DQ61
27	DQS1#	79	BA2	131	DQ33	183	DQ57	28	DM1	80[1]	NF/A14	132	DQ37	184	VSS
29	DQS1	81	VDD	133	VSS	185	VSS	30	RESET#	82	VDD	134	VSS	186	DQS7#
31	VSS	83	A12	135	DQS4#	187	DM7	32	VSS	84	A11	136	DM4	188	DQS7
33	DQ10	85	A9	137	DQS4	189	VSS	34	DQ14	86	A7	138	VSS	190	VSS
35	DQ11	87	VDD	139	VSS	191	DQ58	36	DQ15	88	VDD	140	DQ38	192	DQ62
37	VSS	89	A8	141	DQ34	193	DQ59	38	VSS	90	A6	142	DQ39	194	DQ63
39	DQ16	91	A5	143	DQ35	195	VSS	40	DQ20	92	A4	144	VSS	196	VSS
41	DQ17	93	VDD	145	VSS	197	SA0	42	DQ21	94	VDD	146	DQ44	198	EVENT#
43	VSS	95	A3	147	DQ40	199	VDDSPD	44	VSS	96	A2	148	DQ45	200	SDA
45	DQS2#	97	A1	149	DQ41	201	SA1	46	DM2	98	A0	150	VSS	202	SCL
47	DQS2	99	VDD	151	VSS	203	VTT	48	VSS	100	VDD	152	DQS5#	204	VTT
49	VSS	101	CK0	153	DM5			50	DQ22	102	CK1	154	DQS5		
51	DQ18	103	CK0#	155	VSS			52	DQ23	104	CK1#	156	VSS		

Notes: 1. Pin 80 is NF for 1GB and A14 for 2GB.

6.1.2 DDR Power Sources

VDD, VREF, and VTT voltages power the MPC8569E and SODIMM modules from a separate power supply. See Section 3.2, “PB Power Supply Structure”. The SPD Serial I^2C EEPROM is mounted on each DDR SODIMM and powered from the onboard 3.3V power source.

Voltage values are automatically set according to the SODIMM module: DDR3 @ 1.5V. A termination voltage is also provided.

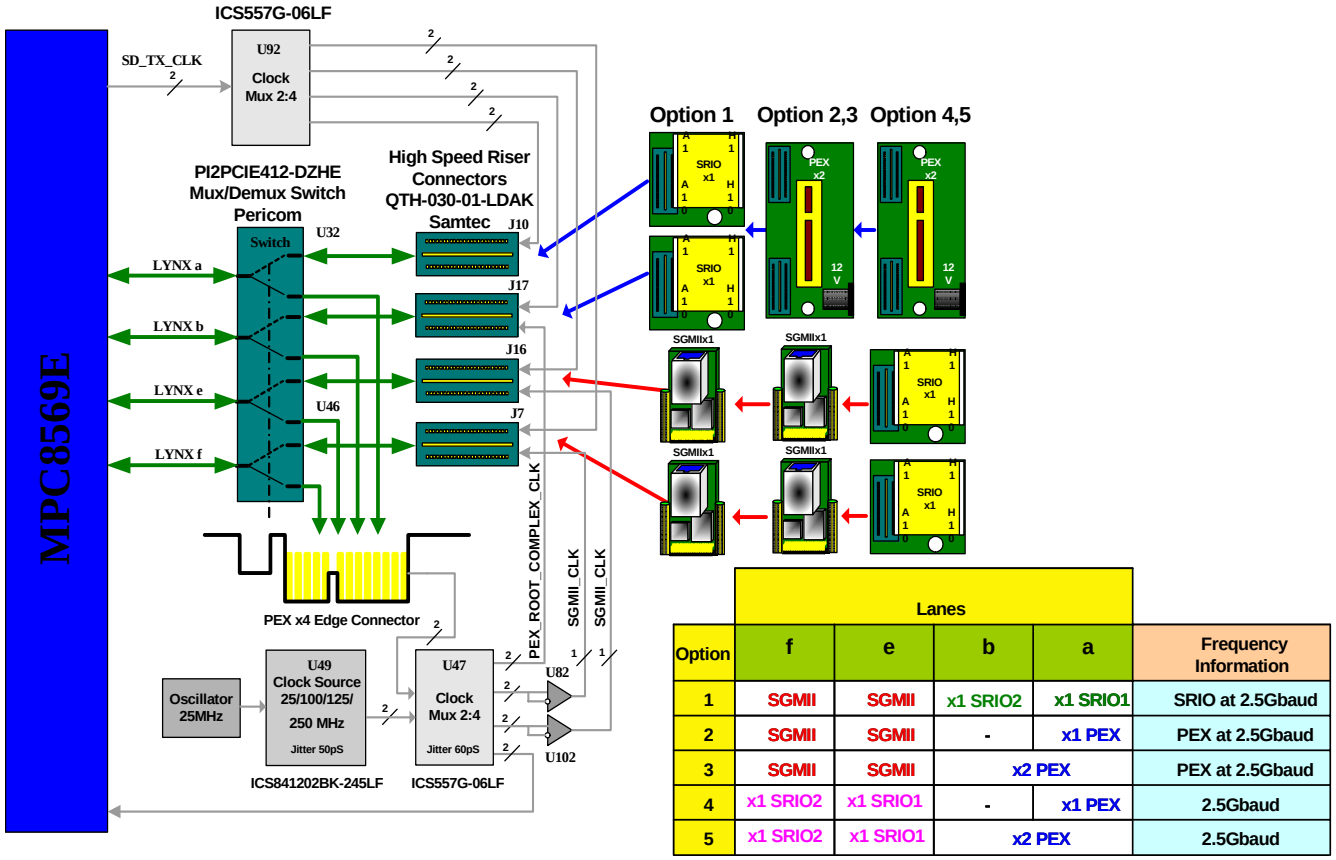
6.1.3 SPD Function

Implement SPD by connecting SODIMM I^2C signals to the MPC8569E’s I^2C1 bus.

6.2 SerDes Interface

Figure 6-2 is a detailed SerDes interface block diagram.

Figure 6-2. SerDes Interface Block Diagram



Option	Lanes f	Lanes e	Lanes b	Lanes a	Frequency Information
1	SGMII	SGMII	x1 SRIO2	x1 SRIO1	SRIO at 2.5Gbaud
2	SGMII	SGMII	-	x1 PEX	PEX at 2.5Gbaud
3	SGMII	SGMII	x2 PEX		PEX at 2.5Gbaud
4	x1 SRIO2	x1 SRIO1	-	x1 PEX	2.5Gbaud
5	x1 SRIO2	x1 SRIO1	x2 PEX		2.5Gbaud

6.2.1 SerDes Clocking

The PB shown in Figure 6-2 provides reference clocks to the MPC8569E SerDes module and peripheral devices.

Table 6-3. SerDes Clocking Solutions

Solution	Description
IDT Clock Source (ICS841202BK-245LF) IDT Clock MUX (ICS557G-06LF)	**Two IDT solutions together provide the following:** • 25/100/125/250MHz reference clocks; • PEX-standard spread spectrum; • total cycle-to-cycle jitter of less than or equal to 110pS; and, • use of external PEX RC reference clocks when onboard MPC8569E serves as a PEX EP. **IDT Clock MUX ICS557G-06LF** • When used, each high-speed connector defined for the SRIO interface receives a separate SD_TX_CLK signal from the MPC8569E SerDes module.
IDT High-Speed Differential Line Driver (ICS83021AMILF)	• Provides SGMII-mode UEM modules with a corresponding reference clock. • Required as UEM-mounted Marvell GETH PHY requires a LVTTL single-ended reference clock.

6.2.2 SerDes Power

MPC8569E SerDes module power (AVDD_SRDS, SCORE_VDD, and XVDD) is derived from a VDD core voltage source and supplied via recommended low-pass filters.

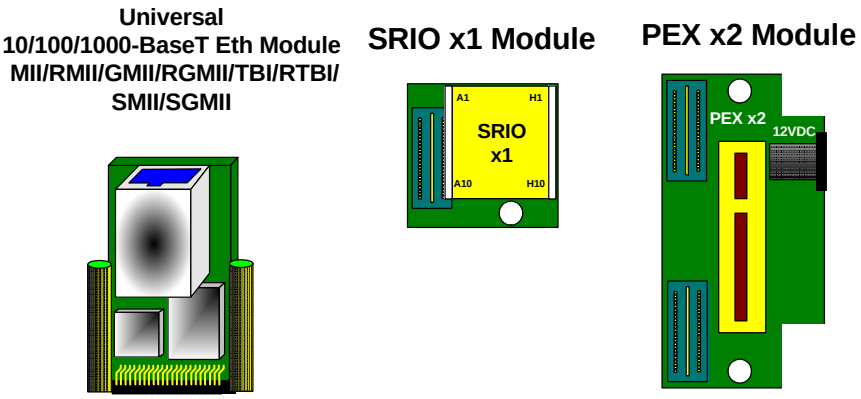
6.2.3 SerDes Interface Overview

The SerDes interface is implemented as four independent, unidirectional, SerDes lines providing three HSSI|—SRIO, PEX and SGMII.

Each SerDes line connects to a predefined, high-speed, onboard connector via a MUX switch. If MPC8569E acts as a PEX EP then the MUX switch redirects the SerDes lines to the PEX edge-connector (not populated).

Special expansion modules are used to create standard interfaces. All modules illustrated in Figure 6-3, aside from the UEM, act as an electrical interconnection between onboard high-speed connectors and standard SRIO header and PEX x2 RC slots.

Figure 6-3. Expansion Modules



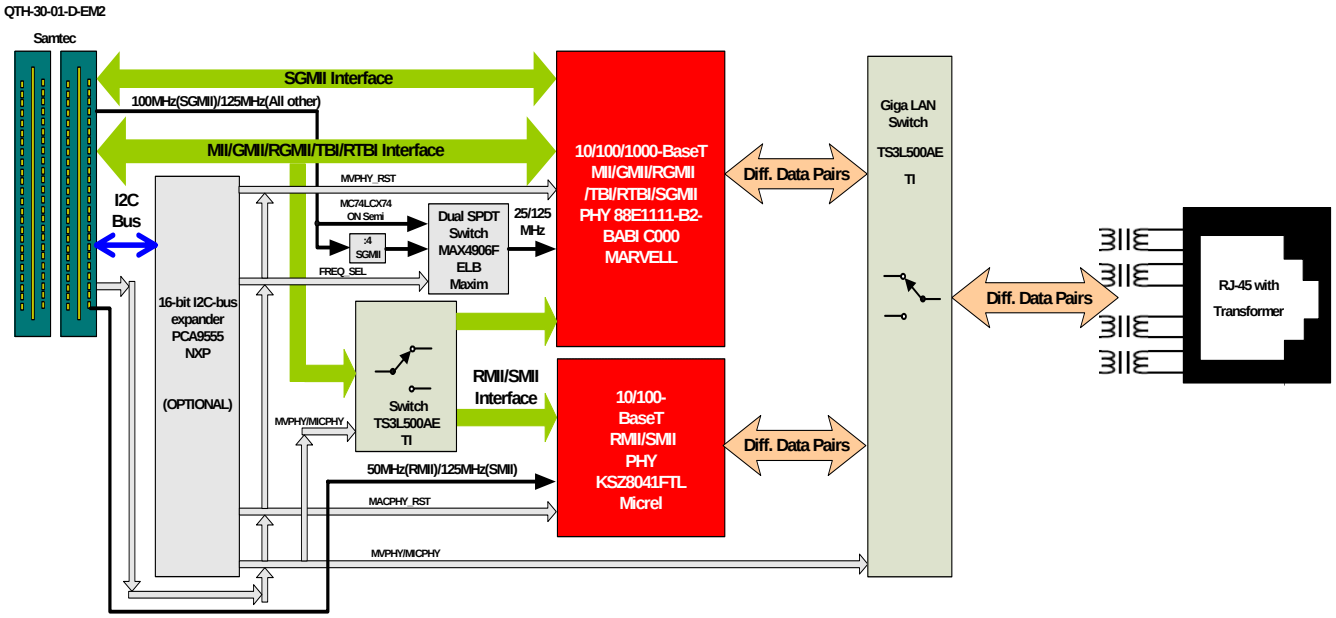
6.2.4 UEM Expansion Module

The UEM acts as a piggyback board and, when mounted on the UEM, its features include the following:

- PHY supporting R/GMII, R/TBI, MII, and SGMII modes.
- PHY supporting RMII and SMII modes.
- Magnetics.
- RJ45 connector.
- Auxiliary components that provide MPC8569E functionality: MAC with 10/100/1000-BaseT MII/RMII/GMII/RGMII/TBI/RTBI/SMII/SGMII interfaces.

Figure 6-4 is a detailed UEM block-diagram.

Figure 6-4. UEM Block Diagram



6.2.5 SRIO Expansion Modules

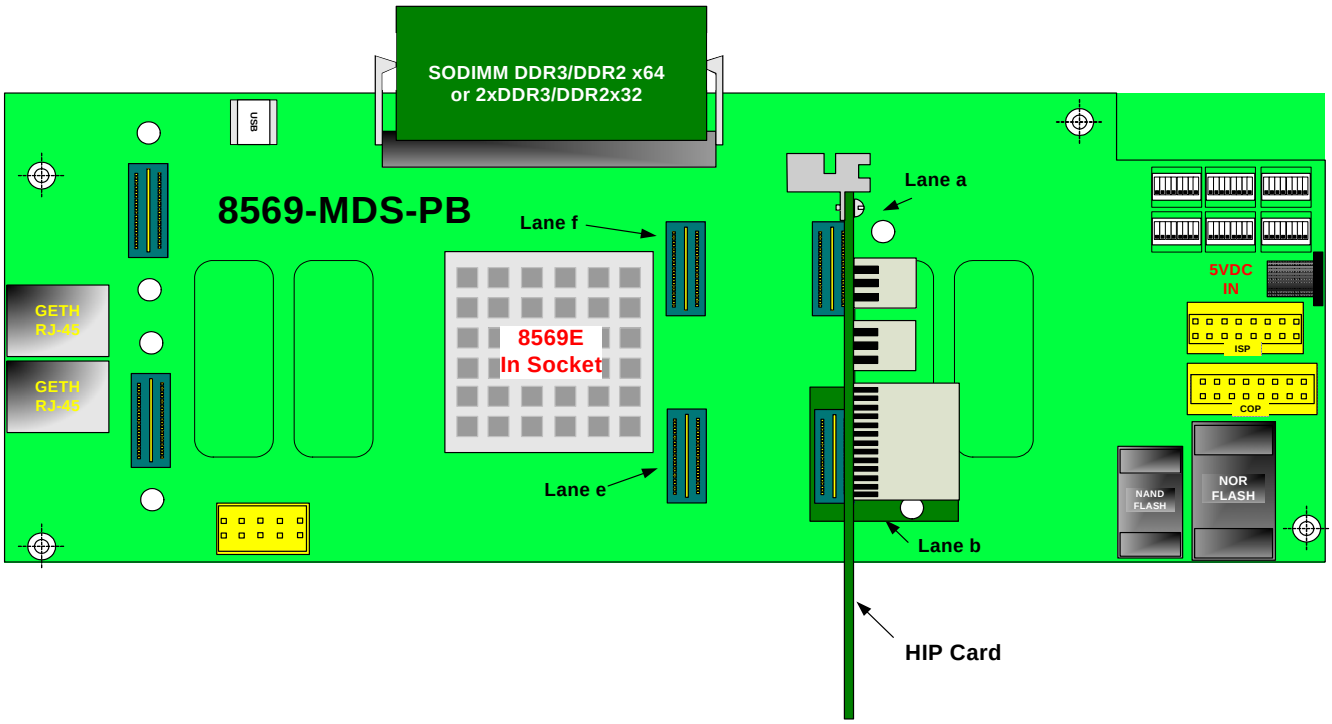
SRIO connectors are placed on SRIO x1 expansion modules to enable HIP card or cable insertions. Figure 6-5 illustrates a HIP card connection mounted on the PB SRIO x1 module.

SRIO connector pin assignments are defined in Table 6-4.

Table 6-4. RapidIO Connector Assignments

Col	A	B	BG	C	D	DG	E	F	FG	G	H	HG
1	TX0	$\overline{\text{TX0}}$	GND	Unused	unused	GND	Unused	unused	GND			GND
2	TX1	$\overline{\text{TX1}}$										
3	TX2	$\overline{\text{TX2}}$										
4	TX3	$\overline{\text{TX3}}$										
5	TCLK0	$\overline{\text{TCLK0}}$										
6												
7										RX3	RX3	
8										RX2	RX2	
9										RX1	RX1	
10										RX0	RX0	

Figure 6-5. HIP Card: Mechanical Scenario



6.2.6 PEX Expansion Modules

PEX connectors are placed on PEX x2 expansion module to interconnect with a standard PEX Add-in card. Figure 6-6 shows a PEX Add-in card connection scenario.

Figure 6-6. PEX Add-in Card: Mechanical Scenario

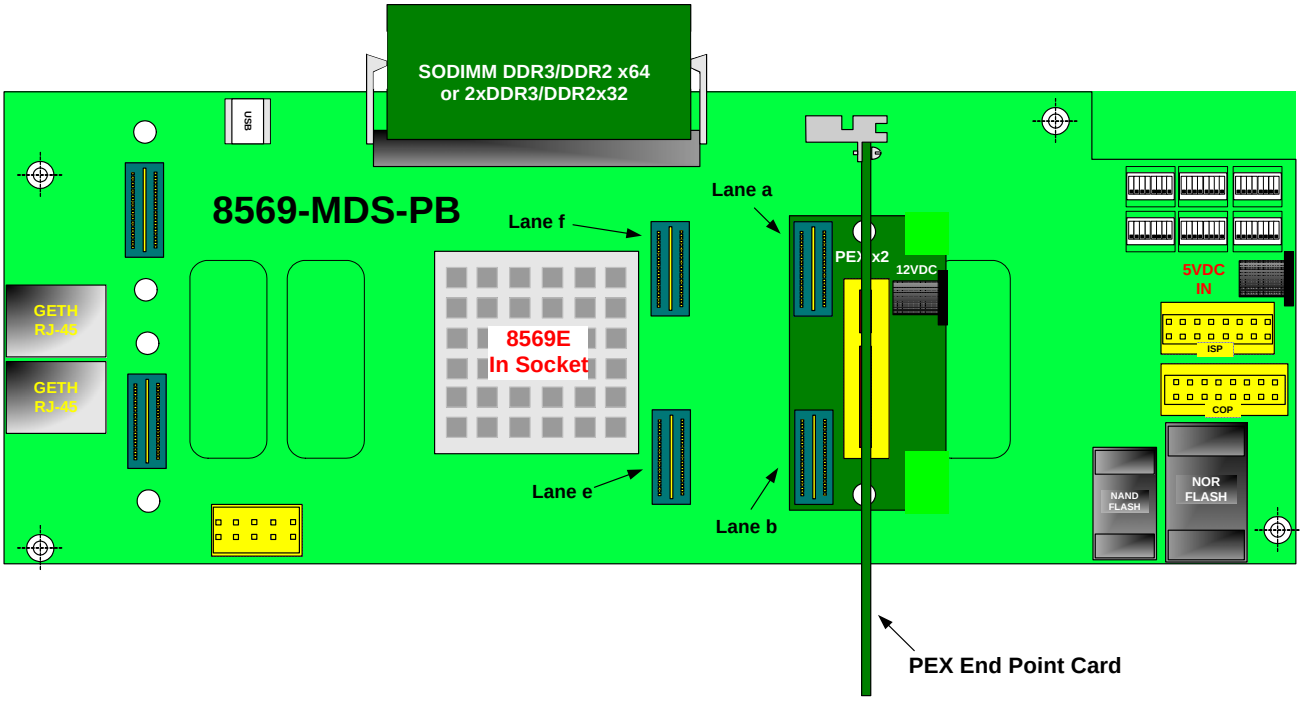


Table 6-5 lists PEX x2 connector pin assignments.

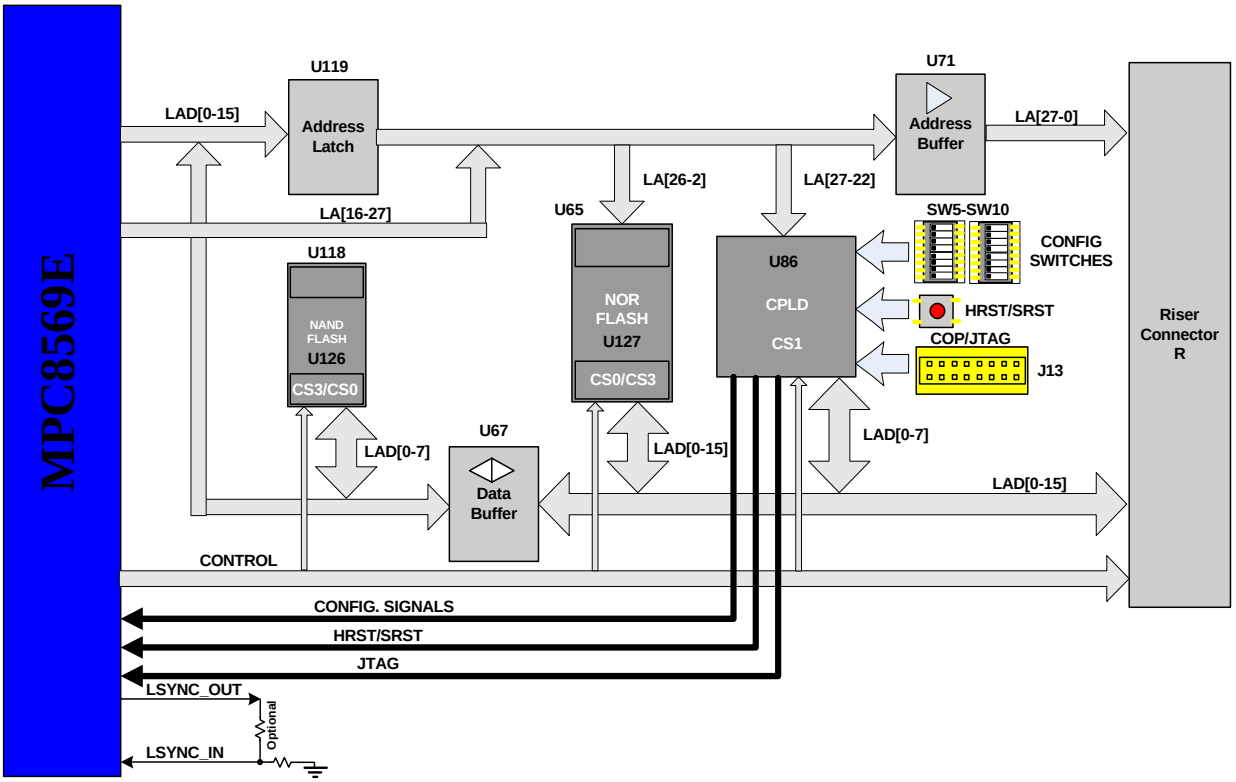
Table 6-5. PEX x2 Signal Connector Assignments

Pin	Name	Pin	Name
A11	PERST	B14	TX0
A13	REFCLK	B15	TX0
A14	REFCLK	B19	TX1
A16	RX0	B20	TX1
A17	RX0	-	-
A21	RX1	-	-
A22	RX1	-	-

6.3 eLBC Interface

Figure 6-7 shows principle interface connections on an eLBC block diagram.

Figure 6-7. eLBC Interface



6.3.1 eLBC Interface Overview

The eLBC port connects to a wide variety of external memories, DSPs, and ASICs. The GPCM, UPM, and FCM state-machines can be programmed separately to access different types of devices. All state-machines can reside in the same system.

Every chip select signal can be configured to allow a state-machine control of an associated chip interface:

- GPCM controls access to asynchronous devices using a simple handshake protocol.
- UPM can be programmed to interface with synchronous devices or custom ASIC interfaces.
- FCM or NAND FLASH further extends interface options.

Onboard eLBC interface features are noted in Table 6-6.

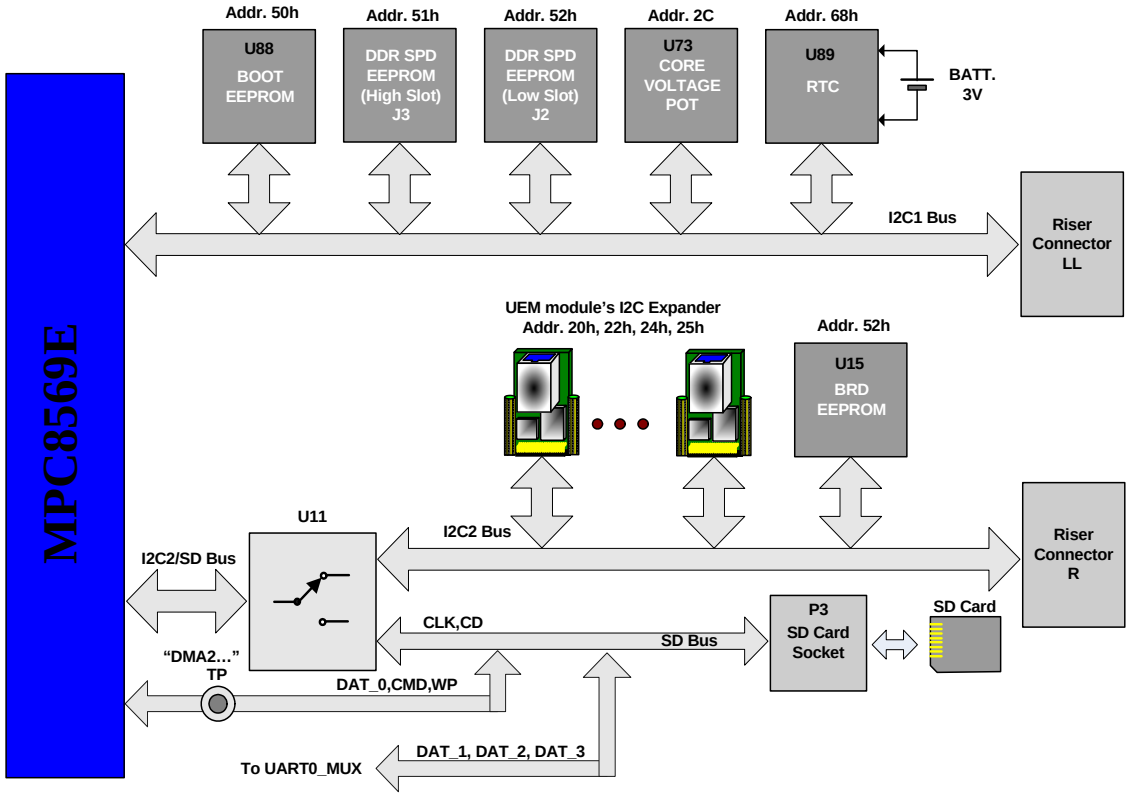
Table 6-6. eLBC Interface Features

Features	Description
NAND FLASH	• Samsung K9F5608U0D-PCB0 • Socketed, onboard memory • 32Mx8Bit (32MB) FLASH device
NOR FLASH	• Spansion S29GL256N11TFIV20 • Socketed, onboard memory • 32Mx8Bit (32MB) Flash device
CPLD-mapped BCSR	• Controls selected PB functions.
Address Latch	• For PIB expansion purposes.
Address Buffer	• For PIB expansion purposes.
Data Buffer	• For slow devices; e.g., CPLD, NOR FLASH, etc.
BOOT	• Selection capability.

6.4 I2C and SD Card Interfaces

Figure 6-8 illustrates an I2C and SD Card interface block diagram.

Figure 6-8. I2C and SD Card Interface Block Diagram



6.4.1 I2C Interface Overview

The MPC8569E has two I2C controllers. These synchronous, multi-master buses can be connected to additional devices for expansion and system development. Non-muxed and muxed buses can be connected to a PIB board for extra functionality and expansion.

Figure 6-8 illustrates the below features:

I2C1 (non-muxed) bus usage:

- Load BOOT EEPROM sequence.
- Read DDR SPD EEPROMs; they provide correct information for using DDR SODIMM.
- VDD controlled via corresponding digital potentiometer.
- Obtain RTC information for application program synchronization.
- Interconnect to PIB for functional expansion.

I2C2 (muxed) bus:

- Used for onboard BRD EEPROM. Enables storage of board-related information such as PCB and CPU revisions, history updates, etc.
- Control I2C expanders are placed on the UEMs.
- SD card interface is an alternative I2C2 bus. Software-related switches provides corresponding interconnections.

The components noted in Table 6-7 are utilized with the I2C interface:

Table 6-7. I2C Interface Components

Feature	Description
BOOT EEPROM	• ST: M24256-BWDW6TG • 256Kbit SERIAL EEPROM
BRD EEPROM	• Atmel: AT24C01A-10TU-2. • 1KB I2C EEPROM
Core Voltage POT	• Analog Device: AD5245BRJZ50-RL7 • 256-Pos I2C Compatible Digi-Pot
RTC	• Maxim: DS1374U-33+ • Real Time Clock
MUX Switches	• TI: TS3L110RGYR • Mux 4Line to 2x4Lines

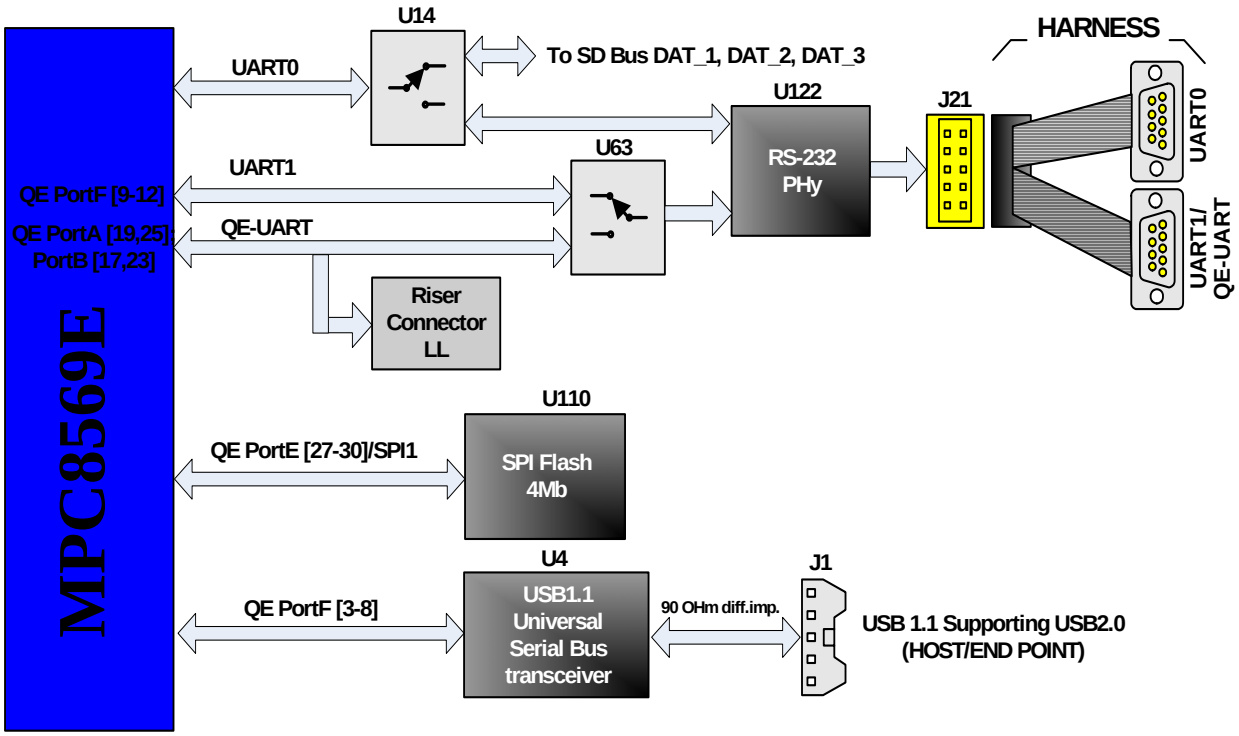
6.4.2 SD Card Interface

eSDHC provides an interface between host system and SD/SDIO/MMC/CE-ATA cards. The SD card is specifically designed to meet the security, capacity, performance, and environmental requirements inherent in emerging audio and video consumer electronic devices.

6.5 RS-232, SPI FLASH, and USB Interfaces

Figure 6-9 is a block diagram illustrating the RS-232, SPI FLASH, and USB interfaces.

Figure 6-9. RS-232, SPI, and USB Interfaces



6.5.1 RS-232 Interface Overview

The RS-232 interface provides an RS-232 standard interconnection between the following: MPC8569E DUART module, QE-mapped universal asynchronous receiver/transmitter (UART), and an external Host.

Table 6-8. RS-232 Interface Components

Feature	Description
RS232 Transceiver	• Analog Devices: ADM561JRSZ 4T5R • RS232 Transceiver 3V3
MUX Switches	• TI: TS3L110RGYR • Mux 4Line to 2x4Lines

The MPC8569E DUART consists of two independent UARTs; see Table 6-9 for feature descriptions.

Table 6-9. MPC8569E UART Features

Features	Description	
UART0	• Defined pins. • Muxed with SD_DAT[1...3] or DMA3 DACK, DREQ, DDONE signals. • Non-muxed RTS signal.	• Noted UART signals are routed to Dual RS-232 PHY and made RS-232 standard compliant. • Connect a pair of standard DB9 connectors, via a complete harness, to create a physical interconnection.
UART1	• Muxed with QE PortF bit [9-12]. • [Option] Reconnect and mux QE UCC UART (PA19 & 25 and PB17 & 23) with UART1signals to test functionality. • [Option] Route signals to PIB to provide ATM, TDM, etc. functionality.	
Full-duplex Operation	-	
SW-programmable Baud Generators	• Divide input clock by 1 to (216 – 1). • Generate a 16x clock for transmitter and receiver engines.	
Modem Control Functions	• CTS • RTS	
SW-selectable Serial Interface Data Format	• Data length • Parity • 1/1.5/2 STOP bit • Baud rate	
Error Detection	• Overrun • Parity • Framing	

Table 6-10 lists RS-232 signals.

Table 6-10. RS-232 Signals

Signal #	Port F Bit#	RS-232 Signal	Alternative Signal	Header J21 Pin#	DB9 Pin#
1	-	• UART0_SOUT (O)	• SD_DAT1	1	UART0/2
2	-	• UART0_SIN (I)	• SD_DAT2	3	UART0/3
3	-	• UART0_CTS_B (I)	• SD_DAT3	2	UART0/7
4	-	• UART0_RTS_B (O)	-	4	UART0/8
5	9	• UART1_SOUT • QE UART SOUT (O)	• Cfg. Device ID5 • PA19	6	UART1/2
6	12	• UART1_SIN • QE UART SIN (I)	• - • PB17	8	UART1/3

Table 6-10. RS-232 Signals

Signal #	Port F Bit#	RS-232 Signal	Alternative Signal	Header J21 Pin#	DB9 Pin#
7	10	• UART1_CTS_B • QE UART CTS (I)	• Cfg. Core Speed • PB23	7	UART1/7
8	11	• UART1_RTS_B • QE UART RTS (O)	• Cfg. Dram Type • PA25	9	UART1/8
9	-	• GND	-	5	UART0/5
10	-	• GND	-	10	UART1/5

6.5.2 SPI FLASH Interface Overview

The SPI management interface defines interconnections with all standard-conforming peripheral devices. The 4 Mbit, low voltage SPI FLASH memory device (ST M25P40VMN6TG) is inserted into the PB for test functionality. Corresponding signals are represented on Port E bit[27-30]. Table 6-11 lists SPI signals.

Table 6-11. SPI Signals

Signal #	Port E Bit#	SPI Signal	Alternative Function
1	27	SPI1_SPIMOSI (IO)	Cfg. DDR PLL0
2	28	SPI1_SPIMISO (IO)	Cfg. DDR PLL1
3	29	SPI1_SPICLK (O)	Cfg. DDR PLL2
4	30	SPI1_SPISEL_B (IO)	-

6.5.3 USB Interface Overview

The USB interface is characterized by the following:

- Supports 12Mbit/s Full-Speed and 1.5Mbit/s Low-Speed serial data transmission.
- Defined to connect with any peripheral device that conforms to the standard USB1.1.
- Interface compatible with USB 2.0 protocol.

Table 6-12. USB Interface Components

Feature	Description
USB Transceiver	NXP: ISP1105W
MUX Switches	IDT: IDT74CBTLV3257PGG Quad, 2:1, MUX/DEMUX bus switch
USB Power Switch	Micrel: MIC2505-2YM

Corresponding signals are represented on Port F bit[3-8]. Table 6-13 lists the USB signals.

Table 6-13. USB Signals

Signal #	Port F Bit#	USB Signal	Alternative Function
1	3	USB_OE (O)	-
2	4	USB_TP (O)	-
3	5	USB_TN (O)	-
4	6	USB_RP (I)	-
5	7	USB_RXD (I)	-
6	8	USB_RN (I)	-

6.6 PIB Interface

6.6.1 PIB Interface Overview

Figure 6-10 illustrates the connection between the PB_MPC8569E_QE Module and the PIB.

Figure 6-10. QE and PIB Interface

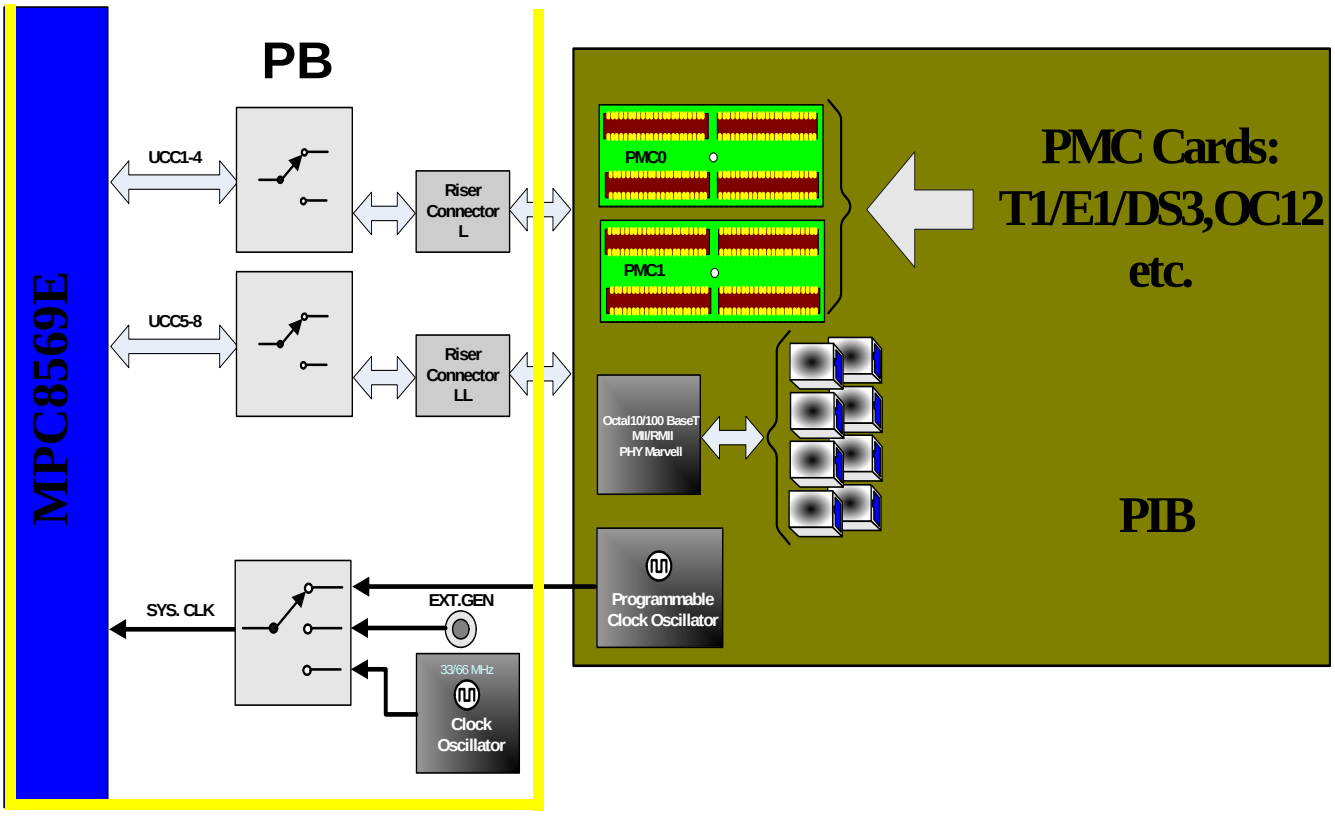
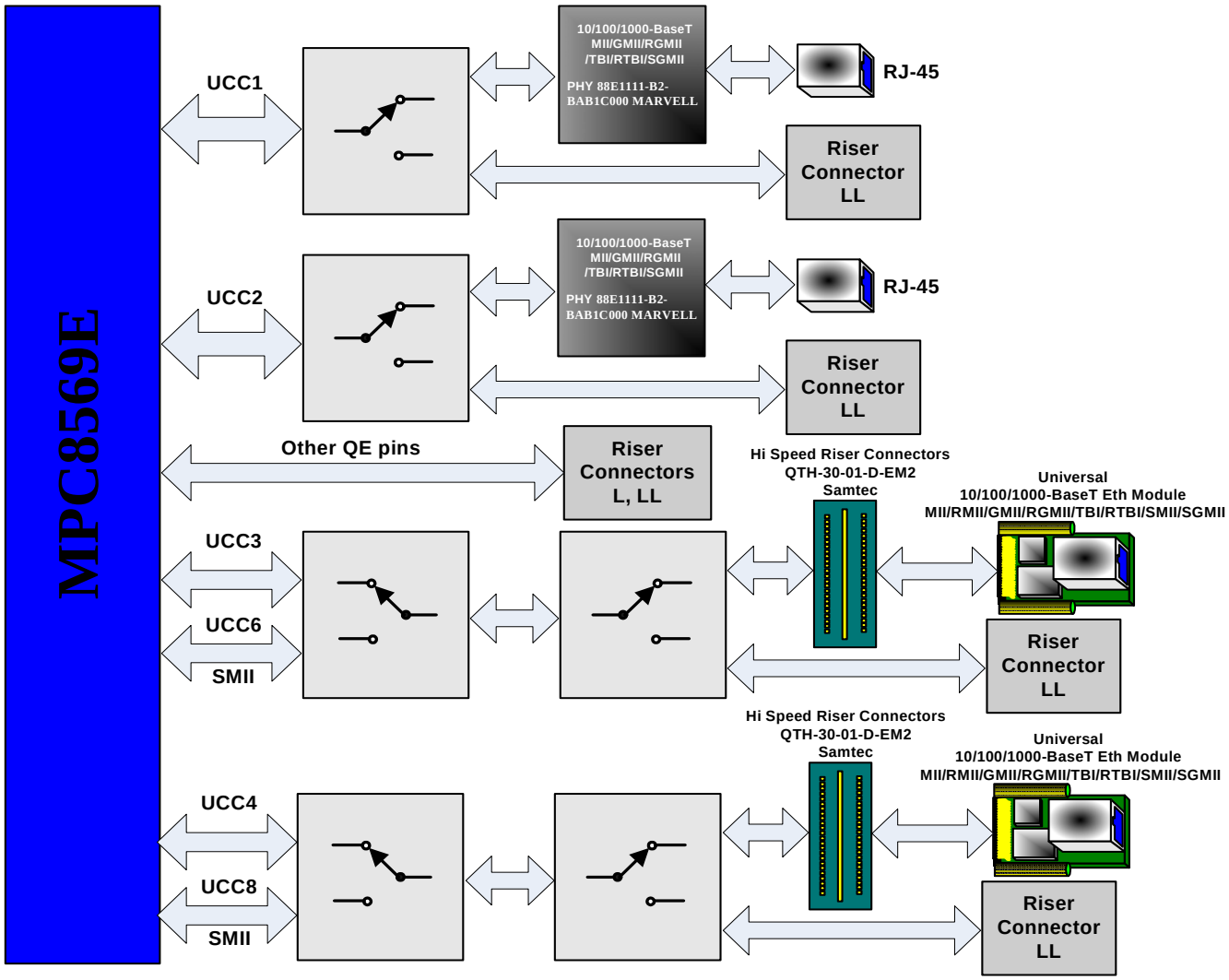


Figure 6-11 shows MPC8569E QE interconnections.

Figure 6-11. QE Interconnections



6.7 GETH Interface

GETH features are noted in Table 6-14.

Table 6-14. GETH Interface Components

Feature	Description
GETH PHY (4)	• Marvel 88E1111 • Connected to UCC1, UCC2, UCC3, and UCC4 ports. • UCC3 and UCC4 are connected via the UEM. • Configure PHYs via PHY internal registers using MDC and MDIO signals.
GETH Port Testing Modes	• [Default] RGMII for 10/100/1000-BaseT • RTBI for 1000Base-T • RTBI for 10/100 MII

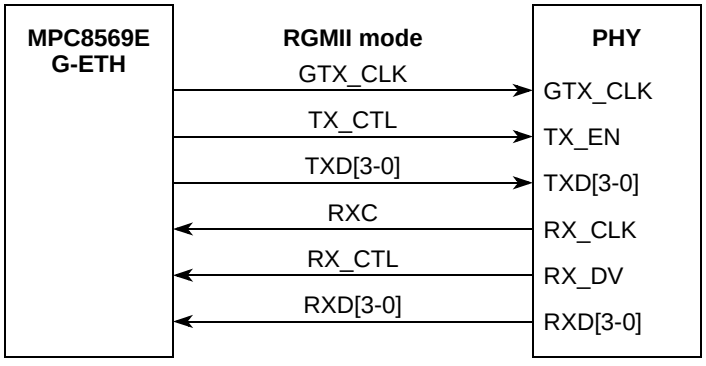
6.7.1 RGMII Interface

RGMII is the default interface at Power-ON and is recommended for the 1000/100/10Base-T speed.

- RGMII interface supports RGMII-to-Copper or RGMII-to-Fiber connections at 1000Base-T speed.
- Select RGMII interface by setting 88E1111 HWCFG_MODE [3-0] to 0b1011 or via BCSR control.
- If using 1000Base-T speed then a MPC8569E 125 MHz input is taken from the PHY.
  - Each PHY drives its own 125 MHz clock to the appropriate UCC.
  - MPC8569E RGMII interface transmits a 125MHz clock to the PHY GTX_CLK pin.
  - Use this option to achieve 10, 100, or 1000Base-T speed.

Figure 6-12 shows MPC8569E (with Marvel 88E1111 device) and PHY signal mapping to the RGMII interface.

Figure 6-12. RGMII Interface Device Signal Mapping



The RGMII interface reduces (to 12) the number of pins between PHY and MPC8569E. The RGMII-to-Copper interface powers-up through MDC and MDIO pins or via BCSR. Table 6-15 lists corresponding RGMII and PHY signals.

Table 6-15. RGMII and PHY Signals

RGMII Signal Name	PHY Signal Name
GTX_CLK	GTX_CLK
TX_EN	TX_EN
TXD[3-0]	TXD[3-0]
RX_CLK	RX_CLK
RX_CTL	RX_DV
RXD[3-0]	RXD[3-0]

6.7.2 Reduced 10-bit Interface (RTBI)

RTBI supports 1000Base-T speed and reduces (to 12) the number of pins between PHY and MPC8569E.

1. Select the RTBI-to-Copper interface: application software should make the selection via MDC and MDIO pins.
2. Select RTBI mode for any UCC(1-4): use BCSR to set a mode configuration that corresponds to the RTBI mode.

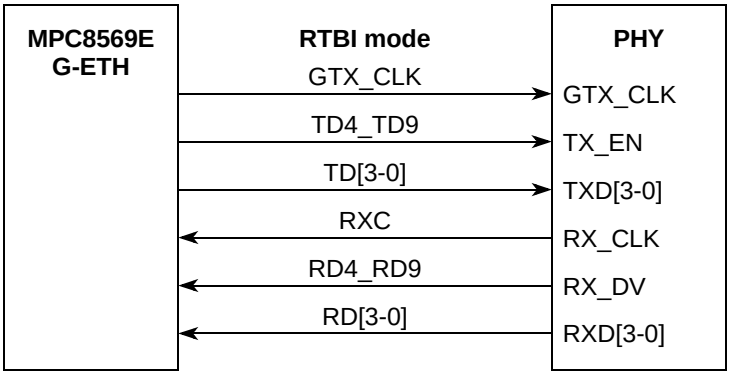
Table 6-16 lists RTBI interface pin mapping.

Table 6-16. RTBI Interface Pin Mapping

RTBI Signal Name	PHY Signal Name
GTX_CLK	GTX_CLK
TD4_TD9	TX_EN
TD [0-3]	TXD [3-0]
RCX	RXCLK
RD4_RD9	RX_DV
RD [3-0]	RXD [3-0]

Figure 6-13 shows MPC8569E and PHY in RTBI mode signal mapping.

Figure 6-13. RTBI Mode Signal Mapping



6.8 QE Interface

6.8.1 Communication Ports

PB communication ports allow for a variety of QE evaluations though it isn't possible to provide all QE-supported communication interface types. The PB and PIB, via riser connectors on the board, provide the MPC8569E with convenient communication interface device connections.

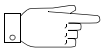
Long layout traces between QE pins and their expansion connectors are avoided as each board QE pin is automatically disconnected from the riser connector.

PB and PIB communication port interfaces:

- UCC1-UCC4 RGMII/RTBI
- UPC1 ATM 155 MHz with Utopia 16-bits
- 16TDM

6.8.2 Mode Selection

Table 6-17 indicates the significance of the colors used in Table 6-18, "QE Functions". The table shows a selected number of application types (as listed in the column headings) and their related pins.



It is possible to choose different application types as long as pin blocks are maintained.

Table 6-17. PQ-MDS-PIB Connector Table Color Legend

Clocks
MII Management
QE_UART0
QE_UART1
RGMII
RMII
SMII
SPI
TDM1
TDM2
UPC1 Dev0
UPC1 Dev1
UPC1 Dev2
UPC1 Dev3
UPC1 POS
USB

Table 6-18. QE Functions

PQ Pin	16TDM, 2RGMII, 1RMII, USB	11TDM, 8RMII, USB	5TDM, 4RGMII, ATM Multidevice MultiPHY USB	5TDM, 2RGMII POS Multidevice MultiPHY
PA10	TDM1a- TXD[0]	TDM1a- TXD[0]	Dev3-TxEN_B[3]	TDM1a- TXD[0]
PA5	TDM1a- RXD[0]	TDM1a- RXD[0]	Dev3-TxCLAV[3]	TDM1a- RXD[0]
PA11	TDM1a- RSYNC	TDM1a- RSYNC	Dev3-RxCLAV[3]	TDM1a- RSYNC
PA28			Dev2- TxCLAV[2]	
PA3	RGMII-Enet1_TXD[3]		RGMII-Enet1_TXD[3]	RGMII-Enet1_TXD[3]
PA2	RGMII-Enet1_TXD[2]		RGMII-Enet1_TXD[2]	RGMII-Enet1_TXD[2]
PA8	RGMII-Enet1_RXD[2]		RGMII-Enet1_RXD[2]	RGMII-Enet1_RXD[2]
PA9	RGMII-Enet1_RXD[3]		RGMII-Enet1_RXD[3]	RGMII-Enet1_RXD[3]
PA12	RGMII-Enet1_RX_DV	RMII1- Enet1_RX_DV	RGMII-Enet1_RX_DV	RGMII-Enet1_RX_DV
PA4	RGMII-Enet1_TX_EN	RMII1- Enet1_TX_EN	RGMII-Enet1_TX_EN	RGMII-Enet1_TX_EN
PA1	RGMII-Enet1_TXD[1]	RMII1- Enet1_TXD[1]	RGMII-Enet1_TXD[1]	RGMII-Enet1_TXD[1]
PA0	RGMII-Enet1_TXD[0]	RMII1- Enet1_TXD[0]	RGMII-Enet1_TXD[0]	RGMII-Enet1_TXD[0]
PA7	RGMII-Enet1_RXD[1]	RMII1- Enet1_RXD[1]	RGMII-Enet1_RXD[1]	RGMII-Enet1_RXD[1]
PA6	RGMII-Enet1_RXD[0]	RMII1- Enet1_RXD[0]	RGMII-Enet1_RXD[0]	RGMII-Enet1_RXD[0]
PA13	TDM1a-TSYNC			TDM1a-TSYNC
PB11			Dev3-RxEN_B[3]	
PB7	TDM2c-TXD[0]	TDM2c-TXD[0]	Dev2-TxEN_B[2]	TDM2c-TXD[0]
PB2	TDM2c-RXD[0]	TDM2c-RXD[0]	Dev2-RxCLAV[2]	TDM2c-RXD[0]
PB8	TDM2c-RSYNC	TDM2c-RSYNC		TDM2c-RSYNC
PB0	TDM2c-TSYNC	TDM2c-TSYNC	RGMII-Enet3_TXD[3]	
PA31			RGMII-Enet3_TXD[2]	
PB5			RGMII-Enet3_RXD[2]	
PB6			RGMII-Enet3_RXD[3]	
PB4		RMII3- Enet3_RXD[1]	RGMII-Enet3_RXD[1]	Dev2- RxEN_B[2]
PA29	TDM1c- TXD[0]	RMII3- Enet3_TXD[0]	RGMII-Enet3_TXD[0]	
PB3	TDM1c- RXD[0]	RMII3- Enet3_RXD[0]	RGMII-Enet3_RXD[0]	
PB9	TDM1c- TSYNC	RMII3- Enet3_RX_DV	RGMII-Enet3_RX_DV	
PB1		RMII3- Enet3_TX_EN	RGMII-Enet3_TX_EN	
PA30		RMII3- Enet3_TXD[1]	RGMII-Enet3_TXD[1]	
PB10	TDM1c-RSYNC		TDM2c-TSYNC	TDM2c-TSYNC
PD1	RMII5- Enet5_TXD[1]	RMII5- Enet5_TXD[1]	TxEN_B[0]	TxEN_B[0]
PD7	RMII5- Enet5_RXD[1]	RMII5- Enet5_RXD[1]	TxDATA[11]	TxDATA[11]
PD0	RMII5- Enet5_TXD[0]	RMII5- Enet5_TXD[0]	TxSOC	TxSOC
PD6	RMII5- Enet5_RXD[0]	RMII5- Enet5_RXD[0]	TxDATA[12]	TxDATA[12]
PD4	RMII5- Enet5_TX_EN	RMII5- Enet5_TX_EN	TxDATA[14]	TxDATA[14]
PD12	RMII5- Enet5_RX_DV	RMII5- Enet5_RX_DV	TxDATA[15]	TxDATA[15]
PD13			RxDATA[14]	RxDATA[14]
PD9			TxDATA[9]	TxDATA[9]
PD8			TxDATA[10]	TxDATA[10]
PD2			TxCLAV[0]	TxCLAV[0]
PD11	TDM2e- RSYNC	TDM2e- RSYNC	TxDATA[7]	TxDATA[7]
PD10	TDM2e- TXD[0]	TDM2e- TXD[0]	TxDATA[8]	TxDATA[8]
PD5	TDM2e- RXD[0]	TDM2e- RXD[0]	TxDATA[13]	TxDATA[13]
PD3	TDM2e- TSYNC	TDM2e- TSYNC	RxDATA[15]	RxDATA[15]
PD31	TDM1g- TSYNC	TDM1g- TSYNC	RxDATA[10]	RxDATA[10]
PE1	TDM1g- RXD[0]	TDM1g- RXD[0]	RxDATA[8]	RxDATA[8]
PE6	TDM1g- TXD[0]	TDM1g- TXD[0]	TxPRTY	TxPRTY
PE7	TDM1g- RSYNC	TDM1g- RSYNC	RxPRTY	RxPRTY
PD30			RxDATA[11]	RxDATA[11]
PE4			RxEN_B[0]	RxEN_B[0]
PE5			RxCLAV[0]	RxCLAV[0]
PD29		RMII7- Enet7_TXD[1]	RxDATA[12]	RxDATA[12]
PE3		RMII7- Enet7_RXD[1]	RxSOC	RxSOC

PQ Pin	16TDM, 2RGMII, 1RMII, USB	11TDM, 8RMII, USB	5TDM, 4RGMII, ATM Multidevice MultiPHY USB	5TDM, 2RGMII POS Multidevice MultiPHY
PD28	TDM2g- TXD[0]	RMII7- Enet7_TXD[0]	RxDATA[13]	RxDATA[13]
PE2	TDM2g- RXD[0]	RMII7- Enet7_RXD[0]	RxDATA[7]	RxDATA[7]
PE0		RMII7- Enet7_TX_EN	RxDATA[9]	RxDATA[9]
PE8	TDM2g- TSYNC	RMII7- Enet7_RX_DV	RxEN_B[1]	RxEN_B[1]
PE9	TDM2g- RSYNC		TxEN_B[1]	TxEN_B[1]
PA19	TDM2b- RXD[0]	TDM2b- RXD[0]		QE_UART_TXD
PA24	TDM2b- TXD[0]	TDM2b- TXD[0]		TDM2b- TXD[0]
PA25	TDM2b- RSYNC	TDM2b- RSYNC		QE_UART_RTS
PA17	RGMII- Enet2_TXD[3]		RGMII- Enet2_TXD[3]	RGMII- Enet2_TXD[3]
PA16	RGMII- Enet2_TXD[2]		RGMII- Enet2_TXD[2]	RGMII- Enet2_TXD[2]
PA23	RGMII- Enet2_RXD[3]		RGMII- Enet2_RXD[3]	RGMII- Enet2_RXD[3]
PA22	RGMII- Enet2_RXD[2]		RGMII- Enet2_RXD[2]	RGMII- Enet2_RXD[2]
PA18	RGMII- Enet2_TX_EN	RMII2- Enet2_TX_EN	RGMII- Enet2_TX_EN	RGMII- Enet2_TX_EN
PA26	RGMII- Enet2_RX_DV	RMII2- Enet2_RX_DV	RGMII- Enet2_RX_DV	RGMII- Enet2_RX_DV
PA20	RGMII- Enet2_RXD[0]	RMII2- Enet2_RXD[0]	RGMII- Enet2_RXD[0]	RGMII- Enet2_RXD[0]
PA21	RGMII- Enet2_RXD[1]	RMII2- Enet2_RXD[1]	RGMII- Enet2_RXD[1]	RGMII- Enet2_RXD[1]
PA14	RGMII- Enet2_TXD[0]	RMII2- Enet2_TXD[0]	RGMII- Enet2_TXD[0]	RGMII- Enet2_TXD[0]
PA15	RGMII- Enet2_TXD[1]	RMII2- Enet2_TXD[1]	RGMII- Enet2_TXD[1]	RGMII- Enet2_TXD[1]
PA27	TDM2b- TSYNC	TDM2b- TSYNC	TDM2b- TSYNC	TDM2b- TSYNC
PB17	TDM1d- RXD[0]	TDM1d- RXD[0]		QE_UART_RXD
PB22	TDM1d- TXD[0]	TDM1d- TXD[0]		TDM1d- TXD[0]
PB23	TDM1d- RSYNC	TDM1d- RSYNC		QE_UART_CTS
PB15	RGMII- Enet4_TXD[3]		RGMII- Enet4_TXD[3]	RGMII- Enet4_TXD[3]
PB14	RGMII- Enet4_TXD[2]		RGMII- Enet4_TXD[2]	RGMII- Enet4_TXD[2]
PB21	RGMII- Enet4_RXD[3]		RGMII- Enet4_RXD[3]	RGMII- Enet4_RXD[3]
PB20	RGMII- Enet4_RXD[2]		RGMII- Enet4_RXD[2]	RGMII- Enet4_RXD[2]
PB13	RGMII- Enet4_TXD[1]	RMII4- Enet4_TXD[1]	RGMII- Enet4_TXD[1]	RGMII- Enet4_TXD[1]
PB12	RGMII- Enet4_TXD[0]	RMII4- Enet4_TXD[0]	RGMII- Enet4_TXD[0]	RGMII- Enet4_TXD[0]
PB19	RGMII- Enet4_RXD[1]	RMII4- Enet4_RXD[1]	RGMII- Enet4_RXD[1]	RGMII- Enet4_RXD[1]
PB18	RGMII- Enet4_RXD[0]	RMII4- Enet4_RXD[0]	RGMII- Enet4_RXD[0]	RGMII- Enet4_RXD[0]
PB16	RGMII- Enet4_TX_EN	RMII4- Enet4_TX_EN	RGMII- Enet4_TX_EN	RGMII- Enet4_TX_EN
PB24	RGMII- Enet4_RX_DV	RMII4- Enet4_RX_DV	RGMII- Enet4_RX_DV	RGMII- Enet4_RX_DV
PB25	TDM1d- TSYNC		TDM1d- TSYNC	TDM1d- TSYNC
PD14	TDM2f- TXD[0]	RMII6- Enet6_TXD[0]	TxDATA[6]	TxDATA[6]
PD20	TDM2f- RXD[0]	RMII6- Enet6_RXD[0]	TxDATA[2]	TxDATA[2]
PD26	TDM2f- TSYNC	RMII6- Enet6_RX_DV	RxDATA[4]	RxDATA[4]
PD27	TDM2f- RSYNC		RxDATA[5]	RxDATA[5]
PD15		RMII6- Enet6_TXD[1]	TxDATA[5]	TxDATA[5]
PD21		RMII6- Enet6_RXD[1]	TxDATA[3]	TxDATA[3]
PD18	TDM2d- RXD[0]	RMII6- Enet6_TX_EN	RxDATA[0]	RxDATA[0]
PD22	TDM2d- TXD[0]		RxDATA[6]	RxDATA[6]
PD23	TDM2d- RSYNC		TxDATA[1]	TxDATA[1]
PD16	TDM2d- TSYNC		RxDATA[2]	RxDATA[2]
PD17	TDM1f- TSYNC	TDM1f- TSYNC	RxDATA[1]	RxDATA[1]
PD19	TDM1f- RXD[0]	TDM1f- RXD[0]	RxDATA[3]	RxDATA[3]
PD24	TDM1f- TXD[0]	TDM1f- TXD[0]	TxDATA[0]	TxDATA[0]
PD25	TDM1f- RSYNC	TDM1f- RSYNC	TxDATA[4]	TxDATA[4]
PE10	TDM1h- TXD[0]	RMII8- Enet8_TXD[0]	RxADDR[2]	SMI8- Enet8_TXD[0]
PE11	TDM1h- TSYNC	RMI8- Enet8_TXD[1]	RxADDR[4]	SMI8- Enet8_SYNC
PE16	TDM1h- RXD[0]	RMII8- Enet8_RXD[0]	TxADDR[2]	SMI8- Enet8_RXD[0]
PE23	TDM1h- RSYNC		TxADDR[4]	
PE14	SMI6- Enet6_RXD[0]	RMII8- Enet8_TX_EN	RxADDR[3]	SMI6- Enet6_RXD[0]
PE17	SMI6- Enet6_TXD[0	RMII8- Enet8_RXD[1]	TxADDR[3]	SMI6- Enet6_TXD[0
PE22	SMI6-Enet6_SYNC	RMII8- Enet8_RX_DV	RxADDR[5]	SMI6-Enet6_SYNC
PE13			RxADDR[0]	

PQ Pin	16TDM, 2RGMII, 1RMII, USB	11TDM, 8RMII, USB	5TDM, 4RGMII, ATM Multidevice MultiPHY USB	5TDM, 2RGMII POS Multidevice MultiPHY
PE21	TDM2h- RSYNC	TDM2h- RSYNC	TxADDR[1]	TxADDR[1]
PE12	TDM2h- TSYNC	TDM2h- TSYNC	TxADDR[5]	TxADDR[5]
PE15	TDM2h- RXD[0]	TDM2h- RXD[0]	RxADDR[1]	RxADDR[1]
PE20	TDM2h- TXD[0]	TDM2h- TXD[0]	TxADDR[0]	TxADDR[0]
PE19			TxCLAV[1]	TxCLAV[1]
PE18			RxCLAV[1]	RxCLAV[1]
PE31	TDM1b- TSYNC	TDM1b- TSYNC	TDM1b- TSYNC	TDM1b- TSYNC
PF0	TDM1b- RXD[0]	TDM1b- RXD[0]	TDM1b- RXD[0]	TDM1b- RXD[0]
PF1	TDM1b- TXD[0]	TDM1b- TXD[0]	TDM1b- TXD[0]	TDM1b- TXD[0]
PF2	TDM1b- RSYNC	TDM1b- RSYNC	TDM1b- RSYNC	TDM1b- RSYNC
PF3	*USB_OE	*USB_OE	*USB_OE	*USB_OE
PF4	USB_TP	USB_TP	USB_TP	USB_TP
PF5	USB_TN	USB_TN	USB_TN	USB_TN
PF6	USB_RP	USB_RP	USB_RP	USB_RP
PF7	USB_RXD	USB_RXD	USB_RXD	USB_RXD
PF8	USB_RN	USB_RN	USB_RN	USB_RN
PF15	TDM2a- TSYNC	TDM2a- TSYNC	TDM2a- TSYNC	POS- TMOD
PF16	TDM2a- TXD[0]	TDM2a- TXD[0]	TDM2a- TXD[0]	POS- RMOD
PF17	TDM2a- RXD[0]	TDM2a- RXD[0]	TDM2a- RXD[0]	POS- STPA
PF18	TDM2a- RSYNC	TDM2a- RSYNC	TDM2a- RSYNC	POS- REOP
PF19	TDM1e- TSYNC	TDM1e- TSYNC	TDM1e- TSYNC	POS- TEOP
PF20	TDM1e- TXD[0]	TDM1e- TXD[0]	TDM1e- TXD[0]	POS- TERR
PF21	TDM1e- RXD[0]	TDM1e- RXD[0]	TDM1e- RXD[0]	POS- RERR
PF22	TDM1e- RSYNC	TDM1e- RSYNC	TDM1e- RSYNC	POS- RVAL
PC8	UCC1-RXCLK	CLK9		
PC20	UCC1-GTXCLK	CLK21		
PC11	UCC1,3-IN125	CLK12		
PC9	UCC3-RXCLK	CLK10		
PC25	UCC3-GTXCLK	CLK26		
PC3	UCC2-RXCLK	CLK4		
PC2	UCC2-GTXCLK	CLK3		
PC16	UCC2,4-IN125	CLK17		
PC17	UCC4-RXCLK	CLK18		
PC24	UCC4-GTXCLK	CLK25		
PC15	RMII1-8	CLK16		
PC4	USB_CLK	CLK5		
PC18	UPC-RXCLK	CLK19		
PC12	UPC-TXCLK	CLK13		
PC0	TDM-SI1-TX-RX-A,B,C,D	CLK1		
PC22	TDM-SI1-RX-TX-E,F,G,H	CLK23		
PC13	TDM-SI2-RX-TX-A,B,C,D	CLK14		
PC26	TDM-SI2-RX-TX-E,F,G,H	CLK27		
PE27	SPI1_SPIMOSI	SPI1_SPIMOSI		
PE28	SPI1_SPIMISO	SPI1_SPIMISO		
PE29	SPI1_SPICLK	SPI1_SPICLK		
PE30	SPI_ENABLE	SPI_ENABLE		
PF9	UART1_SOUT	UART1_SOUT		
PF10	UART1_CTS_B	UART1_CTS_B		
PF11	UART1_RTS_B	UART1_RTS_B		
PF12	UART1_SIN	UART1_SIN		
PC30	SPI2-MDC			
PC31	SPI2-MDIO			

Table 6-19 lists QE clock distributions for the application scenarios found in Table 6-18, “QE Functions”

Table 6-19. QE Clock Distributions

PQ Pin	16TDM, 2RGMII, 1RMII, USB	11TDM, 8RMII, USB
PC8	UCC1-RXCLK	CLK9
PC20	UCC1-GTXCLK	CLK21
PC11	UCC1,3-IN125	CLK12
PC9	UCC3-RXCLK	CLK10
PC25	UCC3-GTXCLK	CLK26
PC3	UCC2-RXCLK	CLK4
PC2	UCC2-GTXCLK	CLK3
PC16	UCC2,4-IN125	CLK17
PC17	UCC4-RXCLK	CLK18
PC24	UCC4-GTXCLK	CLK25
PC15	RMII1-8	CLK16
PC18	UPC-RXCLK	CLK19
PC12	UPC-TXCLK	CLK13
PC0	TDM-SI1-TX-RX-A,B,C,D	CLK1
PC22	TDM-SI1-RX-TX-E,F,G,H	CLK23
PC13	TDM-SI2-RX-TX-A,B,C,D	CLK14
PC26	TDM-SI2-RX-TX-E,F,G,H	CLK27

6.8.3 Riser Connectors

PB riser connectors, including QE and local bus pins, provide full access to both the MPC8569E QE and local bus signals.

Chapter 7: Memory Maps

7.1 MPC8569E PB Memory Map

The memory map has NOT been finalized.

Access to MPC8569E memory slaves is controlled by the MPC8569E memory controller. Table 7-1 is only a recommended memory map; it is a "soft" map device. Users are free to move addresses around the map.

Table 7-1. MPC8569E-MDS-PB Memory Map (with NOR Flash as Boot Source**)**

ADDRESS RANGE	Block	Allocation	Port Size
00000000 - 1FFFFFFF	DDR3/DDR3 Memory Controller	MEMC1 (512MB)	32
00000000 - 3FFFFFFF		MEMC1 (Integrated Mode) 1GB	64
20000000 - 3FFFFFFF		MEMC2 (512MB)	32
40000000 - 7FFFFFFF	Reserved	1GB	
80000000 - 9FFFFFFF	SRIO1	Outbound Window (512 MB)	x4 lane
A0000000 - BFFFFFFF	SRIO2	Outbound Window (512 MB)	x4 lane
C0000000 - DFFFFFFF	PEX	Outbound Window (512 MB)	x4 lane
E0000000 - E00FFFFF	MPC8569 Internal Map	Internal Memory Register Space (1 MB)	32
E0100000 - E03FFFFF	Reserved	For future MPC8569 derivatives (3 MB)	-
E0400000 - E047FFFF	L2SRAM	1MB	
E0480000 - F7FFFFFF	Reserved	400MB	
F8000000 - F8007FFF	BCSR on CS1	Altera (32KB)	8
F8008000 - F800FFFF	CS4	PIB (32KB)	8
F8010000 - F8017FFF	CS5	PIB (32KB)	8
FA018000 - FFFFFFFF	Reserved	100MB	
FC000000 - FDFFFFFF	NAND Flash on CS3/CS0	Samsung: K9F5608U0D-PCB0 (32MB)	8
FE000000 - FFFFFFFF	NOR Flash on CS0/CS3	Spansion: S29GL256N11TFIV2O (32MB)	8

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