01 - TITLE PAGE

PROJECT:	MCF5329 Validation Board
PART NUMBER:	
ASSEMBLY NAME:	MCF5329VB
SCHEMATICS:	ECR/KTL/PBH

TABLE OF CONTENTS

COLOR LEGEND

NOTE:
NOTES IN GREEN TEXT ARE GENERAL DESIGN OR SCHEMATIC NOTES

LAYOUT NOTE:
NOTES IN RED TEXT ARE PCB LAYOUT RECOMMENDATIONS OR GUIDLINES

NOTES IN BLACK TEXT INDICATE A PARTICULAR FUNCTIONALITY OF A SPECIFIC PART OF THE SCHEMATIC FOR CLARIFICATION OF THE FUNCTIONALITY.

Launched by Motorola
freescale semiconductor

Revision Control

ECO Number	Rev	Description of Change	Date
	A	Preliminary Schematics	3rd May 05
	B	Revised USB OTG D+/D- connections for U22	25th July 05
	C	Re-wired pin L13 to VSS/GND.	30th Aug 05
	D	Corrected order of FEC TXD & RXD data.	22nd Sept 05
	E	Corrected byte enable signals for the ASRAM	8th Nov 05
	F	Updated USB ULPI interface	2nd Mar 06

NOTE: for all capacitors < 0.1uF in value please use capacitors with either a COG or NPO dielectric.

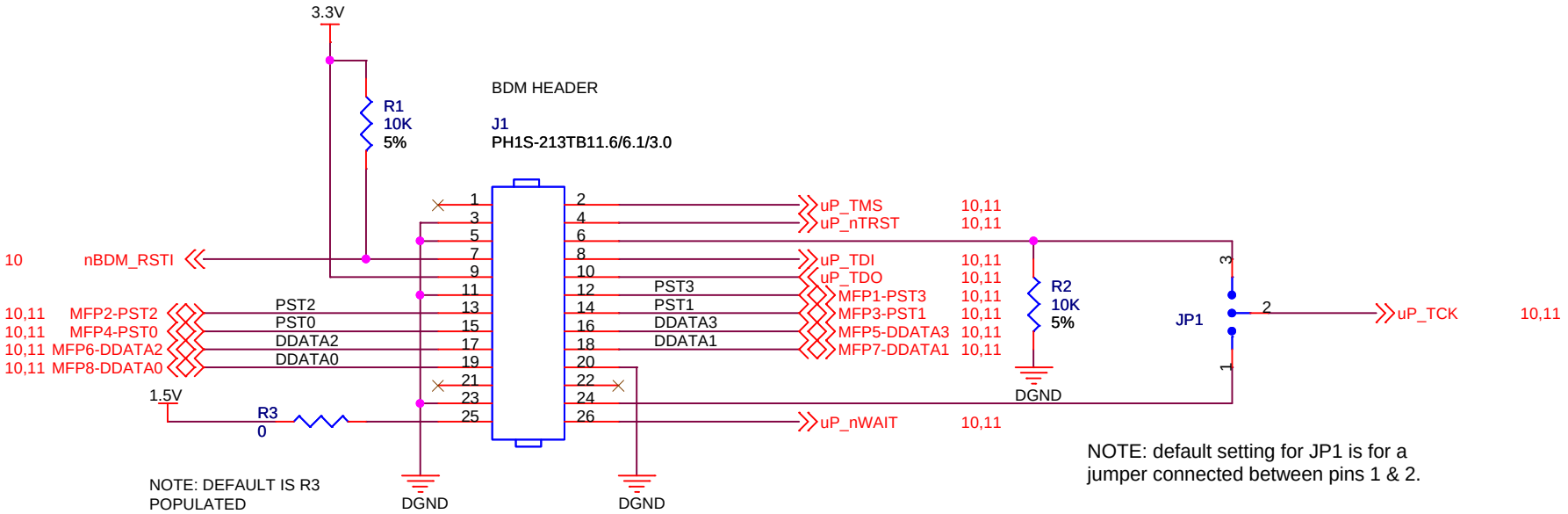
MicroController Division, TSPG, Freescale.

Title: Title & Revison Page

Size: B | Document Number: MCF5329 Validation Board | Rev: F

Date: Wednesday, March 08, 2006 | Sheet 1 of 15

02 - BDM/JTAG



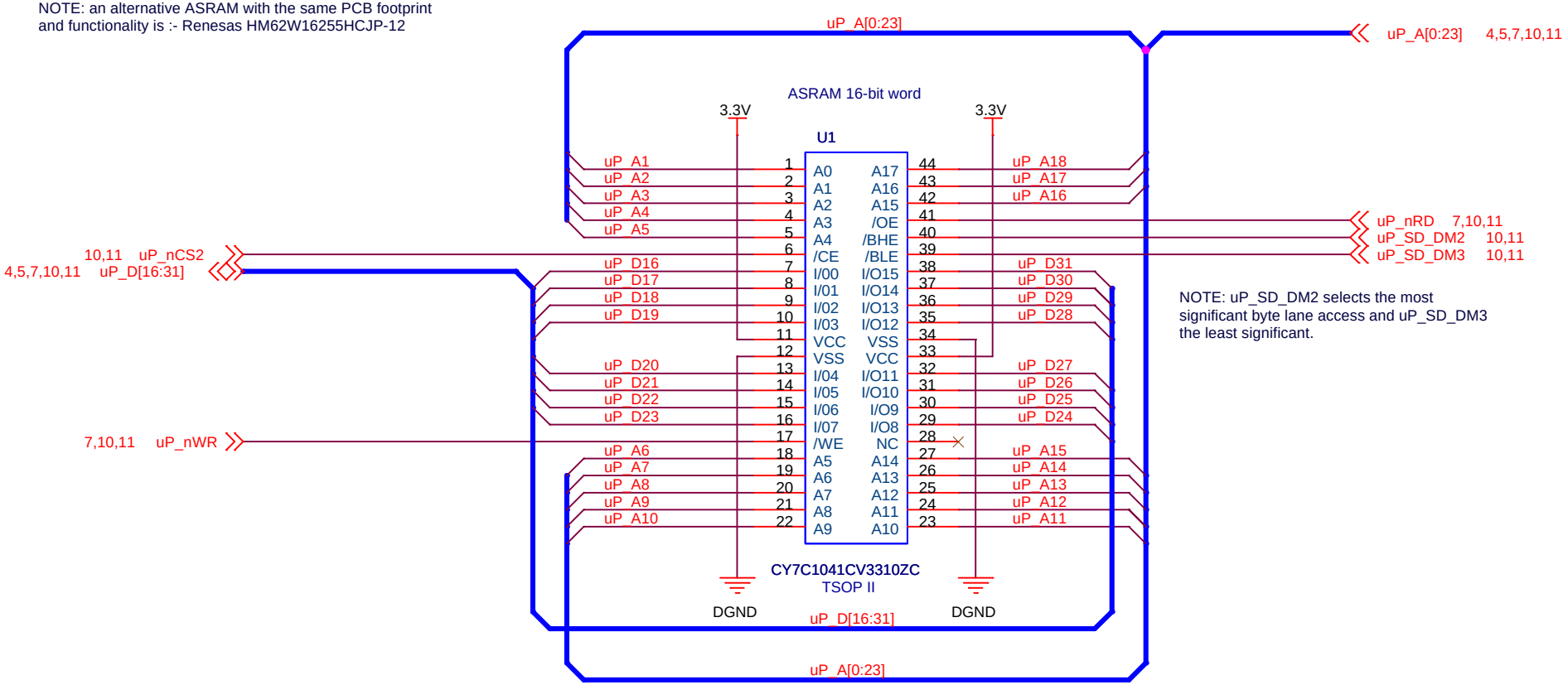
NOTE: ONLY 3.3V BDM debugging cables can be used with MCF532x processors.

MicroController Division, TSPG, Freescale.		
Title: BDM & JTAG connections		
Size: A	Document Number: MCF5329 Validation Board	Rev: F
Date: Wednesday, March 08, 2006	Sheet 2 of 15	

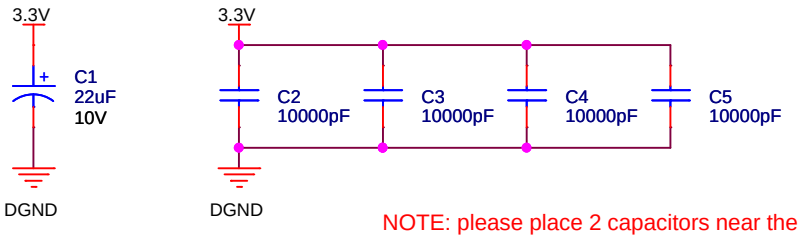
03 - SRAM

ASRAM is a 256K x 16bit (512KB) device

NOTE: an alternative ASRAM with the same PCB footprint
and functionality is :- Renesas HM62W16255HCJP-12



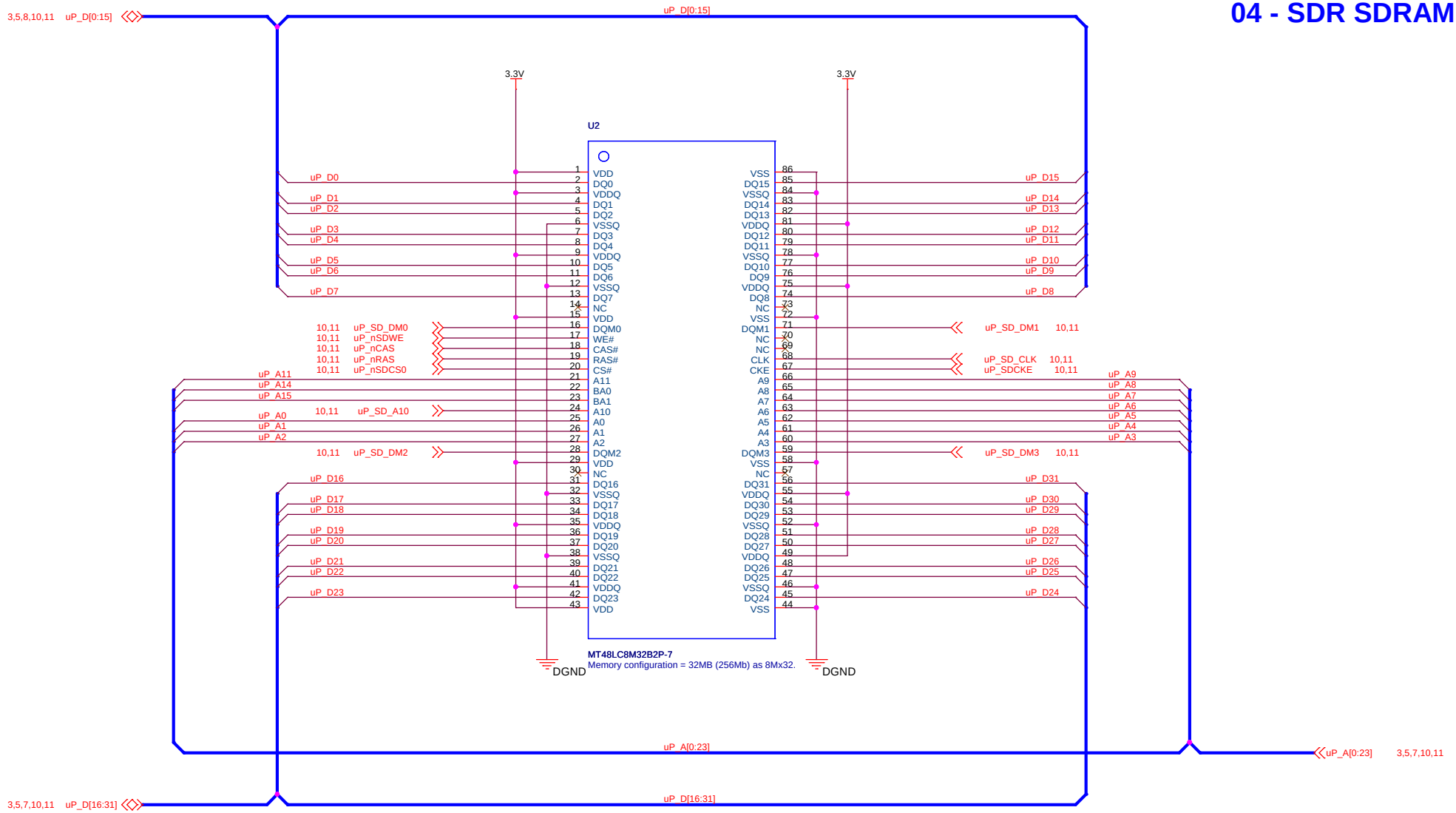
NOTE: uP_SD_DM2 selects the most significant byte lane access and uP_SD_DM3 the least significant.

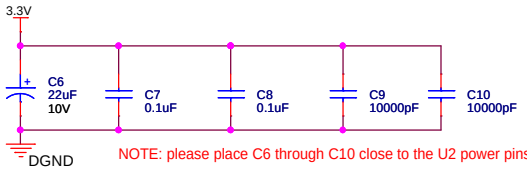


NOTE: please place 2 capacitors near the power pins of each buffer/transceiver, the bulk capacitor (C1) should be placed in the general area of the SRAM.

MicroController Division, TSPG, Freescale.		
Title: Buffers & Transceivers		
Size: A	Document Number: MCF5329 Validation Board	Rev: F
Date: Wednesday, March 08, 2006	Sheet 3 of 15	

04 - SDR SDRAM



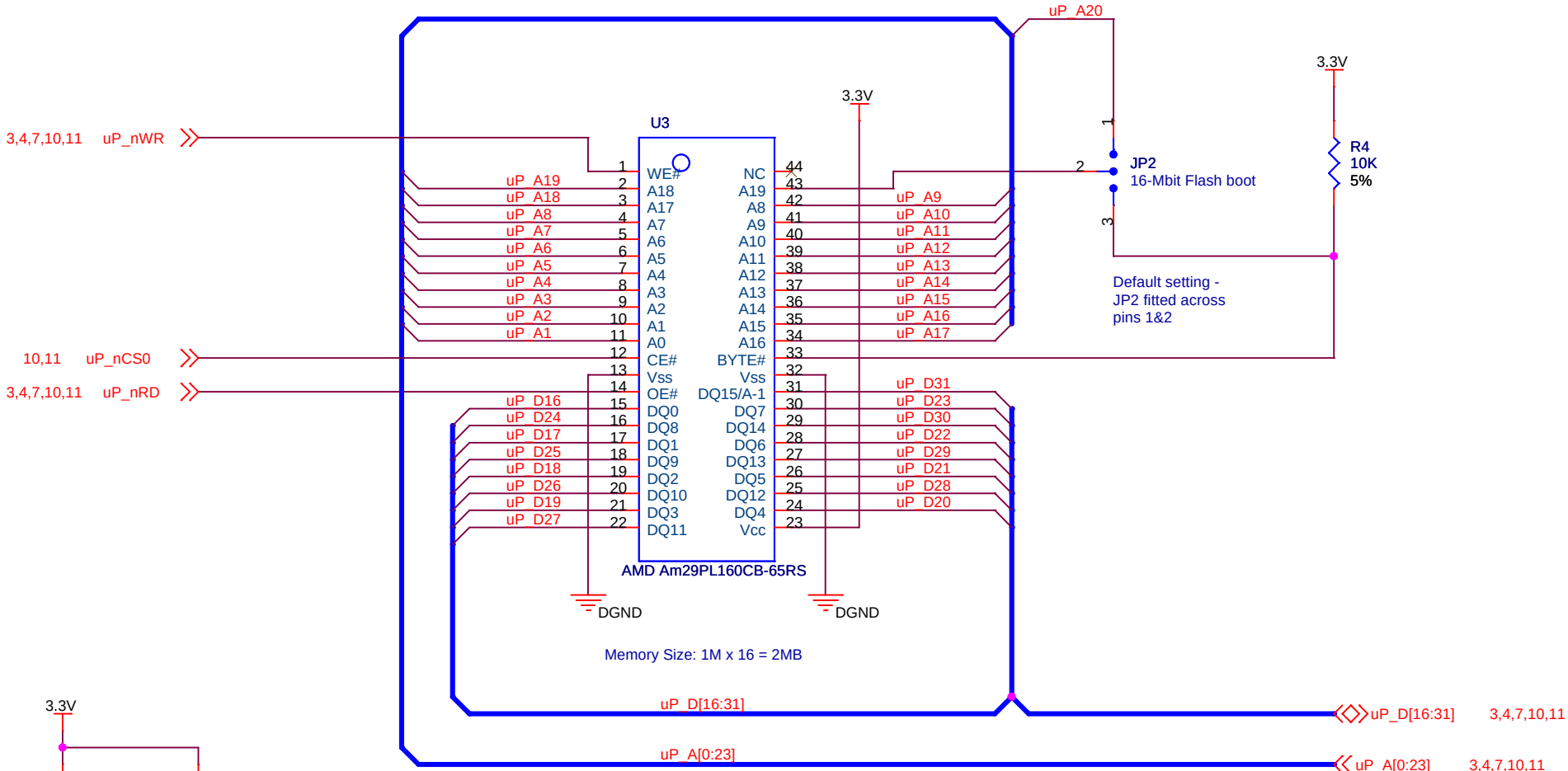


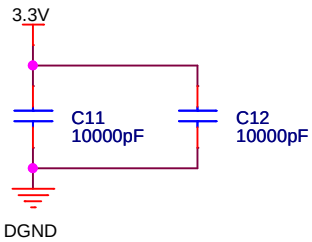
NOTE: please place C6 through C10 close to the U2 power pins.

MicroController Division, TSPG, Freescale.

Title: SDR SDRAM		
Size: B	Document Number: MCF5329 Validation Board	Rev: F
Date: Wednesday, March 08, 2006	Sheet 4 of 15	

05 - FLASH

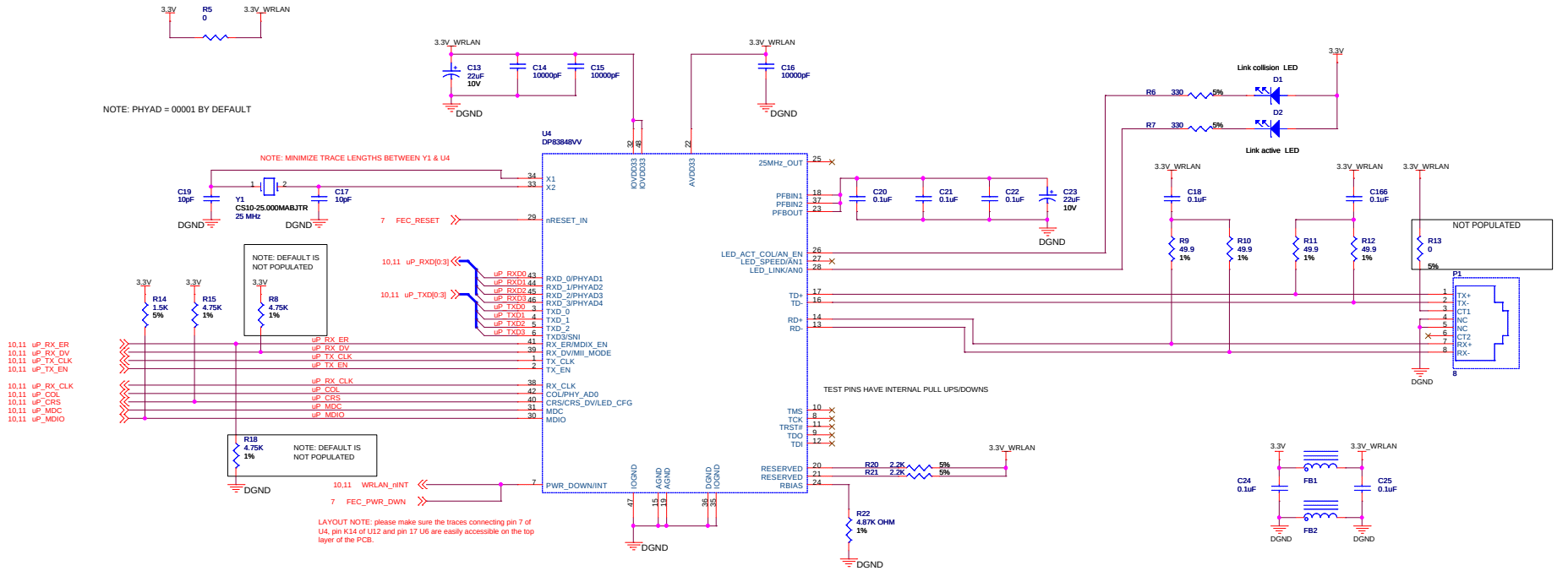




NOTE: please place these two .01uF decoupling cap.s near the Flash memory (U3) supply pins.

MicroController Division, TSPG, Freescale.		
Title: Flash Memory		
Size: A	Document Number: MCF5329 Validation Board	Rev: F
Date: Wednesday, March 08, 2006	Sheet 5 of 15	

06 - WIRED LAN

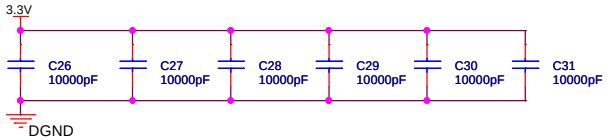


MicroController Division, TSPG, Freescale.

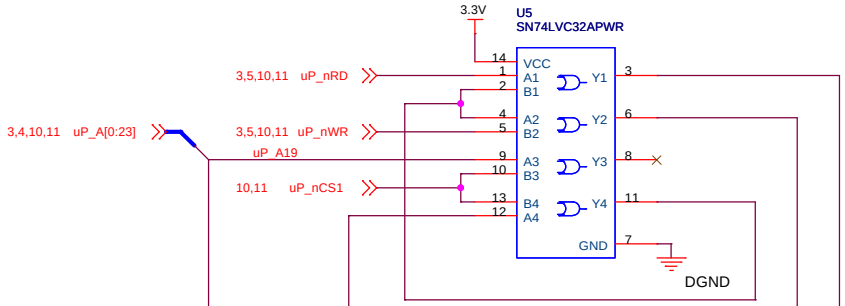
Title	10/100BaseT Ethernet Interface	
Size C	Document Number MCF5329 Validation Board	Rev F
Date: Wednesday, March 08, 2006	Sheet 6 of 15	

07 - LOGIC

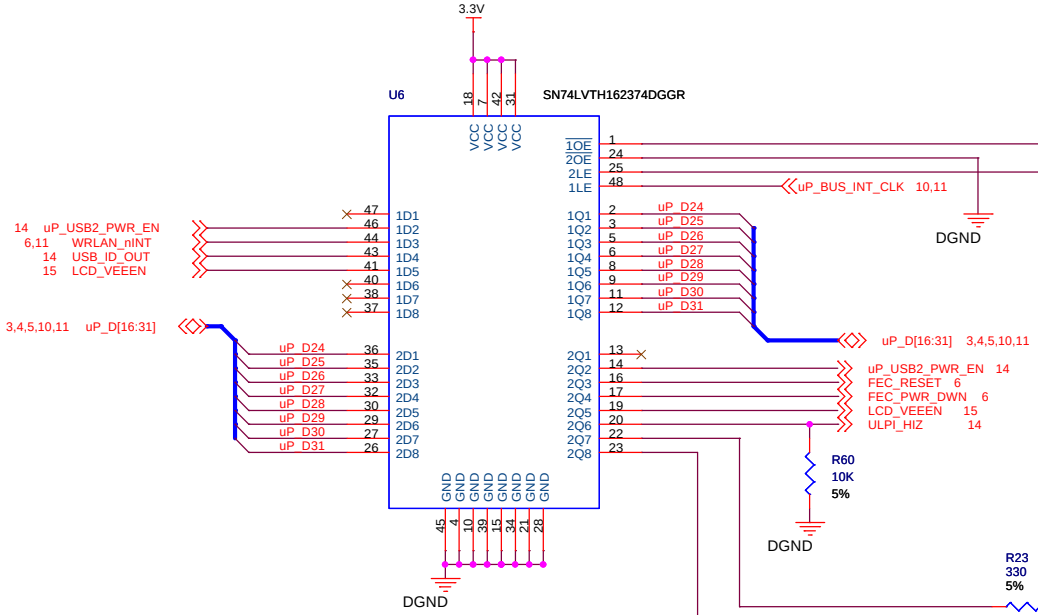
NOTE: PLACE ONE .01uF DECOUPLING CAPS PER CHIP
NEAR EACH LOGIC DEVICE (4 FOR U6) ON THE PCB.



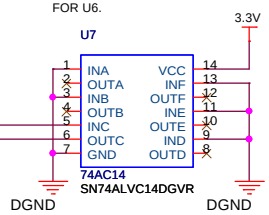
U5 USES THE /CS1, /OE & R/W SIGNALS FROM THE CPU
ALONG WITH ADDRESS LINE A19 TO GENERATE OUTPUT ENABLE
AND LATCH ENABLE SIGNALS FOR U6 THE MEMORY MAPPED
16-BIT LATCH. THE READS AND WRITES TO U6 ARE QUALIFIED
USING /CS1 AND A19.

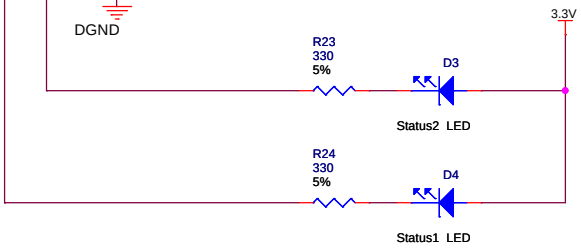


LATCH U6 IS USED AS A MEMORY MAPPED INPUT/OUTPUT
REGISTER BASED ON READS AND WRITES TO AN
ADDRESS AREA DEFINED BY /CS1 + AN OFFSET GIVEN BY
A19. THE PHYSICAL ADDRESS IS /CS1 + 0x00080000 (i.e.
/CS1 LOW AND A19 HIGH)



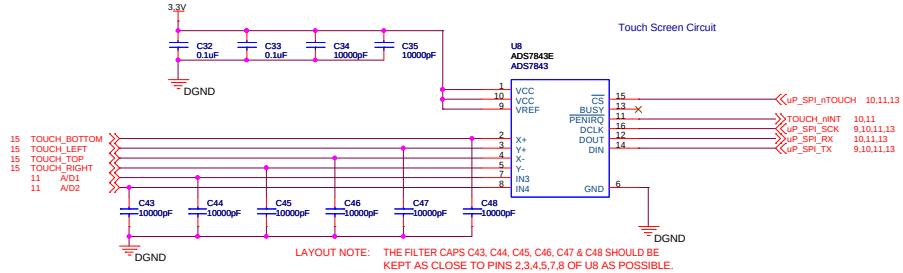
U7 CREATES AN INVERTED
A19 SIGNAL THAT, ALONG
WITH /CS1 IN U5, IS USED TO
CREATE /OE & /LE SIGNALS
FOR U6.





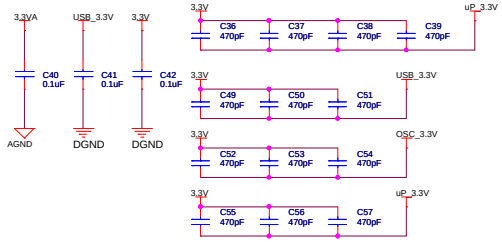
MicroController Division, TSPG, Freescale.		
Title: Logic Interface Circuits		
Size: B	Document Number: MCF5329 Validation Board	Rev: F
Date: Wednesday, March 08, 2006	Sheet 7 of 15	

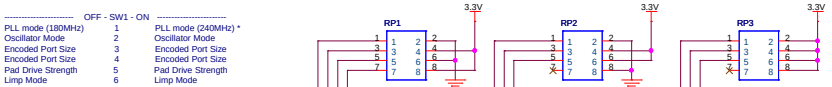
08 - PERIPHERAL CIRCUITS



LAYOUT NOTE:

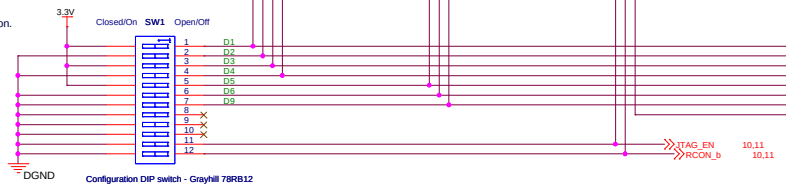
THESE CAPACITORS ARE USED FOR DECOUPLING ACROSS POWER PLANES ON THE VALIDATION BOARD AND SHOULD BE STRATEGICALLY PLACED TO MINIMIZE EMISSIONS.



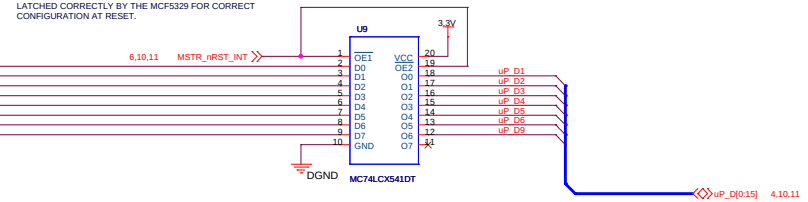


Note: default setting for SW1 is all switches closed/on.

NOTE: Please place these tables on the silkscreen on the topside of the PCB close to SW1. * = default setting.

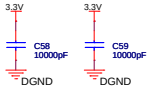


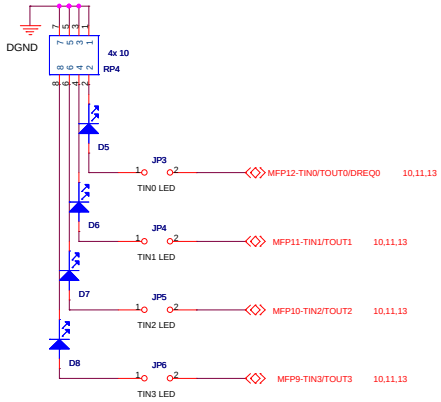
IMPORTANT NOTE: THE MSTR_nRST_INT SIGNAL MUST BE USED TO DRIVE THE OUTPUT ENABLE PINS OF U9 TO ALLOW THE D1, D2, D3, D4, D5, D6 & D9 SIGNALS TO BE LATCHED CORRECTLY BY THE MCF5329 FOR CORRECT CONFIGURATION AT RESET.



PLL Mode		Oscillator Mode		Encoded Boot Device (Port Size)			Output Pad Drive Strength	
SW1-1	Mode	SW1-2	Mode	SW1-3	SW1-4	Mode	SW1-5	Mode
OFF	180MHz/60MHz	OFF	Oscillator bypass	OFF	OFF	8-bit port	OFF	Low drive
ON	240MHz/80MHz *	ON	Crystal oscillator *	OFF	ON	32-bit port	ON	High drive *
				ON	OFF	32-bit port		
				ON	ON	16-bit port *		

Limp Mode Selection		Encoded Address/Chip Select Configuration		BDM/JTAG Enable		CPU Configuration	
SW1-6	Mode	SW1-7	Mode	SW1-11	Mode	SW1-12	Mode
OFF	Limp mode	ON	A[23:22] = A[23:22] *	OFF	JTAG	OFF	Disabled
ON	Normal PLL mode *	OFF	A[23:22] = FB_CS5_b,FB_CS4_b	ON	BDM *	ON	Enabled *





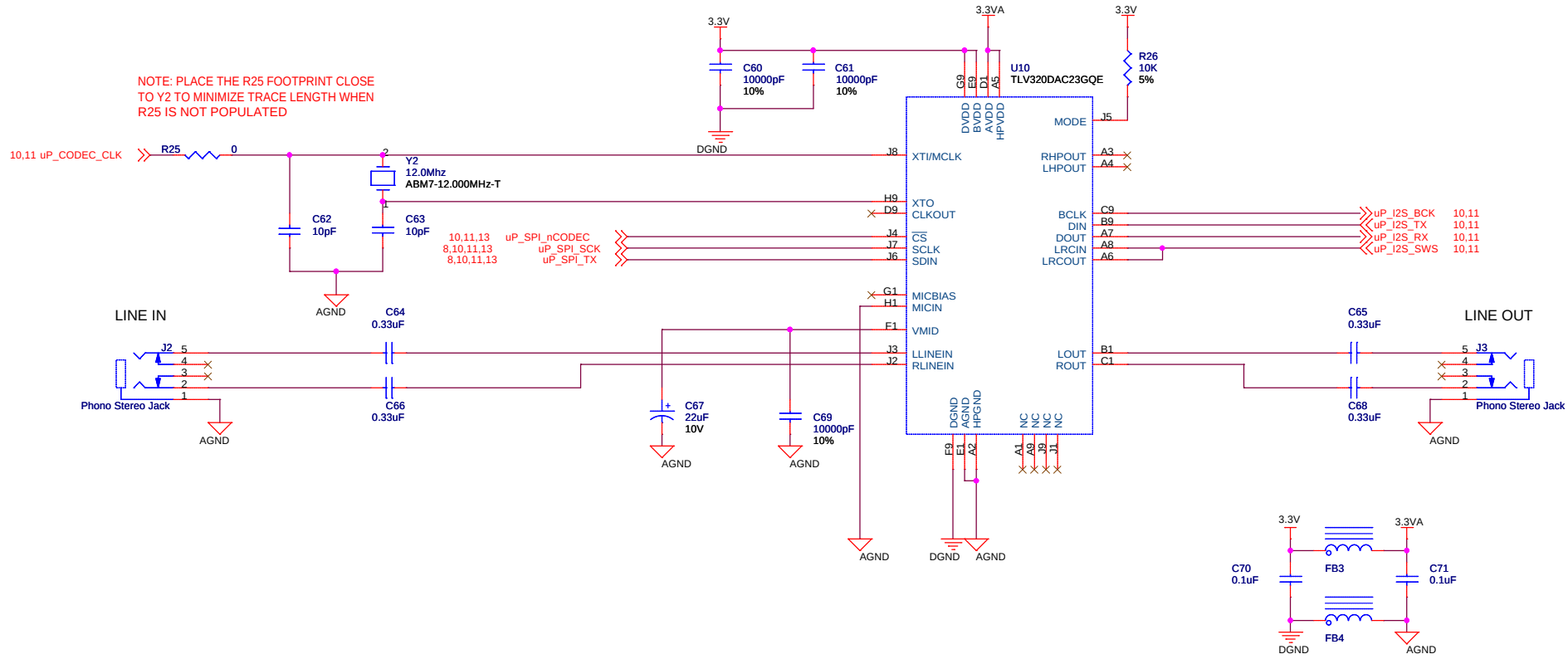
NOTE: Please place D5 through D8 together in a line.

Default setting for JP3 through JP6 is fitted.

MicroController Division, TSPG, Freescale.

Title	Peripheral Circuits	
Size C	Document Number MCF5329 Validation Board	Rev F
Date: Wednesday, March 08, 2006	Sheet 8 of 15	

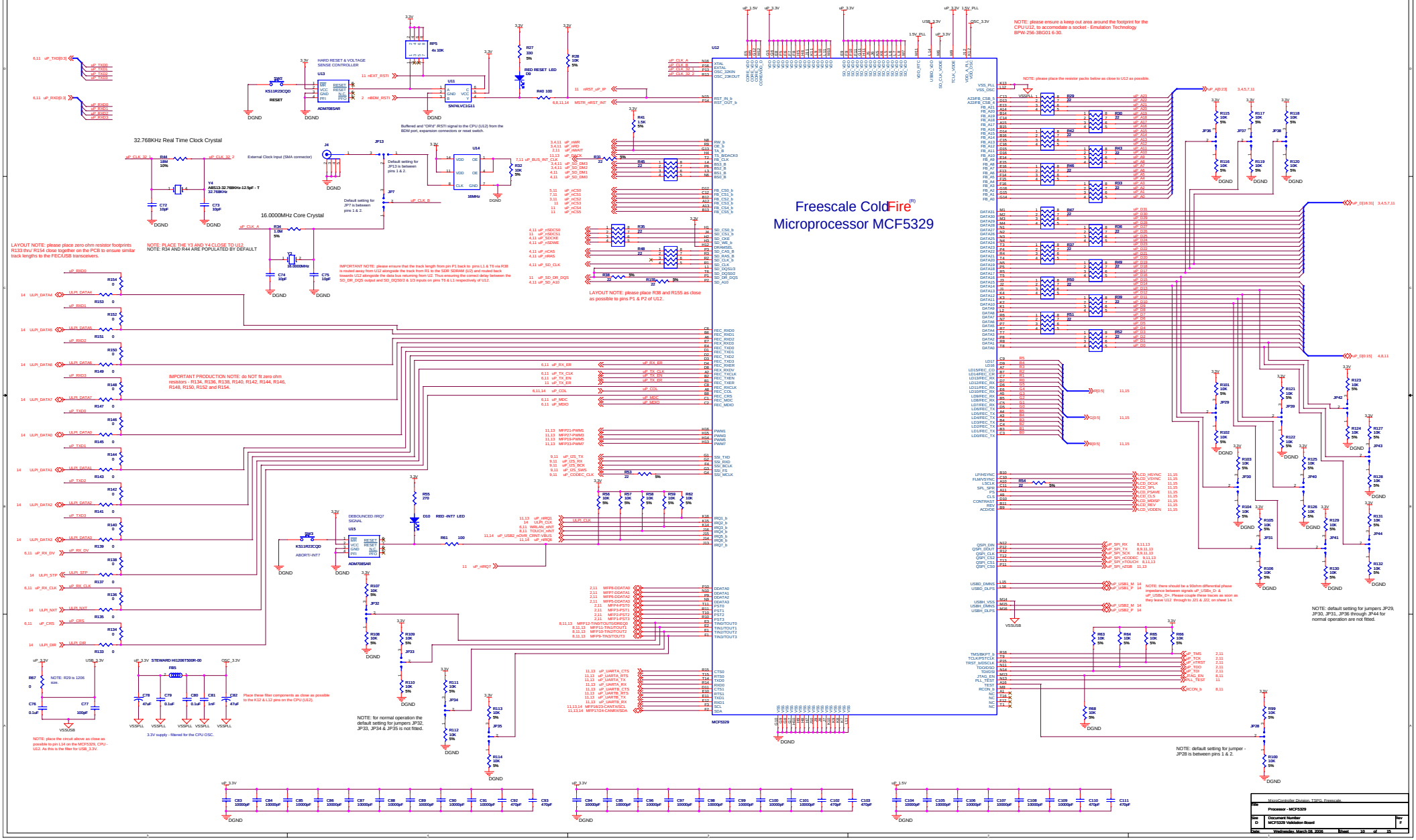
09 - CODEC



MicroController Division, TSPG, Freescale.

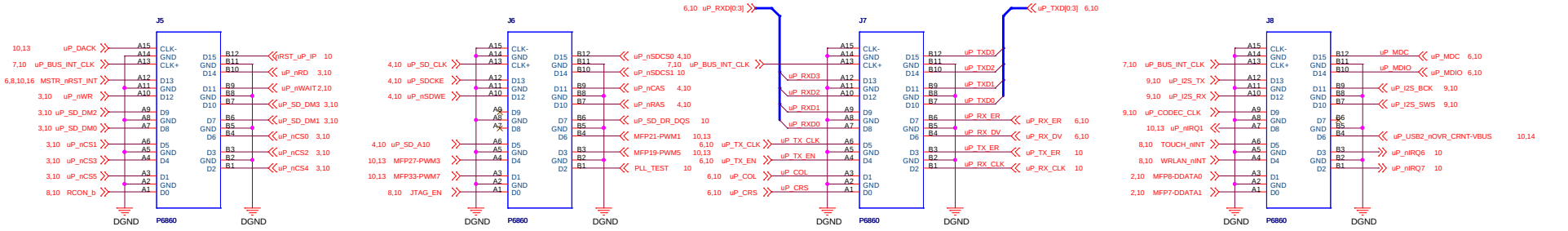
Title	Audio CODEC	
Size B	Document Number MCF5329 Validation Board	Rev F
Date: Wednesday, March 08, 2006	Sheet 9 of 15	

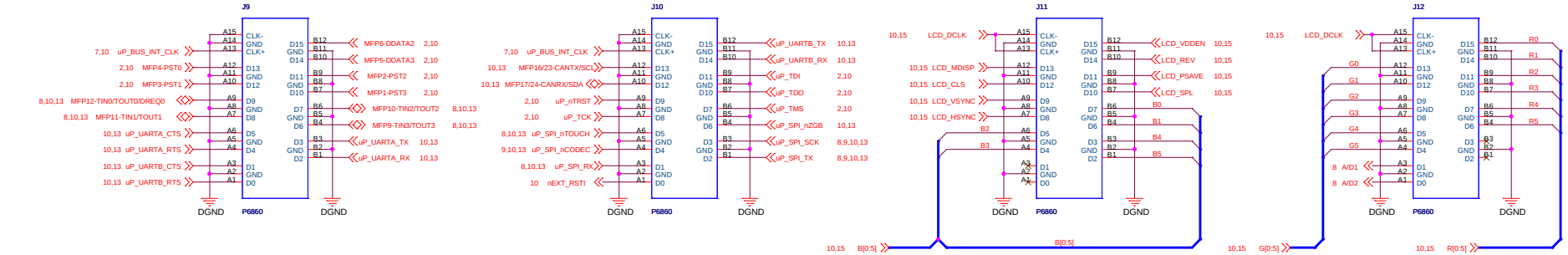
10 - PROCESSOR

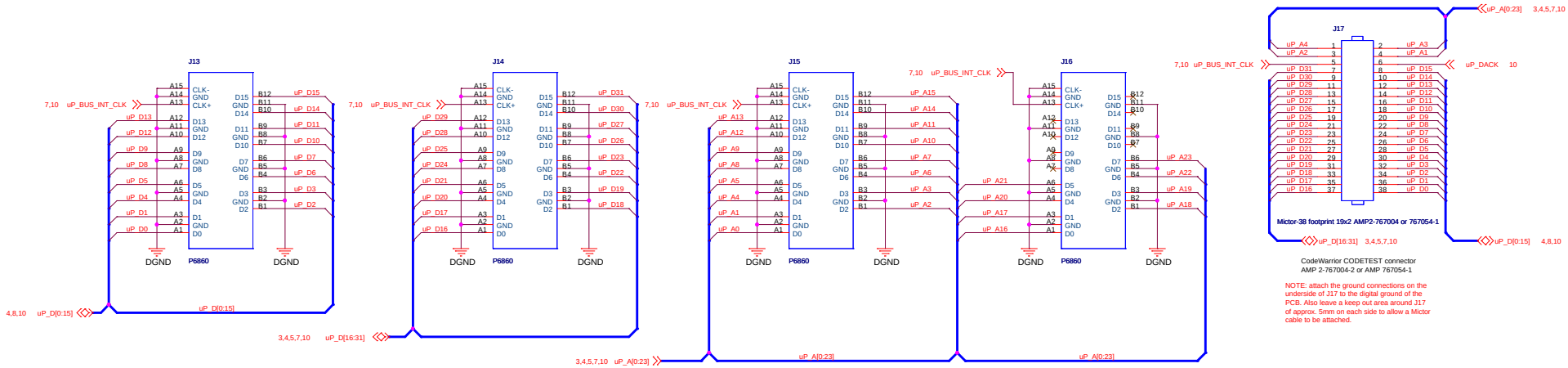


11 - HEADERS/TEST POINTS

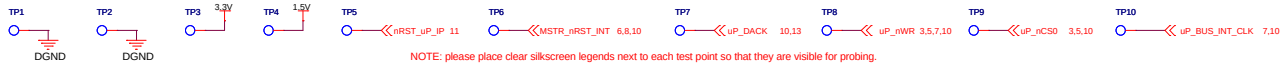
NOTE: please place the P6860 foot prints as close to the CPU (U12) as possible and through route to external devices where possible.
Connectors J5 through J16 represent Tektronix P6860 high density contactless connectors.







NOTE: please place TP1 & TP2 at opposite diagonal corners of the PCB. These TP's are to allow connections of 'scope ground leads.



NOTE: please place clear silkscreen legends next to each test point so that they are visible for probing.

MicroController Division, TSPG, Freescale.

Title	Logic Analyzer/Serial headers + Test Points	
Size C	Document Number MCF5329 Validation Board	Rev F
Date: Wednesday, March 08, 2006	Sheet 11 of 15	

12 - POWER SUPPLIES

DC voltage input range +7 to +14V & 1A min.

Power Jack Connector - 2.1mm diameter
P2
Switchcraft RAPC722
NOTE: P2 is center tap positive, please show this clearly on the silkscreen.
POWER SW SLIDE-SPST(Board Edge)
SW4
2-way Bare Wire Power Connector
P3
Augat 25V-02
J18
+12V
GND
GND
+5V
PC disk drive power connector
NOTE: the positive terminal of each power connector must be shown on the silkscreen of the PCB

C114 0.1uF
C115 1nF
F1 5A Fast blow.
D17 MBRS340T3
C116 1000uF 35V

3.3V Regulator
U16 LM2596S-3.3
VIN ~ON/OFF GND TAB VOUT FB
L1 25uH
D11 MBRS340T3
C112 330uF
C113 0.1uF
JP21 SHOULD BE INSTALLED DURING ASSEMBLY
JP21 2 PIN JUMPER
uP_3.3V
3.3V
R69 270
D12
+3.3V GREEN POWER LED

5.0V Regulator
U17 LM2596S-5
L2 25uH
D18 MBRS340T3
C117 330uF
C118 0.1uF
5V
R70 560
D19
+5V GREEN POWER LED

NOTE: Diodes prevent excessive difference between 3.3V & 1.5V rails, at power up
3.3V D13 MRA4003T3 D14 MRA4003T3 D15 MBRS340T3 1.5V

NOTE: Schottky Diode prevents excessive difference between 3.3V & 1.5V rails, at power down
3.3V D16 MBRS340T3 1.5V

1.5V Regulator
U18 LT1086CM
VIN ADJ VOUT
C119 47uF
R71 120
R72 22
C120 330uF
C121 0.1uF
JP22 SHOULD BE INSTALLED DURING ASSEMBLY
JP22 2 PIN JUMPER
uP_1.5V
1.5V

STEWARD HI1206T500R-00
FB6
1.5V
1.5V_PLL
C122 47uF
C123 0.1uF
C124 0.1uF
C125 1nF
C126 47uF
VSSPLL
1.5V supply - filtered for the CPU PLL
Place these filter components as close to J12 & K13 pins on the CPU (U12).

STEWARD HI1206T500R-00
FB7
VSSPLL
DGND
VSSPLL - filtered ground for CPU PLL module

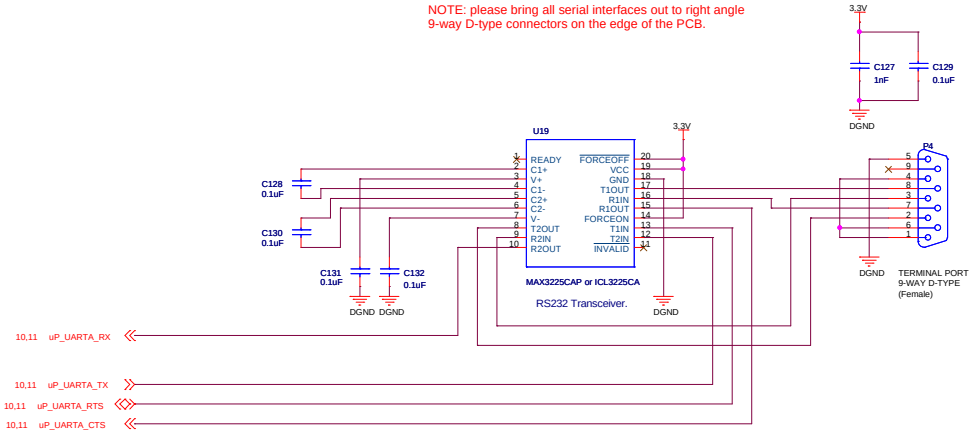
STEWARD HI1206T500R-00
FB8
VSSUSB
DGND
USBPLL - filtered ground for CPU USB module

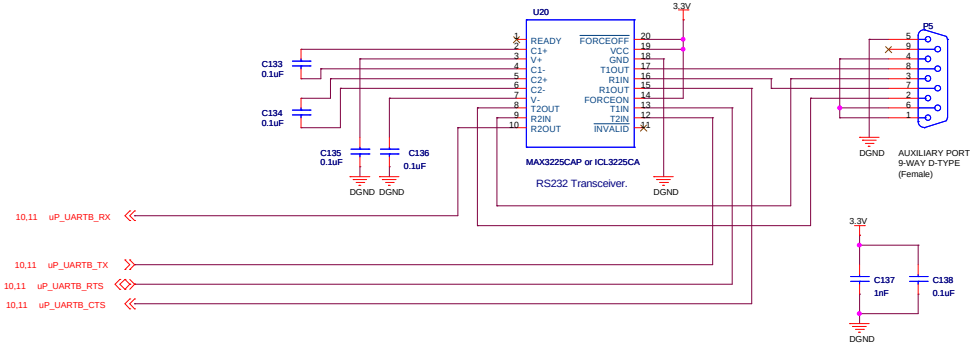
Unless otherwise specified, all resistors are 0805 body size.
All caps less than 1uF are 0805 body size and COG/NPO dielectric material.

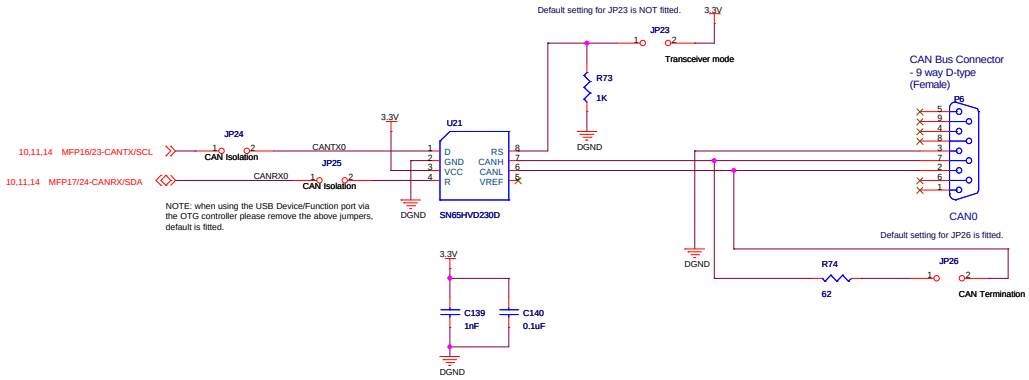
MicroController Division, TSPG, Freescale.
Title: Power Supplies
Size: B
Document Number: MCF5329 Validation Board
Rev: F
Date: Wednesday, March 08, 2006
Sheet 12 of 15

13 - SERIAL INTERFACES

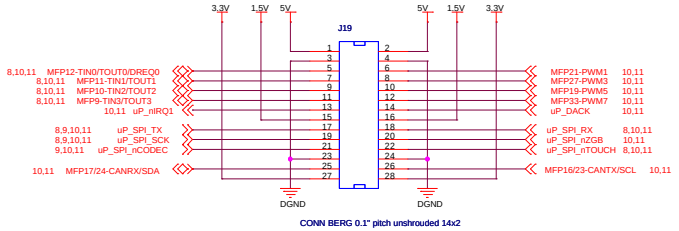
NOTE: please bring all serial interfaces out to right angle 9-way D-type connectors on the edge of the PCB.







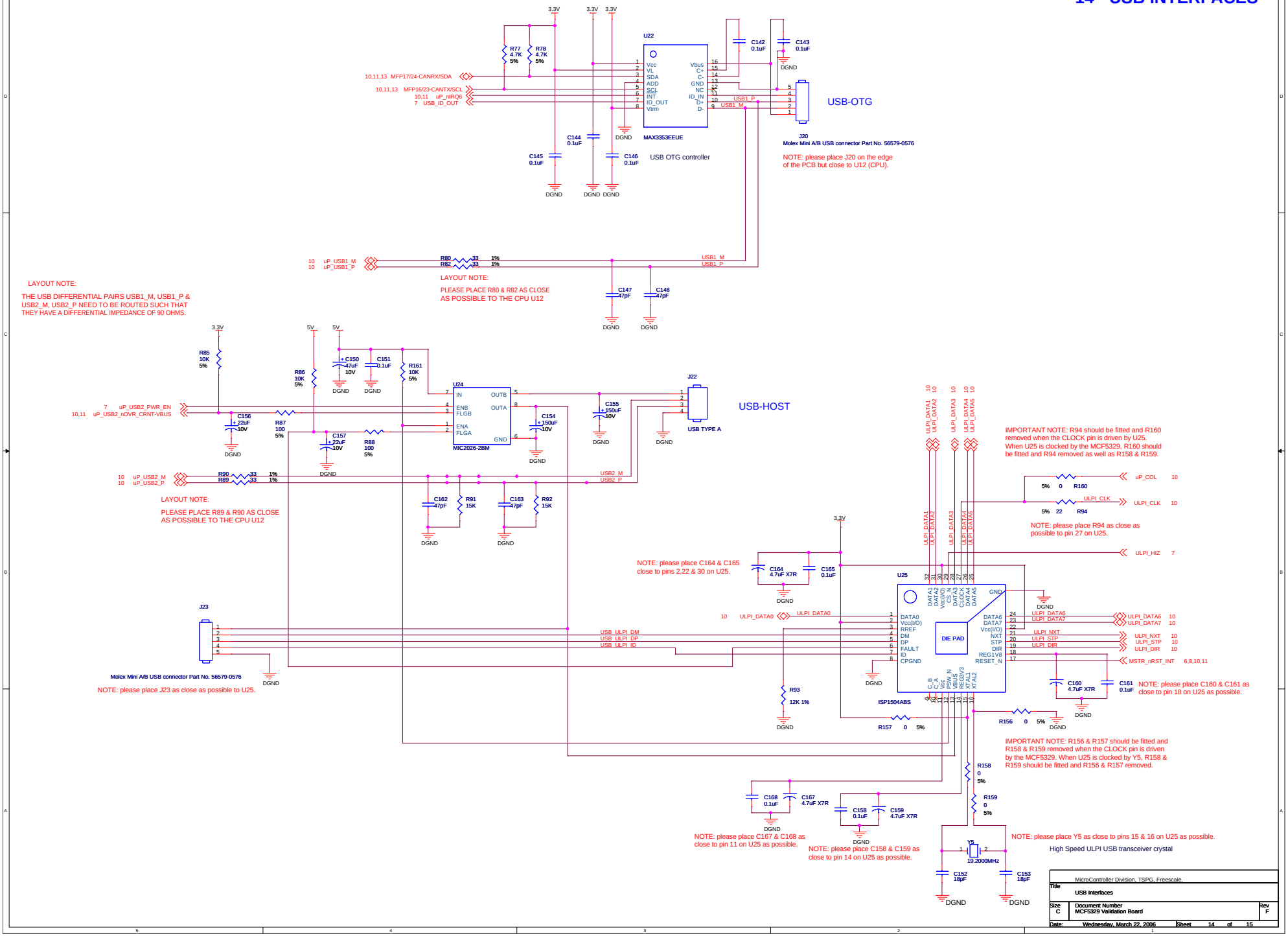
NOTE: if space allows on the PCB please put the signal names (or abbreviated version of the name) next to each relevant pin on J19.



MicroController Division, TSPG, Freescale.

Title	Serial Interfaces	
Size C	Document Number MCF5329 Validation Board	Rev F
Date: Wednesday, March 08, 2006	Sheet 13 of 15	

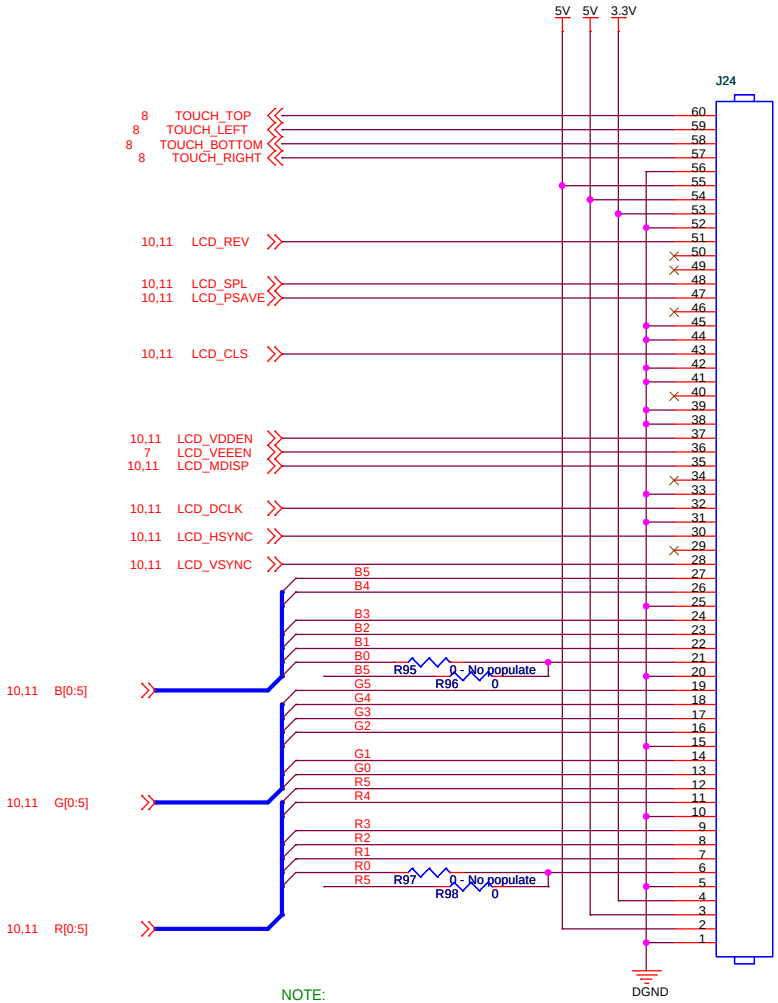
14 - USB INTERFACES



15 - VIDEO INTERFACE

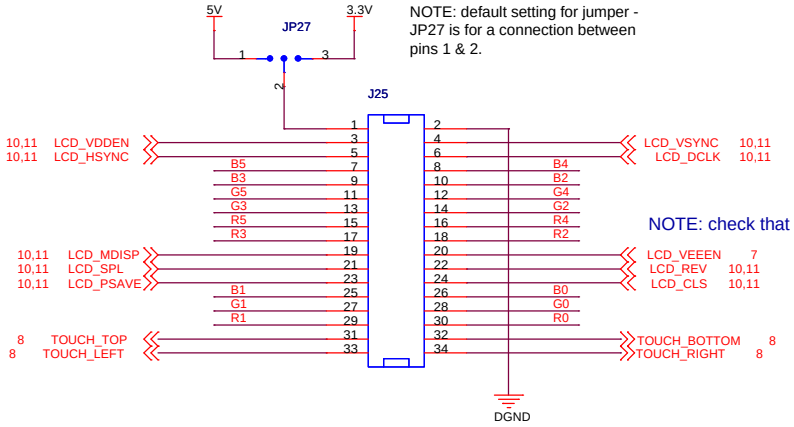
NOTE:

J24 IS ACTUALLY A 30X2 DUAL ROW .100" PITCH, .025"SQ POST MALE HEADER.
IT IS REPRESENTED SYMBOLICALLY AS A SINGLE ROW CONNECTOR TO
ILLUSTRATE HOW THE SIGNALS WILL ROUTE THROUGH THE RIBBON CABLE.



NOTE:

THE DATA SIGNALS ARE SETUP FOR A 16-BIT
TFT INTERFACE BY SELECTION OF R96 & R98
OVER R95 & R97.



NOTE: default setting for jumper - JP27 is for a connection between pins 1 & 2.

NOTE: check that LCD_VEEEN is valid for LCDON.

17x2 0.1" pitch connector for Sharp LCD's

MicroController Division, TSPG, Freescale.		
Title: LCD/Video Connector		
Size: B	Document Number: MCF5329 Validation Board	Rev: F
Date: Wednesday, March 08, 2006	Sheet 15 of 15	