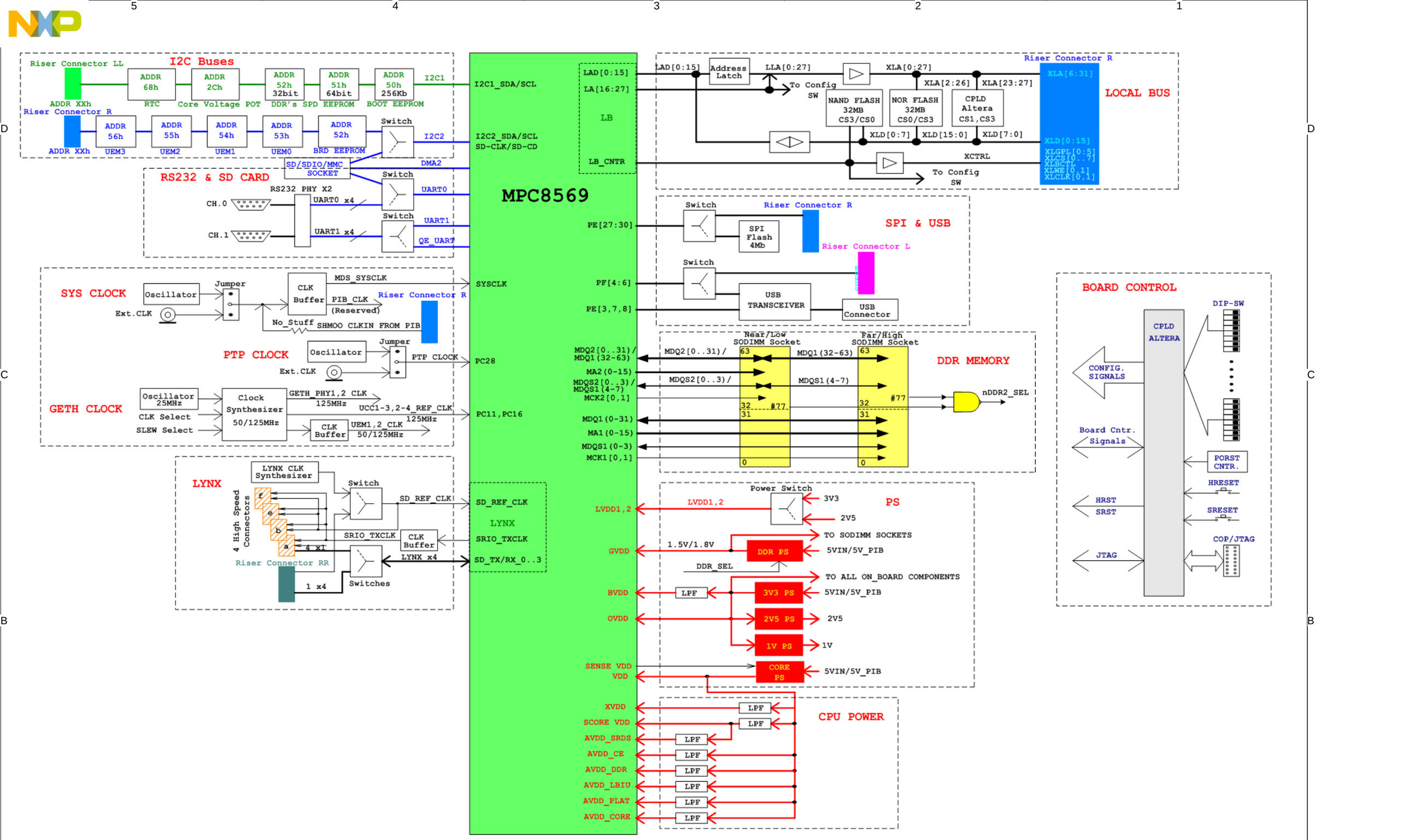


Preliminary – subject to change

MPC8569E-MDS-PB (Block Diagram)		
Size C	Document Number 084-00369-2	Rev Pilot
Date: Sunday, March 01, 2009	Sheet 1 of 21	

MPC8569E-MDS-PB

MODULAR DEVELOPMENT SYSTEM

MPC8569E Processor Board

LEGEND:

1. Do Not Place component
2. Component assembled for 8569E device Rev1 only
3. Signals/Components used for Core Issue solution only

Updates:
1. Connect U84/42 to RN1/3
2. Replace R259 for 15K (P/N:006-00697)
3. Replace R263, R276 for 100OHm (P/N:006-00626)
4. Replace R4 for 100OHm
5. Add zener: D14 P/N:048-1SMA5913BT3 in series with R4
6. Add Q8 and R687 to control USB VCC
7. Replace U38, U53, U120, U121 forNL17SZ126XV5T2G
(P/N: 051-NL17SZ126XV)
8. Change polarity of the signal nUSBVCC for USBVCC
9. Change C212, C226 for 470uF/6.3V (Agile P/N:150-75143)
10. Shift MP1, MP2 for any other free space
11. Add R688 =10K between U107/2 - U107/5 (PU) to I2C1_CLK out signal
12. Add R689-R691 (separate Cfg_60x & Cfg_Global_waitr)
13. Add PS13 signal to U86 (Altera BCSR)
14. Add SD0_EN signal from Altera U86 to U11 to separate
SD control (disconnect U14-U11 SD_EN general control
while allow SD operate with Data 0 only)
15. Add PU R693 = 10K to U45/M21 (UDE signal)
16. Add PU R692 = 10K to U45/M22 (MCP signal)
17. Disconnect XPC10 signal from U99/C5 (Riser L)
18 Add R694=0R to connect PB11 and PC10
19 Reconnect XPC23 signal from U99/C22 to U99/A1
20. Add C599, C600 10uF (VTT decoupling) near each DDR slot
21. Reconnect signal PE17 from U43/4 to U62/12
22. Reconnect signal XUPC1_TXADDR3 from U43/2 to U62/14
23. Reconnect signal XENET8_RXD1 from U43/3 to U62/13
24. Add R695-697 PD to THERM0-2 pins
25. Reconnect U4/6 form GND to new R698 (PU)
26. Change connection: USB_TN to U4/12, USB_TP to U4/11
27. Add PD 510OHm P/N:006-00629 to following pins:
U99/J10,U99/J11,U99/J15,U99/J21,U99/H27, U99/H29,U99/J24,U99/H30,U99/J16,U99/J22
28. Change R486 for 100R
29. Change R459 for 200R
30. Add optional PD R709 to TRIG_OUT signal
31. Connect TP64 to U86/A5 (LSSD_MODE) Core Issue
32. Add R710 1K PD (UART_RTS0) Core Issue
33. Connect TP66 to U86/A14 (DMA_DREQ0) Core Issue
34. Add R711 1K PU to U55/3 Core Issue
35. Add R712 1K PD to R103/1 (G4TXD2) Core Issue
36. Add R713 1K PD to U55/2 (G4TXD1) Core Issue
37. Connect U97/E7 to U86/F4 (nIRQ4) Core Issue
38. Connect TP45 to U86/D1 (DMA_DACK2_CI) Core Issue
39. Add R714 0R to disable IRQ4 toggle (Core Issue)
40. Add R715 1K to U55/9 (PB16 PD) Core Issue
41. Add R716 1K in serial to DMA_DACK2_CI to isolate SD card operation (Core Issue)
42. Add optional R717-R722 PU 1K (RMII6 issue)
43. Replace R449 for 0R (to provide BootWiz power)
44. Replace R103, R104, R137, R157, R158 for 0R (UCC4 TXD signals amplification)
45. Change R7,R16,R17,R23 and R24 for 0R (UCC4 RXD signals amplification)
46. Add R723, R724 = 10K (PU's on MDIO signal)
47. Provide metallization on heatsink holes and slide traces on CS (Pad D should be >=6mm)
48. Add resistor R725 = 1K to split signal UART_SOUT0 and UART_SOUT0_CFG (SD card stability)
49. Add vias to following pins:
U100 - A28, C28, D26, E3, E5, J13.
U99 - A1, A3, A5, A7, A13, A22, A28, A30, C10, C28, C30, D8, E1, G5.
U97 - A28, A30, C30.
50. Replace R92, R95, R96, R100, R101, R102, R115, R441, R442 and R461 for 0R
(UCC3 TXD/RXD signals amplification)
51. Replace R48, 49, 52, 63-66, 70, 75-78,81-84,98,99,
113,132-134,151,152,154-156,171-174 and R402 for 0R
(To improve operation with PIB mounted ETh PHY's)

Plastic Parts:
- 042-00016, NYLON METRICS SCREW 6.4mm M3 LF 3pieces
- 042-00018, HEX NUT M3 3pieces
- 042-00064, SPACER FEM/MALE THREADED 7mm LF 4pieces
- 042-00060, NYLON METRIC SPACER 8mm LF 4pieces
- 042-00073, HEXAGONAL STANDOFF 5mm LF 3pieces

Preliminary – subject to change

freescale semiconductor

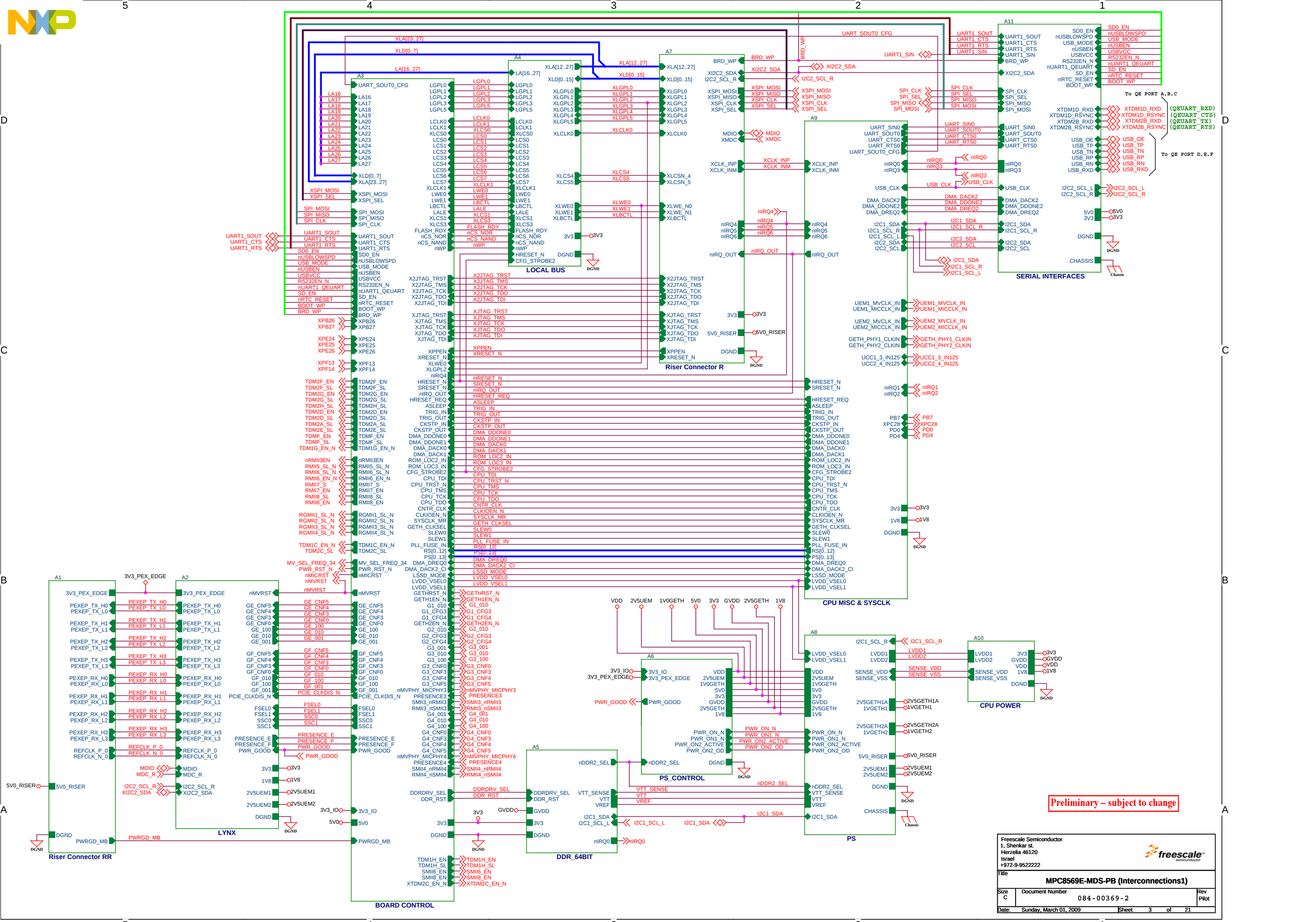
ICAP Classification: FCP: ___ FIUO: X PUBI: ___

Drawing Title: **Cover Page**

Page Title: **MPC8569E-MDS-PB**

Size	Document Number	Rev
C	084-00369-2	Pilot

Date: Wednesday, March 04, 2009 Sheet 2 of 21


A1
Riser Connector RR
A2
LYNX
A3
LOCAL BUS
A4
BOARD CONTROL
A5
DDR_64BIT
A6
PS_CONTROL
A7
Riser Connector R
A8
PS
A9
CPU MISC & SYSCLK
A10
CPU POWER
A11
SERIAL INTERFACES
Preliminary – subject to change
Freescale Semiconductor
1, Shenkar st.
Herzelia 46120
Israel
+972-9-9522222
MPC8569E-MDS-PB (Interconnections1)
Size C
Document Number 084-00369-2
Rev Pilot
Date: Sunday, March 01, 2009
Sheet 3 of 21

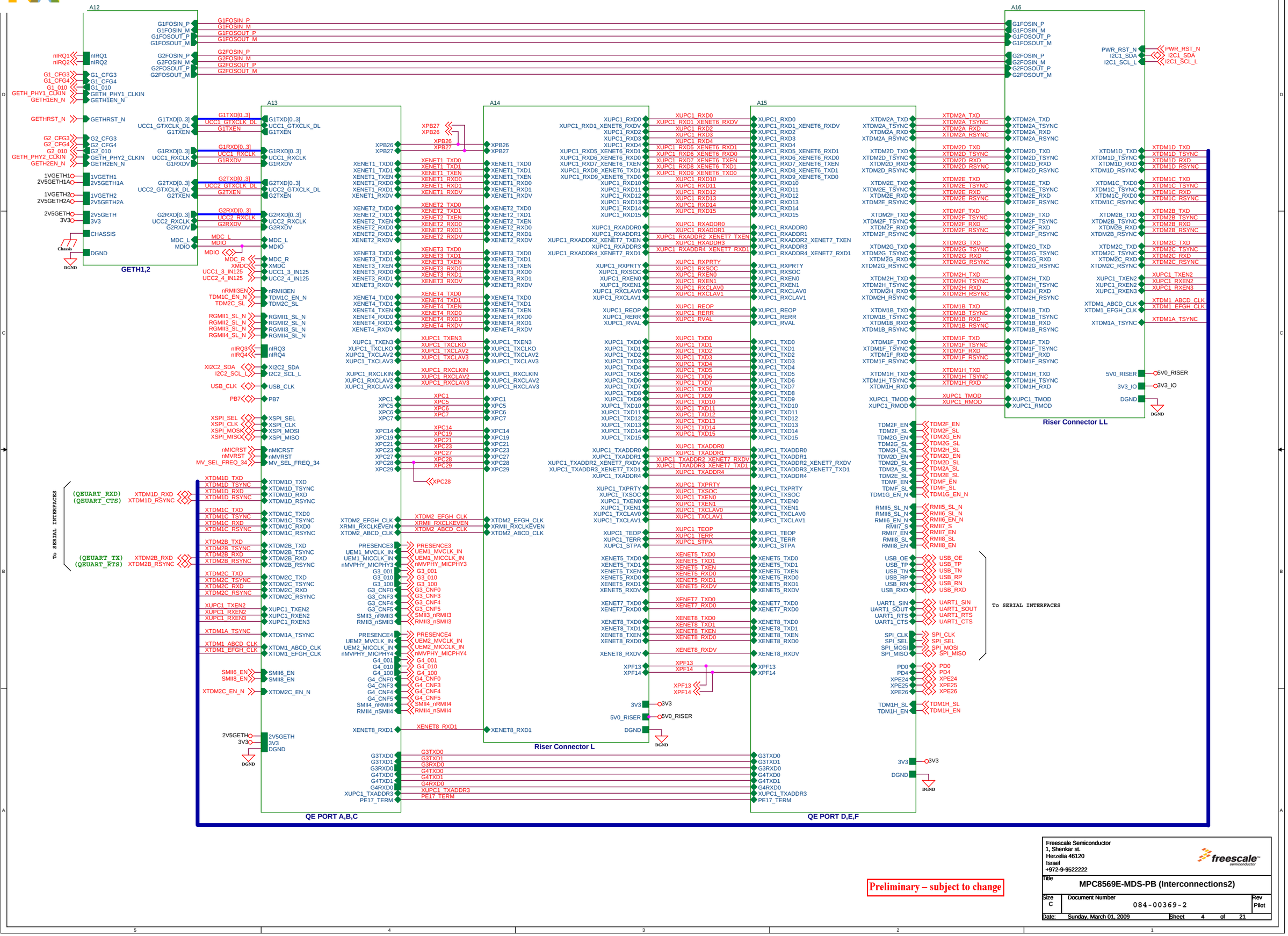

A12
GETH1,2
A13
QE PORT A,B,C
A14
Riser Connector L
A15
QE PORT D,E,F
A16
Riser Connector LL
To SERIAL INTERFACES
(QEUART_RXD)
(QEUART_CTS)
(QEUART_TX)
(QEUART_RTS)
To SERIAL INTERFACES
Preliminary – subject to change
Freescale Semiconductor
1, Shenkar st.
Herzelia 46120
Israel
+972-9-9522222
Title
MPC8569E-MDS-PB (Interconnections2)
Size C
Document Number 084-00369-2
Rev Pilot
Date: Sunday, March 01, 2009
Sheet 4 of 21

TABLE OF CONTENTS

PAGE	NAME
1	BLOCK DIAGRAM
2	COVER PAGE
3	INTERCONNECTIONS 1
4	INTERCONNECTIONS 2
5	TABLE OF CONTENTS
6	BOARD CONTROL
7	CPU MISC & SYSCLK
8	CPU POWER
9	DDR 64BIT
10	GETH 1,2
11	LOCAL BUS
12	LYNX
13	PS
14	PS CONTROL
15	QE PORT A,B,C
16	QE PORT D,E,F
17	RISER CONNECTOR L
18	RISER CONNECTOR LL
19	RISER CONNECTOR R
20	RISER CONNECTOR RR
21	SERIAL INTERFACE

Preliminary – subject to change

freescale semiconductor

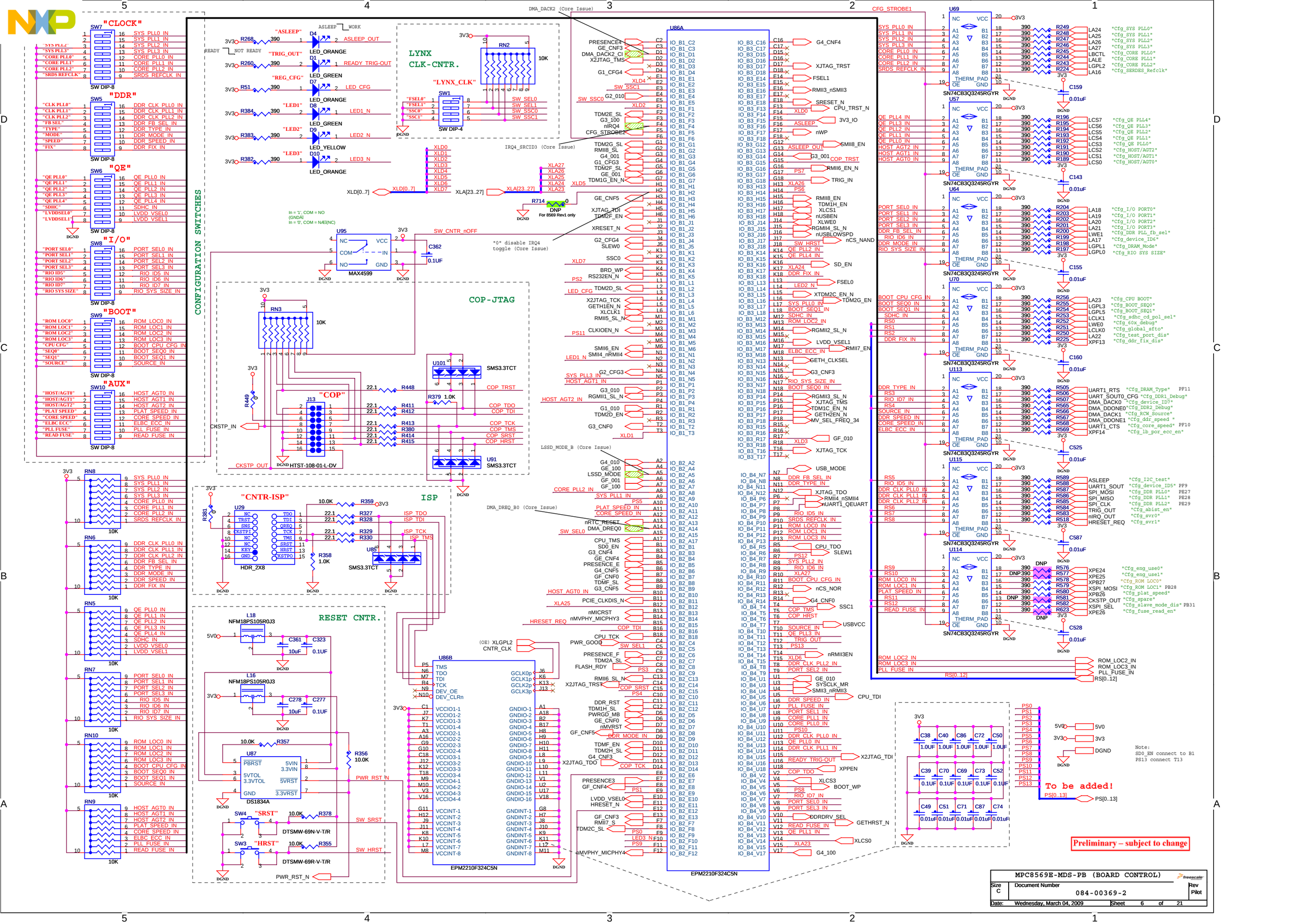
ICAP Classification: FCP: ___ FIUO: X PUBI: ___

Drawing Title: **Table of Contents**

Page Title: **MPC8569E-MDS-PB**

Size	Document Number	Rev
C	084-00369-2	Pilot

Date: Sunday, March 01, 2009 Sheet 5 of 21


"CLOCK"
SW7
SYS_PLL0_IN
SYS_PLL1_IN
SYS_PLL2_IN
SYS_PLL3_IN
CORE_PLL0_IN
CORE_PLL1_IN
CORE_PLL2_IN
SRDS_REFCLK_IN
"DDR"
SW5
DDR_CLK_PLL0_IN
DDR_CLK_PLL1_IN
DDR_CLK_PLL2_IN
DDR_FB_SEL_IN
DDR_TYPE_IN
DDR_MODE_IN
DDR_SPEED_IN
DDR_FIX_IN
"QE"
SW6
QE_PLL0_IN
QE_PLL1_IN
QE_PLL2_IN
QE_PLL3_IN
QE_PLL4_IN
SDHC_IN
LVDD_VSEL0
LVDD_VSEL1
"I/O"
SW8
PORT_SEL0_IN
PORT_SEL1_IN
PORT_SEL2_IN
PORT_SEL3_IN
RIO_ID5_IN
RIO_ID6_IN
RIO_ID7_IN
RIO_SYS_SIZE_IN
"BOOT"
SW9
ROM_LOC0_IN
ROM_LOC1_IN
ROM_LOC2_IN
ROM_LOC3_IN
BOOT_CPU_CFG_IN
BOOT_SEQ0_IN
BOOT_SEQ1_IN
SOURCE_IN
"AUX"
SW10
HOST_AGT0_IN
HOST_AGT1_IN
HOST_AGT2_IN
PLAT_SPEED_IN
CORE_SPEED_IN
ELBC_ECC_IN
PLL_FUSE_IN
READ_FUSE_IN
SW DIP-8
CONFIGURATION SWITCHES
"ASLEEP"
"TRIG_OUT"
"REG_CFG"
"LED1"
"LED2"
"LED3"
R268
R260
R51
R384
R383
R382
390
D4
D1
D7
D8
D9
D10
LED_ORANGE
LED_GREEN
LED_YELLOW
ASLEEP
WORK
READY
NOT READY
ASLEEP_OUT
READY_TRIG-OUT
LED_CFG
LED1_N
LED2_N
LED3_N
LYNX
CLK-CNTR.
"LYNX_CLK"
SW1
SW DIP-4
"FSEL0"
"FSEL1"
"SSC0"
"SSC1"
SW_SEL0
SW_SEL1
SW_SSC0
SW_SSC1
RN2
10K
XLD[0..7]
XLA[23..27]
R714
DNP
For 8569 Rev1 only
In = '1', COM = NO
(GNDA)
In = '0', COM = N/A(NC)
U95
MAX4599
SW_CNTR_nOFF
C362
0.1UF
"0" disable IRQ4
toggle (Core Issue)
COP-JTAG
RN3
U101
SMS3.3TCT
U91
SMS3.3TCT
"COP"
J13
HTST-108-01-L-DV
R448
R379
1.0K
R411
R412
R413
R380
R414
R415
COP_TRST
COP_TDO
COP_TDI
COP_TCK
COP_TMS
COP_SRST
COP_HRST
R449
CKSTP_IN
CKSTP_OUT
"CNTR-ISP"
ISP
U29
HDR_2X8
R359
R327
R328
R329
R330
R358
R381
ISP_TDO
ISP_TDI
ISP_TCK
ISP_TMS
U85
SMS3.3TCT
RESET CNTR.
L18
NFM18PS105R0J3
L16
NFM18PS105R0J3
C361
C323
10uF
0.1UF
C278
C277
R357
R356
U87
DS1834A
PWR_RST_IN
SW4
"SRST"
SW3
"HRST"
R378
R355
DTSMW-69N-V-T/R
DTSMW-69R-V-T/R
SW_SRST
SW_HRST
PWR_RST_N
U86A
U86B
EPM2210F324C5N
IO_B1_C2
IO_B1_C3
IO_B1_D1
IO_B1_D2
IO_B1_D3
IO_B1_D4
IO_B1_E1
IO_B1_E2
IO_B1_E3
IO_B1_E4
IO_B1_E5
IO_B1_F1
IO_B1_F2
IO_B1_F3
IO_B1_F4
IO_B1_F5
IO_B1_F6
IO_B1_G1
IO_B1_G2
IO_B1_G3
IO_B1_G4
IO_B1_G5
IO_B1_G6
IO_B1_G7
IO_B1_H1
IO_B1_H2
IO_B1_H3
IO_B1_H4
IO_B1_H5
IO_B1_H6
IO_B1_J1
IO_B1_J2
IO_B1_J3
IO_B1_J4
IO_B1_J5
IO_B1_K1
IO_B1_K2
IO_B1_K3
IO_B1_K4
IO_B1_K5
IO_B1_L1
IO_B1_L2
IO_B1_L3
IO_B1_L4
IO_B1_L5
IO_B1_L6
IO_B1_M1
IO_B1_M2
IO_B1_M3
IO_B1_M4
IO_B1_M5
IO_B1_M6
IO_B1_N1
IO_B1_N2
IO_B1_N3
IO_B1_N4
IO_B1_N5
IO_B1_P1
IO_B1_P2
IO_B1_P3
IO_B1_P4
IO_B1_R1
IO_B1_R2
IO_B1_R3
IO_B1_T2
IO_B1_T3
IO_B2_A2
IO_B2_A4
IO_B2_A5
IO_B2_A6
IO_B2_A7
IO_B2_A8
IO_B2_A9
IO_B2_A10
IO_B2_A11
IO_B2_A12
IO_B2_A13
IO_B2_A14
IO_B2_A15
IO_B2_A17
IO_B2_B1
IO_B2_B3
IO_B2_B4
IO_B2_B5
IO_B2_B6
IO_B2_B7
IO_B2_B8
IO_B2_B9
IO_B2_B10
IO_B2_B11
IO_B2_B12
IO_B2_B13
IO_B2_B14
IO_B2_B15
IO_B2_B16
IO_B2_B18
IO_B2_C4
IO_B2_C5
IO_B2_C6
IO_B2_C7
IO_B2_C8
IO_B2_C9
IO_B2_C13
IO_B2_C14
IO_B2_C15
IO_B2_C10
IO_B2_C11
IO_B2_C12
IO_B2_D5
IO_B2_D6
IO_B2_D7
IO_B2_D8
IO_B2_D9
IO_B2_D10
IO_B2_D11
IO_B2_D12
IO_B2_D13
IO_B2_D14
IO_B2_E6
IO_B2_E7
IO_B2_E8
IO_B2_E9
IO_B2_E10
IO_B2_E11
IO_B2_E12
IO_B2_E13
IO_B2_F7
IO_B2_F8
IO_B2_F9
IO_B2_F10
IO_B2_F11
IO_B2_F12
PRESENCE4
GE_CNF3
DMA_DACK2_CI
X2JTAG_TMS
G1_CFG4
XLD4
SW_SSC1
G2_010
XLD2
TDM2E_SL
G3_100
nIRQ4
CFG_STROBE2
TDM2G_SL
RMII8_SL
G4_001
G1_CFG3
TDM2F_SL
GE_001
TDM1G_EN_N
XLD5
GE_CNF5
XJTAG_TDI
TDM2F_EN
XRESET_N
G2_CFG4
SLEW0
SSC0
XLD7
BRD_WP
RS232EN_N
PS2
TDM2D_SL
LED_CFG
X2JTAG_TCK
GETH1EN_N
XLCLK1
RMII5_SL_N
CLKIOEN_N
PS11
SMII6_EN
SMII4_nRMII4
LED1_N
G2_CFG3
SYS_PLL3_IN
HOST_AGT1_IN
G3_010
RGMII1_SL_N
HOST_AGT2_IN
G1_010
TDM2D_EN
G3_CNF0
XLD1
LSSD_MODE_B (Core Issue)
G4_010
GE_100
LSSD_MODE
GF_001
GF_100
CORE_PLL2_IN
SYS_PLL1_IN
PS5
PLAT_SPEED_IN
CORE_SPEED_IN
DMA_DREQ_B0 (Core Issue)
nRTC_RESET
DMA_DREQ0
SW_SEL0
CPU_TMS
SD0_EN
G3_CNF4
GE_CNF4
PRESENCE_E
G4_CNF5
GF_CNF0
TDMF_SL
G3_CNF5
HOST_AGT0_IN
PCIE_CLKDIS_N
XLA25
nMICRST
nMVPHY_MICPHY3
HRESET_REQ
COP_TDI
CPU_TCK
PWR_GOOD
SW_SEL1
PRESENCE_F
TDM2A_SL
FLASH_RDY
PS3
RMII6_SL_N
X2JTAG_TRST
COP_SRST
PS4
DDR_RST
TDM1H_SL
PWRGD_MB
GE_CNF0
nMVRST
GF_CNF5
DDR_MODE_IN
TDMF_EN
TDM2H_SL
G4_CNF3
X2JTAG_TDO
COP_TCK
PRESENCE3
GF_CNF4
PS1
LVDD_VSEL0
HRESET_N
GF_CNF3
RMII7_S
TDM2C_SL
PS0
LED3_N
PS9
nMVPHY_MICPHY4
IRQ4_SRCID3 (Core Issue)
DMA_DACK2 (Core Issue)
CFG_STROBE1
XLA27
XLA26
XLA25
XLA24
XLA23
G4_CNF4
XJTAG_TRST
FSEL1
RMII3_nSMII3
SRESET_N
CPU_TRST_N
XLD0
3V3_IO
ASLEEP
nWP
SMII8_EN
ASLEEP_OUT
G3_001
COP_TRST
RMII6_EN_N
PS7
TRIG_IN
TRIG_OUT
XLA26
PS6
RMII8_EN
TDM1H_EN
XLCS1
nUSBEN
XLWE0
RGMII4_SL_N
nUSBLOWSPD
nCS_NAND
SW_HRST
QE_PLL2_IN
QE_PLL4_IN
SD_EN
XLA24
DDR_FIX_IN
FSEL0
LED2_N
XTDM2C_EN_N
TDM2G_EN
SYS_PLL0_IN
BOOT_SEQ1_IN
SDHC_IN
ROM_LOC2_IN
RGMII2_SL_N
LVDD_VSEL1
RMII7_EN
ELBC_ECC_IN
GETH_CLKSEL
RIO_SYS_SIZE_IN
G3_CNF3
BOOT_SEQ0_IN
RGMII3_SL_N
XJTAG_TMS
TDM1C_EN_N
GETH2EN_N
MV_SEL_FREQ_34
GF_010
XLD3
XJTAG_TCK
USB_MODE
DDR_FB_SEL_IN
DDR_TYPE_IN
XJTAG_TDO
RMII4_nSMII4
nUART1_QEUART
RIO_ID5_IN
SRDS_REFCLK_IN
ROM_LOC0_IN
ROM_LOC1_IN
ROM_LOC3_IN
CPU_TDO
SLEW1
PS12
SYS_PLL2_IN
RIO_ID6_IN
XLA27
BOOT_CPU_CFG_IN
nCS_NOR
G4_CNF0
SSC1
COP_TMS
COP_HRST
USBVCC
SOURCE_IN
QE_PLL3_IN
TRIG_OUT
PS13
XLD6
nRMII3EN
DDR_CLK_PLL2_IN
PORT_SEL2_IN
GE_010
SYSCLK_MR
SMII3_nRMII3
CPU_TDI
DDR_SPEED_IN
PLL_FUSE_IN
PORT_SEL1_IN
CORE_PLL1_IN
CORE_PLL0_IN
PS10
DDR_CLK_PLL0_IN
QE_PLL0_IN
DDR_CLK_PLL1_IN
X2JTAG_TDI
READY_TRIG-OUT
XPPEN
COP_TDO
XLCS3
BOOT_WP
PS8
RIO_ID7_IN
PORT_SEL0_IN
PORT_SEL3_IN
DDRDRV_SEL
GETHRST_N
QE_PLL1_IN
XLCS0
XLA23
G4_100
U69
U57
U64
U70
U113
U115
U114
SN74CB3Q3245RGYR
THERM_PAD
OE
GND
3V3
DGND
0.01uF
C159
C143
C155
C160
C525
C587
C528
SYS_PLL0_IN
SYS_PLL1_IN
SYS_PLL2_IN
SYS_PLL3_IN
CORE_PLL0_IN
CORE_PLL1_IN
CORE_PLL2_IN
SRDS_REFCLK_IN
QE_PLL4_IN
QE_PLL3_IN
QE_PLL2_IN
QE_PLL1_IN
QE_PLL0_IN
HOST_AGT2_IN
HOST_AGT1_IN
HOST_AGT0_IN
PORT_SEL0_IN
PORT_SEL1_IN
PORT_SEL2_IN
PORT_SEL3_IN
DDR_FB_SEL_IN
DDR_MODE_IN
RIO_ID6_IN
RIO_SYS_SIZE_IN
BOOT_CPU_CFG_IN
BOOT_SEQ0_IN
BOOT_SEQ1_IN
SDHC_IN
RS0
RS1
RS2
DDR_FIX_IN
DDR_TYPE_IN
RS3
RIO_ID7_IN
RS4
SOURCE_IN
DDR_SPEED_IN
CORE_SPEED_IN
ELBC_ECC_IN
RS5
RIO_ID5_IN
DDR_CLK_PLL0_IN
DDR_CLK_PLL1_IN
DDR_CLK_PLL2_IN
RS6
RS7
RS8
RS9
RS10
ROM_LOC0_IN
ROM_LOC1_IN
PLAT_SPEED_IN
RS11
RS12
READ_FUSE_IN
ROM_LOC2_IN
ROM_LOC3_IN
PLL_FUSE_IN
RS[0..12]
R249
R248
R247
R246
R245
R244
R243
R224
R196
R195
R194
R193
R192
R191
R190
R189
R204
R203
R202
R201
R200
R199
R198
R197
R256
R255
R254
R253
R252
R251
R250
R225
R505
R506
R507
R565
R566
R567
R568
R569
R589
R588
R587
R586
R585
R584
R583
R518
R576
R577
R578
R579
R580
R581
R582
R623
LA24
LA25
LA26
LA27
LA16
LA18
LA19
LA20
LA21
LWE1
LA17
LGPL1
LGPL0
LA23
LGPL3
LGPL5
LCLK1
LWE0
LCLK0
LA22
XPF13
UART1_RTS
UART_SOUT0_CFG
DMA_DACK0
DMA_DDONE0
DMA_DACK1
DMA_DDONE1
UART1_CTS
XPF14
ASLEEP
UART1_SOUT
SPI_MOSI
SPI_MISO
SPI_CLK
TRIG_OUT
nIRQ_OUT
HRESET_REQ
XPE24
XPE25
XPB27
XSPI_MOSI
XPB26
CKSTP_OUT
XSPI_SEL
XPE26
LCS7
LCS6
LCS5
LCS4
LCS3
LCS2
LCS1
LCS0
"Cfg_SYS PLL0"
"Cfg_SYS PLL1"
"Cfg_SYS PLL2"
"Cfg_SYS PLL3"
"Cfg_CORE PLL0"
"Cfg_CORE PLL1"
"Cfg_CORE PLL2"
"Cfg_SERDES_Refclk"
"Cfg_QE PLL4"
"Cfg_QE PLL3"
"Cfg_QE PLL2"
"Cfg_QE PLL1"
"Cfg_QE PLL0"
"Cfg_HOST/AGT2"
"Cfg_HOST/AGT1"
"Cfg_HOST/AGT0"
"Cfg_I/O PORT0"
"Cfg_I/O PORT1"
"Cfg_I/O PORT2"
"Cfg_I/O PORT3"
"Cfg_DDR PLL_fb_sel"
"Cfg_device_ID6"
"Cfg_DRAM_Mode"
"Cfg_RIO SYS SIZE"
"Cfg_CPU BOOT"
"Cfg_BOOT_SEQ0"
"Cfg_BOOT_SEQ1"
"Cfg_sdhc_cd_pol_sel"
"Cfg_60x_debug"
"Cfg_global_sfto"
"Cfg_test_port_dis"
"Cfg_ddr_fix_dis"
"Cfg_DRAM_Type"
"Cfg_device_ID5"
"Cfg_DDR1_Debug"
"Cfg_device_ID7"
"Cfg_DDR2_Debug"
"Cfg_RCW_Source"
"Cfg_ddr_speed "
"Cfg_core_speed"
"Cfg_I2C_test"
"Cfg_device_ID5"
"Cfg_DDR PLL0"
"Cfg_DDR PLL1"
"Cfg_DDR PLL2"
"Cfg_dabist_en"
"Cfg_svr0"
"Cfg_svr1"
"Cfg_eng_use0"
"Cfg_eng_use1"
"Cfg_ROM LOC0"
"Cfg_ROM LOC1"
"Cfg_plat_speed"
"Cfg_spare"
"Cfg_slave_mode_dis"
"Cfg_fuse_read_en"
PF9
PE27
PE28
PE29
PB28
PB31
PF10
PF11
PF12
PF13
PS0
PS1
PS2
PS3
PS4
PS5
PS6
PS7
PS8
PS9
PS10
PS11
PS12
PS13
PS[0..13]
To be added!
Note:
SD0_EN connect to B1
PS13 connect T13
Preliminary – subject to change
MPC8569E-MDS-PB (BOARD CONTROL)
Size C
Document Number 084-00369-2
Rev Pilot
Date: Wednesday, March 04, 2009
Sheet 6 of 21

CPU MISC

MISC

U45D — 8569

IRQ[0] IRQ[1] IRQ[2] IRQ[3] IRQ[4]_SRCID3 IRQ[5]_SRCID4 IRQ[6]_DVAL — IRQ_OUT_B

CKSTP_IN_B — CKSTP_OUT_B

BVDD_VSEL0 BVDD_VSEL1

MCP — MCP_B

UDE — UDE_B

LSSD_MODE_B

DMA_DREQ_B[0] DMA_DACK_B[0] DMA_DDONE_B[0]

DMA_DREQ_B[1]_SRCID0 DMA_DACK_B[1]_SRCID1 DMA_DDONE_B[1]_SRCID2

DMA_DREQ_B[2]_SD-DAT0 DMA_DACK_B[2]_SD-CMD DMA_DDONE_B[2]_SD-WP

UART_SIN[0]/DMA_DACK_[B3]_SD_DAT2 UART_SOUT[0]/DMA_DREQ_[B3]_SD_DAT1 UART_CTS_B[0]/DMA_DDONE_[B3]_SD_DAT3 UART_RTS_B[0]

SYSCLK THERM0 THERM1 THERM2 TRIG_IN TRIG_OUT_READY_QUIESCE_B HRESET_B HRESET_REQ_B SRESET_B RTC CLK_OUT IIC1_SDA IIC1_SCL TDI TDO TCK TMS TRST_B ASLEEP LVDD_VSEL0 LVDD_VSEL1 IIC2_SDA_SD-CLK IIC2_SCL_SD-CD

TRIG_IN — TRIG_OUT

HRESET_N HRESET_REQ SRESET_N

CLOCK_OUT

I2C1_SDA

CPU_TDI CPU_TDO CPU_TCK CPU_TMS CPU_TRST_N

ASLEEP

LVDD_VSEL0 LVDD_VSEL1 I2C2_SDA I2C2_SCL

UART_SOUT0_CFG UART_SIN0 UART_SOUT0 UART_CTS0 UART_RTS0

nIRQ0 nIRQ1 nIRQ2 nIRQ3 nIRQ4 nIRQ5 nIRQ6 nIRQ_OUT

CKSTP_IN CKSTP_OUT

BVDD_SEL0 BVDD_SEL1

DMA_DACK0 DMA_DDONE0 DMA_DACK1 DMA_DDONE1 DMA_DREQ2 DMA_DACK2 DMA_DDONE2 DMA_DACK2_CI

TP31 TP37 TP32 TP27 TP64 TP66 TP49 TP65 TP45 TP46 TP62 TP47 TP48

TP34 TP35 TP39 TP33 TP63 TP5 TP75 TP41

R696 R695 R697 10.0K; R431 1.0K; R709 1.5K; R162 49.9; R163 0; R42 0; R725 1.0K; R188 0; R710 1.0K; R187 10.0K; R688 10.0K; R434 4.7K; RN4 10K; R108 R107 R435 DNP 0; R88 R106 R87 R86 1.0K; R692 R693 R164 10.0K 1.0K; R141 R140 R159 R139 R138 R165 R716 0 1.0K DNP For 8569 Rev1 only

R710 DNP For 8569 Rev1 only

3V3 1V8 DGND

SYS CLOCK

J20 CON_1_SMB; R501 49.9; R417 2.2; L20 4.7UH; C366 10uF C367 0.1UF C368 1500PF; R451 1.0K; Y4 OSC. 67MHZ DNP; CLKIOEN_N; EXTCLK; J18 HDR 3X1 Default; CLK_IN; R477 22.1; L8 NFE31PT222Z1E9L; C420 0.1UF; Y7 66.67MHZ; J11 DIP SOCKET 110-83-308-41-105161; OSC_IN; TCLK_IN1; U50 ICS553; U105 NL17SZ125XV5T2G; R478 DNP; SH_CLK; U104 MC100EPT21DTG; XCLK_INP XCLK_INM; R473 R474 83.5; R475 R476 130; C485 C421 C486 C487 0.01uF 0.1UF; R130 PIB_SYSCLK; R129 CNTR_CLK; R169 RTCCLK; R170 SYSCLK; TP41 CNTR_CLK

BOARD CONTROL

U121 U38 U53 U120 NL17SZ126XV5T2G

CFG_STROBE2 ROM_LOC2_IN — R649 390 "Cfg_ROM_loc2" USB_CLK (PC4)

ROM_LOC3_IN — R79 390 "Cfg_ROM_loc3" PD4

PLL_FUSE_IN — R153 390 "Cfg_Pll_fuse_ovrd_dis" PD0

R647 390 "Cfg_Global_waitr" PB7

C591 C80 C139 C590 0.01uF

RS13 RS[0..12] PS[0..13]

PS0 R208 RS0 R209 R210 "Cfg_60x_debug"

PS1 R561 RS1 R560 R559 "Cfg_global_sfto"

PS2 R205 RS2 R206 R207 "Cfg_test_port_dis"

PS3 R502 RS3 R504 R503 "Cfg_DDR1_Debug"

PS4 R562 RS4 R563 R564 "Cfg_DDR2_Debug"

PS5 R644 RS5 R643 R642 "Cfg_I2C_test"

PS6 R215 RS6 R216 R217 "Cfg_abist_en"

PS7 R185 RS7 R184 R186 "Cfg_svr0"

PS8 R517 RS8 R515 R516 "Cfg_svr1"

PS9 R512 RS9 R513 R514 "Cfg_eng_use0"

PS10 R570 RS10 R571 R572 "Cfg_eng_use1"

PS11 R573 RS11 R574 R575 "Cfg_spare"

PS12 R617 RS12 R618 R619 "Cfg_slave_mode_dis"

PS13 R689 RS13 R690 R691 "Cfg_Global_waitr"

DNP 0 1.0K

GETH CLOCK

U21 ICS840S071

XTAL_IN XTAL_OUT REFIN REF_SEL F_SELAA0 F_SELAA1 F_SELAA2 F_SELB0 F_SELB1 F_SELB2 nREF_OE MR/nOE SLEW0 SLEW1 VDD VDDA VDDO_AA VDDO_AB VDDO_B VDDO_REF QAA QAB QB0 QB1 QB2 REF_OUT0 REF_OUT1 GND1 GND2 GND3 GND4 GND_REF EP

Y1 OSC. 25MHZ; L3 0.12UH; R31 1.0K; C27 0.1UF; R312 1.0K; R56 1.0K; C256 0.01uF; R491 1.0K; R490 33

GETH_CLKSEL

GETH_CLKSEL	QAA
0	50MHz
1	125MHz

SYSCLK_MR SLEW0 SLEW1

Setting		Slew Rate
SLEW1	SLEW0	(V/ns)
0	0	4
0	1	3
1	0	2
1	1	1

U103 FANOUT BUFFER 0...350MHz MPC9448

PCLK PCLK CLK_STOP CLK_SEL OE CCLK

R111 R466 R112 R467 R445 R444 R447 R446 R109 R468 R110 R492 DNP

UEM1_MICCLK_IN UEM1_MVCLK_IN UEM2_MICCLK_IN UEM2_MVCLK_IN — 50/125MHz

R50 R59 R58 R57

UCC1_3_IN125 UCC2_4_IN125 GETH_PHY1_CLKIN GETH_PHY2_CLKIN — 125MHz

C255 C30 C45 C287 C286 C279 C288 C289 C280 C257 C480 C520 C481 C418 C417 C478 C479 0.1UF 0.01UF 10UF

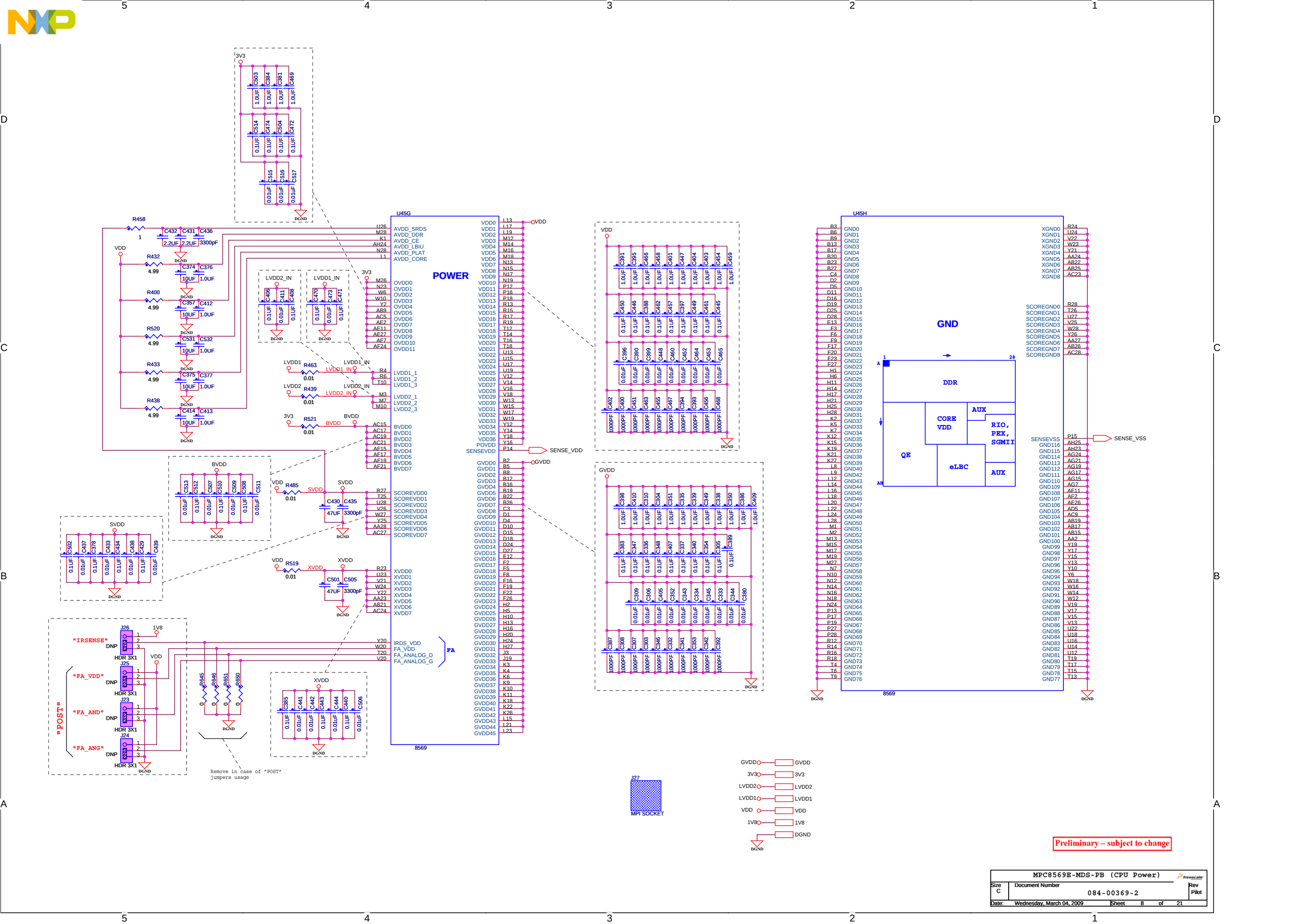
PTP CLOCK

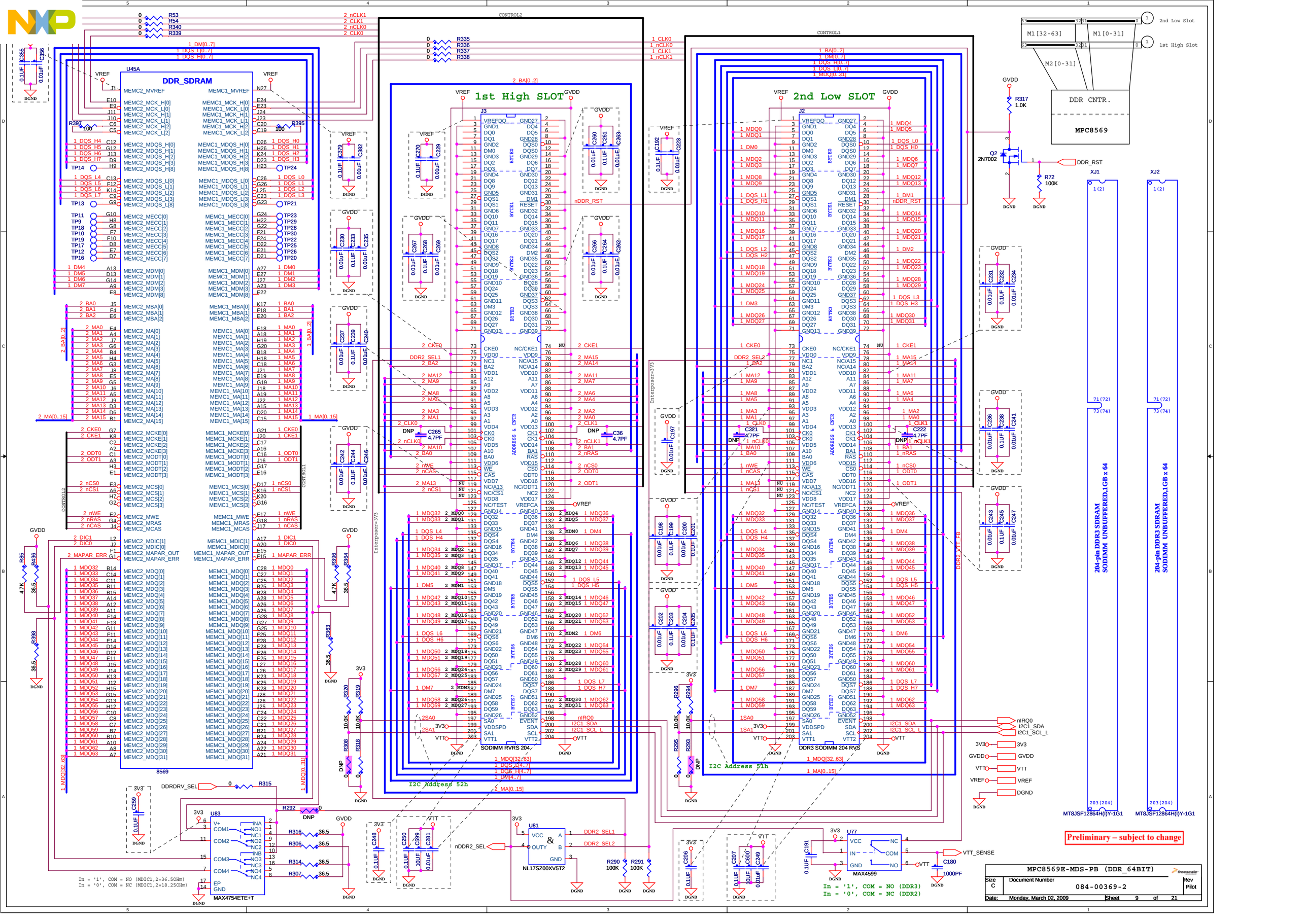
J22 CON_1_SMB; R416 2.2; L19 4.7UH; C363 10uF C365 0.1UF C364 1500PF; R556 49.9; PTP_EXTCLK; J19 HDR 3X1 Default; PTP_OSC_IN; R472 22.1 XPC28; R450 1.0K; Y6 66.67MHZ; J12 DIP SOCKET 110-83-308-41-105161

3V3 3V3; 1V8 1V8; DGND

Preliminary – subject to change

MPC8569E-MDS-PB (CPU MISC & SYSCLK)		
Size C	Document Number 084-00369-2	Rev Pilot
Date: Wednesday, March 04, 2009	Sheet 7 of 21	


U45G
POWER
U45H
GND
DDR
CORE VDD
AUX
RIO, PEX, SGMII
QE
eLBC
AUX
R458
R432
R400
R520
R433
R438
C432 C431 C436
2.2UF 2.2UF 3300pF
C374 C376
C357 C412
C531 C532
C375 C377
C414 C413
10UF 1.0UF
4.99
VDD
DGND
3V3
LVDD2_IN
LVDD1_IN
C406 C411 C408
C470 C473 C471
0.1UF 0.01UF
LVDD1
LVDD2
R463
R439
0.01
BVDD
R521
SVDD
R485
XVDD
R519
C430 C435
C501 C505
47UF 3300pF
C513 C512 C507 C510 C509 C508 C511
C502 C437 C378 C433 C434 C438 C429 C439
0.01UF 0.1UF
AVDD_SRDS
AVDD_DDR
AVDD_CE
AVDD_LBIU
AVDD_PLAT
AVDD_CORE
OVDD0
OVDD1
OVDD2
OVDD3
OVDD4
OVDD5
OVDD6
OVDD7
OVDD8
OVDD9
OVDD10
OVDD11
LVDD1_1
LVDD1_2
LVDD1_3
LVDD2_1
LVDD2_2
LVDD2_3
BVDD0
BVDD1
BVDD2
BVDD3
BVDD4
BVDD5
BVDD6
BVDD7
SCOREVDD0
SCOREVDD1
SCOREVDD2
SCOREVDD3
SCOREVDD4
SCOREVDD5
SCOREVDD6
SCOREVDD7
XVDD0
XVDD1
XVDD2
XVDD3
XVDD4
XVDD5
XVDD6
XVDD7
IRDS_VDD
FA_VDD
FA_ANALOG_D
FA_ANALOG_G
FA
8569
VDD0
VDD1
VDD2
VDD3
VDD4
VDD5
VDD6
VDD7
VDD8
VDD9
VDD10
VDD11
VDD12
VDD13
VDD14
VDD15
VDD16
VDD17
VDD18
VDD19
VDD20
VDD21
VDD22
VDD23
VDD24
VDD25
VDD26
VDD27
VDD28
VDD29
VDD30
VDD31
VDD32
VDD33
VDD34
VDD35
VDD36
POVDD
SENSEVDD
SENSE_VDD
GVDD0
GVDD1
GVDD2
GVDD3
GVDD4
GVDD5
GVDD6
GVDD7
GVDD8
GVDD9
GVDD10
GVDD11
GVDD12
GVDD13
GVDD14
GVDD15
GVDD16
GVDD17
GVDD18
GVDD19
GVDD20
GVDD21
GVDD22
GVDD23
GVDD24
GVDD25
GVDD26
GVDD27
GVDD28
GVDD29
GVDD30
GVDD31
GVDD32
GVDD33
GVDD34
GVDD35
GVDD36
GVDD37
GVDD38
GVDD39
GVDD40
GVDD41
GVDD42
GVDD43
GVDD44
GVDD45
GVDD
J26
J25
J23
J24
"IRSENSE"
"FA_VDD"
"FA_AND"
"FA_ANG"
"POST"
DNP
HDR 3X1
1V8
R645 R646 R651 R650
0
Remove in case of "POST" jumpers usage
J27
MPI SOCKET
GND0
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
GND11
GND12
GND13
GND14
GND15
GND16
GND17
GND18
GND19
GND20
GND21
GND22
GND23
GND24
GND25
GND26
GND27
GND28
GND29
GND30
GND31
GND32
GND33
GND34
GND35
GND36
GND37
GND38
GND39
GND40
GND42
GND43
GND44
GND45
GND46
GND47
GND48
GND49
GND50
GND51
GND52
GND53
GND54
GND55
GND56
GND57
GND58
GND59
GND60
GND61
GND62
GND63
GND64
GND65
GND66
GND67
GND68
GND69
GND70
GND71
GND72
GND73
GND74
GND75
GND76
XGND0
XGND1
XGND2
XGND3
XGND4
XGND5
XGND6
XGND7
XGND8
SCOREGND0
SCOREGND1
SCOREGND2
SCOREGND3
SCOREGND4
SCOREGND5
SCOREGND6
SCOREGND7
SCOREGND8
SENSEVSS
SENSE_VSS
GND116
GND115
GND114
GND113
GND112
GND111
GND110
GND109
GND108
GND107
GND106
GND105
GND104
GND103
GND102
GND101
GND100
GND99
GND98
GND97
GND96
GND95
GND94
GND93
GND92
GND91
GND90
GND89
GND88
GND87
GND86
GND85
GND84
GND83
GND82
GND81
GND80
GND79
GND78
GND77
8569
GVDD
3V3
LVDD2
LVDD1
VDD
1V8
DGND
Preliminary – subject to change
MPC8569E-MDS-PB (CPU Power)
freescale
Size C
Document Number 084-00369-2
Rev Pilot
Date: Wednesday, March 04, 2009
Sheet 8 of 21


DDR_SDRAM
U45A
MEMC2_MVREF
MEMC1_MVREF
MEMC2_MCK_H[0]
MEMC2_MCK_L[0]
MEMC2_MCK_H[1]
MEMC2_MCK_L[1]
MEMC2_MCK_H[2]
MEMC2_MCK_L[2]
MEMC1_MCK_H[0]
MEMC1_MCK_L[0]
MEMC1_MCK_H[1]
MEMC1_MCK_L[1]
MEMC1_MCK_H[2]
MEMC1_MCK_L[2]
MEMC2_MDQS_H[0]
MEMC2_MDQS_H[1]
MEMC2_MDQS_H[2]
MEMC2_MDQS_H[3]
MEMC2_MDQS_H[8]
MEMC1_MDQS_H[0]
MEMC1_MDQS_H[1]
MEMC1_MDQS_H[2]
MEMC1_MDQS_H[3]
MEMC1_MDQS_H[8]
MEMC2_MDQS_L[0]
MEMC2_MDQS_L[1]
MEMC2_MDQS_L[2]
MEMC2_MDQS_L[3]
MEMC2_MDQS_L[8]
MEMC1_MDQS_L[0]
MEMC1_MDQS_L[1]
MEMC1_MDQS_L[2]
MEMC1_MDQS_L[3]
MEMC1_MDQS_L[8]
MEMC2_MECC[0]
MEMC2_MECC[1]
MEMC2_MECC[2]
MEMC2_MECC[3]
MEMC2_MECC[4]
MEMC2_MECC[5]
MEMC2_MECC[6]
MEMC2_MECC[7]
MEMC1_MECC[0]
MEMC1_MECC[1]
MEMC1_MECC[2]
MEMC1_MECC[3]
MEMC1_MECC[4]
MEMC1_MECC[5]
MEMC1_MECC[6]
MEMC1_MECC[7]
MEMC2_MDM[0]
MEMC2_MDM[1]
MEMC2_MDM[2]
MEMC2_MDM[3]
MEMC2_MDM[8]
MEMC1_MDM[0]
MEMC1_MDM[1]
MEMC1_MDM[2]
MEMC1_MDM[3]
MEMC1_MDM[8]
MEMC2_MBA[0]
MEMC2_MBA[1]
MEMC2_MBA[2]
MEMC1_MBA[0]
MEMC1_MBA[1]
MEMC1_MBA[2]
MEMC2_MA[0]
MEMC2_MA[1]
MEMC2_MA[2]
MEMC2_MA[3]
MEMC2_MA[4]
MEMC2_MA[5]
MEMC2_MA[6]
MEMC2_MA[7]
MEMC2_MA[8]
MEMC2_MA[9]
MEMC2_MA[10]
MEMC2_MA[11]
MEMC2_MA[12]
MEMC2_MA[13]
MEMC2_MA[14]
MEMC2_MA[15]
MEMC1_MA[0]
MEMC1_MA[1]
MEMC1_MA[2]
MEMC1_MA[3]
MEMC1_MA[4]
MEMC1_MA[5]
MEMC1_MA[6]
MEMC1_MA[7]
MEMC1_MA[8]
MEMC1_MA[9]
MEMC1_MA[10]
MEMC1_MA[11]
MEMC1_MA[12]
MEMC1_MA[13]
MEMC1_MA[14]
MEMC1_MA[15]
MEMC2_MCKE[0]
MEMC2_MCKE[1]
MEMC2_MCKE[2]
MEMC2_MCKE[3]
MEMC2_MODT[0]
MEMC2_MODT[1]
MEMC2_MODT[2]
MEMC2_MODT[3]
MEMC1_MCKE[0]
MEMC1_MCKE[1]
MEMC1_MCKE[2]
MEMC1_MCKE[3]
MEMC1_MODT[0]
MEMC1_MODT[1]
MEMC1_MODT[2]
MEMC1_MODT[3]
MEMC2_MCS[0]
MEMC2_MCS[1]
MEMC2_MCS[2]
MEMC2_MCS[3]
MEMC1_MCS[0]
MEMC1_MCS[1]
MEMC1_MCS[2]
MEMC1_MCS[3]
MEMC2_MWE
MEMC2_MRAS
MEMC2_MCAS
MEMC1_MWE
MEMC1_MRAS
MEMC1_MCAS
MEMC2_MDIC[1]
MEMC2_MDIC[0]
MEMC2_MAPAR_OUT
MEMC2_MAPAR_ERR
MEMC1_MDIC[1]
MEMC1_MDIC[0]
MEMC1_MAPAR_OUT
MEMC1_MAPAR_ERR
MEMC2_MDQ[0]
MEMC2_MDQ[1]
MEMC2_MDQ[2]
MEMC2_MDQ[3]
MEMC2_MDQ[4]
MEMC2_MDQ[5]
MEMC2_MDQ[6]
MEMC2_MDQ[7]
MEMC2_MDQ[8]
MEMC2_MDQ[9]
MEMC2_MDQ[10]
MEMC2_MDQ[11]
MEMC2_MDQ[12]
MEMC2_MDQ[13]
MEMC2_MDQ[14]
MEMC2_MDQ[15]
MEMC2_MDQ[16]
MEMC2_MDQ[17]
MEMC2_MDQ[18]
MEMC2_MDQ[19]
MEMC2_MDQ[20]
MEMC2_MDQ[21]
MEMC2_MDQ[22]
MEMC2_MDQ[23]
MEMC2_MDQ[24]
MEMC2_MDQ[25]
MEMC2_MDQ[26]
MEMC2_MDQ[27]
MEMC2_MDQ[28]
MEMC2_MDQ[29]
MEMC2_MDQ[30]
MEMC2_MDQ[31]
MEMC1_MDQ[0]
MEMC1_MDQ[1]
MEMC1_MDQ[2]
MEMC1_MDQ[3]
MEMC1_MDQ[4]
MEMC1_MDQ[5]
MEMC1_MDQ[6]
MEMC1_MDQ[7]
MEMC1_MDQ[8]
MEMC1_MDQ[9]
MEMC1_MDQ[10]
MEMC1_MDQ[11]
MEMC1_MDQ[12]
MEMC1_MDQ[13]
MEMC1_MDQ[14]
MEMC1_MDQ[15]
MEMC1_MDQ[16]
MEMC1_MDQ[17]
MEMC1_MDQ[18]
MEMC1_MDQ[19]
MEMC1_MDQ[20]
MEMC1_MDQ[21]
MEMC1_MDQ[22]
MEMC1_MDQ[23]
MEMC1_MDQ[24]
MEMC1_MDQ[25]
MEMC1_MDQ[26]
MEMC1_MDQ[27]
MEMC1_MDQ[28]
MEMC1_MDQ[29]
MEMC1_MDQ[30]
MEMC1_MDQ[31]
8569
CONTROL2
CONTROL1
1st High SLOT
2nd Low SLOT
J3
J2
SODIMM RVRS 204
DDR3 SODIMM 204 RVS
I2C Address 52h
I2C Address 51h
nDDR_RST
nIRQ0
I2C1_SDA
I2C1_SCL_L
Interposer=3V3
DDR2_VTT_EN
M1[32-63]
M1[0-31]
M2[0-31]
2nd Low Slot
1st High Slot
DDR CNTR.
MPC8569
DDR_RST
204-pin DDR3 SDRAM
SODIMM UNBUFFERED,1GB x 64
MT8JSF12864H(I)Y-1G1
MAX4754ETE+T
NL17SZ00XV5T2
MAX4599
In = '1', COM = NO (MDIC1,2=36.50Hm)
In = '0', COM = NC (MDIC1,2=18.25Ohm)
In = '1', COM = NO (DDR3)
In = '0', COM = NC (DDR2)
Preliminary – subject to change
MPC8569E-MDS-PB (DDR_64BIT)
Document Number 084-00369-2
Rev Pilot
Date: Monday, March 02, 2009
Sheet 9 of 21

GETH1

125MHz_IN_CLK Selected

U58A

MDC_L
MDIO
G1RXDV
G1RXD[0..3]
UCC1_GTXCLK_DL
G1TXEN
G1TXD[0..3]
GETH1EN_N
GETH_PHY1_CLKIN
UCC1_RXCLK
nIRQ1

MDI3_M
MDI3_P
MDI2_M
MDI2_P
MDI1_M
MDI1_P
MDI0_M
MDI0_P

G1MDI3M
G1MDI3P
G1MDI2M
G1MDI2P
G1MDI1M
G1MDI1P
G1MDI0M
G1MDI0P

G1FOSIN_P
G1FOSIN_M
G1FOSOUT_P
G1FOSOUT_M
G1_010
G1_LINK1000
G1_LINK100
G1_CNF6
G1_CFG4
G1_CFG3

Address "00111"

To be replaced for 49.9Ohm in case of Delay Line used

J14 — RJ45_LED — 1G — 100M

2V5GETH1A

1VGETH1 2V5GETH 2V5GETH1A

U58B — 88E1111-BAB — POWER

GETH2

U23A

G2RXDV
G2RXD[0..3]
UCC2_GTXCLK_DL
G2TXEN
G2TXD[0..3]
GETH2EN_N
GETHRST_N
GETH_PHY2_CLKIN
UCC2_RXCLK
nIRQ2

G2MDI3M
G2MDI3P
G2MDI2M
G2MDI2P
G2MDI1M
G2MDI1P
G2MDI0M
G2MDI0P

G2FOSIN_P
G2FOSIN_M
G2FOSOUT_P
G2FOSOUT_M
G2_010
G2_LINK1000
G2_LINK100
G2_CNF0
G2_CNF6
G2_CFG4
G2_CFG3

Address "00001"

J6 — RJ45_LED — 1G — 100M

2V5GETH2A

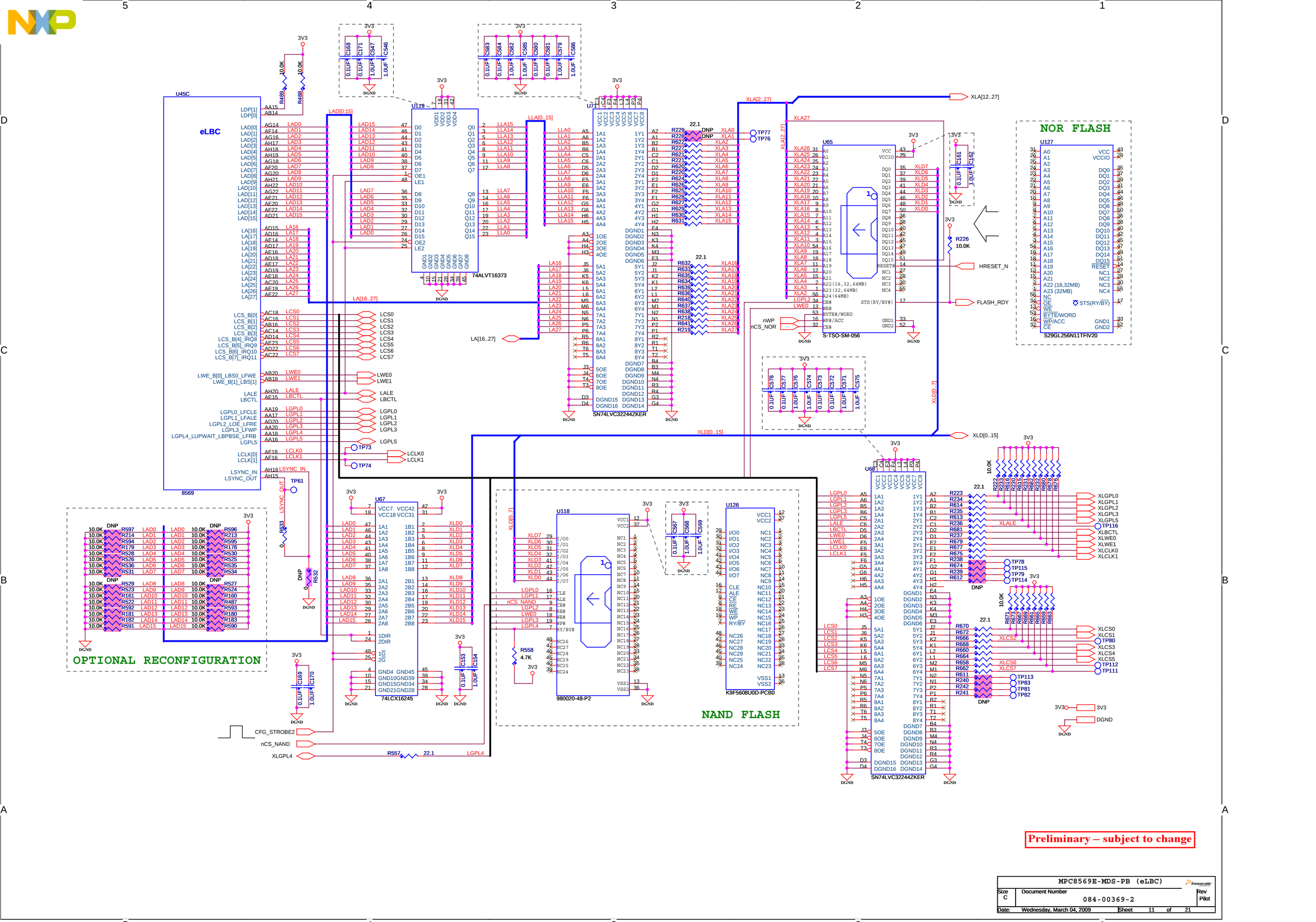
1VGETH2 2V5GETH2A 2V5GETH

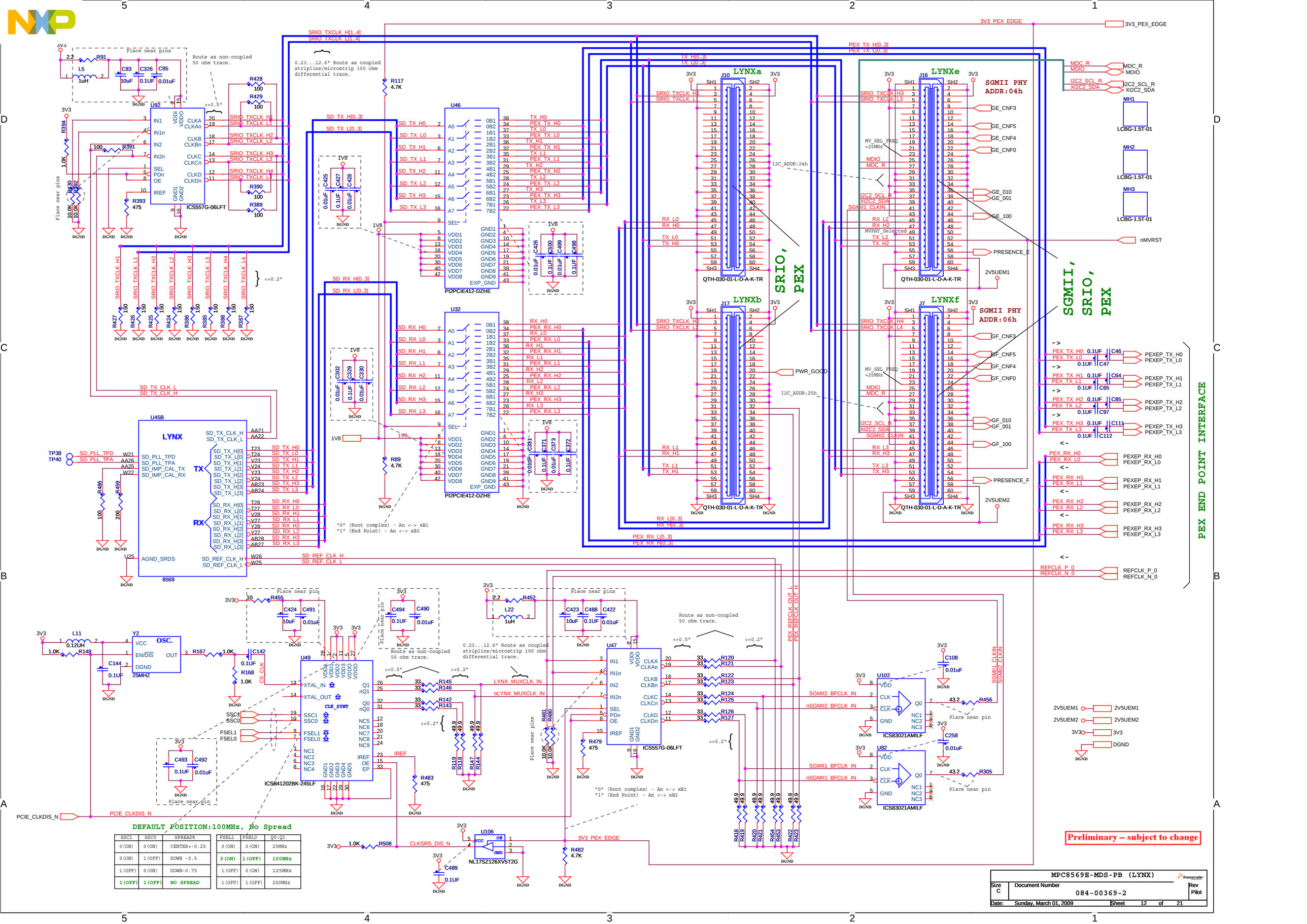
U23B — 88E1111-BAB — POWER

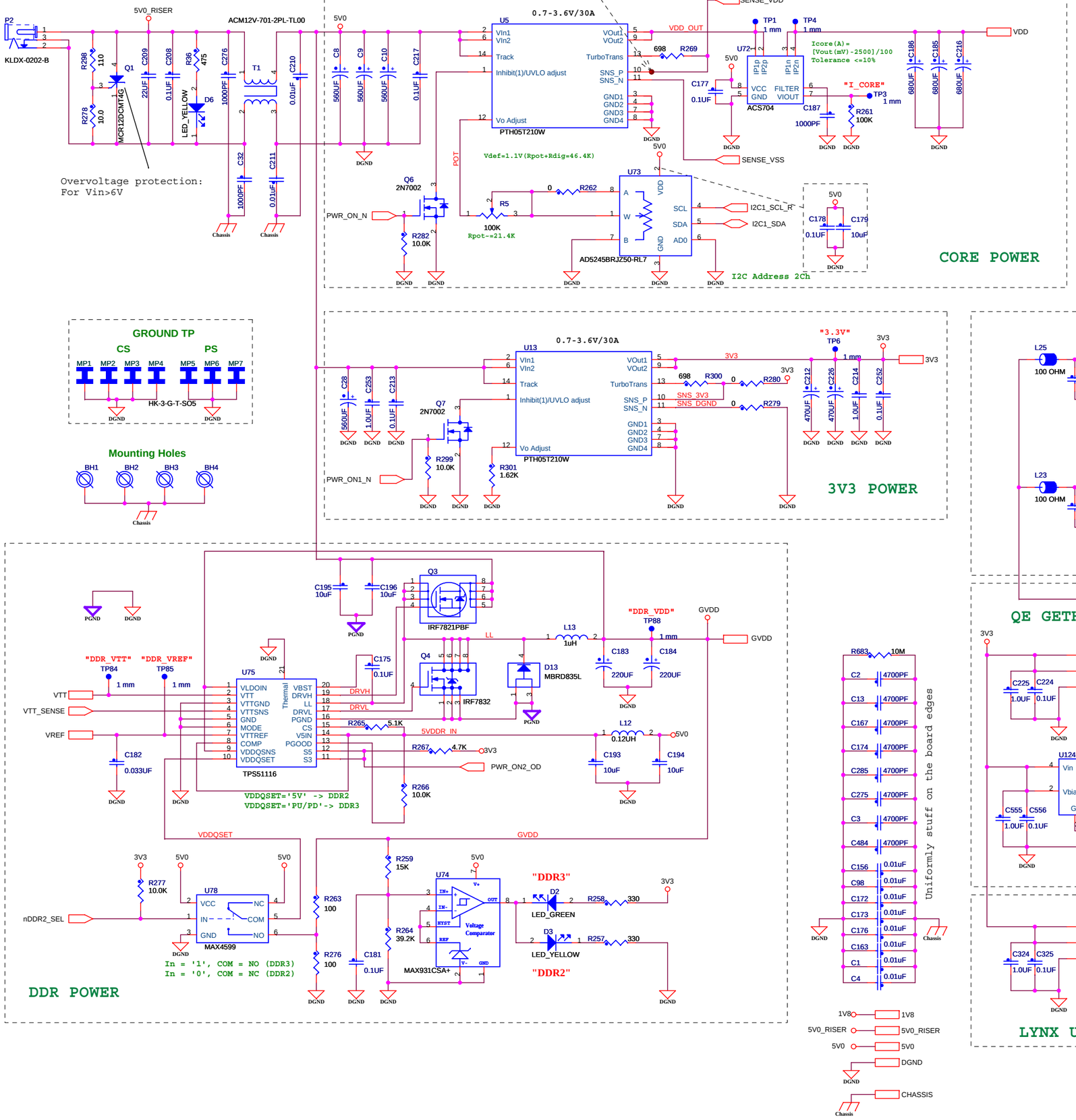
3V3 2V5GETH 2V5GETH1A 2V5GETH2A 1VGETH1 1VGETH2 DGND CHASSIS

Preliminary – subject to change

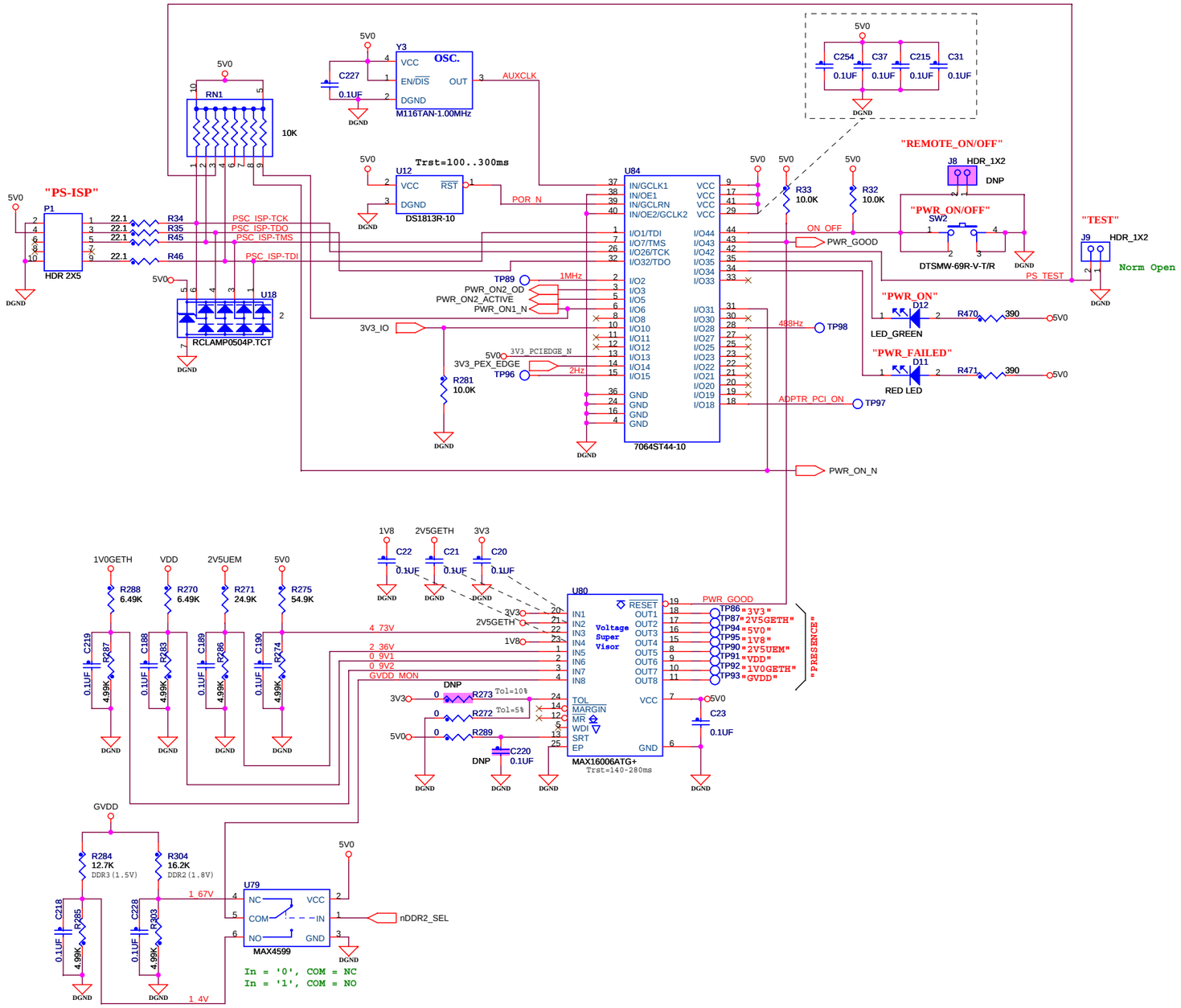
MPC8569E-MDS-PB (GETH 1,2)		
Size C	Document Number 084-00369-2	Rev Pilot
Date: Sunday, March 01, 2009	Sheet 10 of 21	

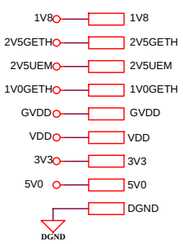

eLBC
U45C
8569
LAD[0:15]
LA[16..27]
LA[0..15]
LA[16..27]
LCS[0..7]
LWE_B[0]_LBS0_LFWE
LWE_B[1]_LBS1_LFWE
LALE
LBCTL
LGPL0_LFCLE
LGPL1_LFALE
LGPL2_LOE_LFRE
LGPL3_LFWP
LGPL4_LUPWAIT_LBPBSE_LFRB
LGPL5
LCLK[0]
LCLK[1]
LSYNC_IN
LSYNC_OUT
TP61
TP73
TP74
74ALVT16373
SN74LVC32244ZKER
XLA[2..27]
XLA[12..27]
XLA27
XLD[0..7]
XLD[0..15]
U65
S-TSO-SM-056
NOR FLASH
U127
S29GL256N11TFIV20
HRESET_N
FLASH_RDY
nWP
nCS_NOR
R226
10.0K
OPTIONAL RECONFIGURATION
74LCX16245
CFG_STROBE2
nCS_NAND
XLGPL4
R557
22.1
U67
U118
980020-48-P2
U126
K9F5608U0D-PCB0
NAND FLASH
R558
4.7K
U68
XLGPL0
XLGPL1
XLGPL2
XLGPL3
XLGPL5
XLALE
XLBCTL
XLWE0
XLWE1
XLCLK0
XLCLK1
XLCS0
XLCS1
XLCS2
XLCS3
XLCS4
XLCS5
XLCS6
XLCS7
TP116
TP78
TP115
TP79
TP114
TP80
TP112
TP111
TP113
TP83
TP81
TP82
Preliminary – subject to change
MPC8569E-MDS-PB (eLBC)
Document Number
084-00369-2
Rev
Pilot
Size
C
Date: Wednesday, March 04, 2009
Sheet 11 of 21


SRIO_TXCLK_H[1..4]
SRIO_TXCLK_L[1..4]
0.23...12.6" Route as coupled stripline/microstrip 100 ohm differential trace.
Place near pins
Route as non-coupled 50 ohm trace.
ICS557G-06LFT
SD_TX_H[0..3]
SD_TX_L[0..3]
PI2PCIE412-DZHE
SD_RX_H[0..3]
SD_RX_L[0..3]
LYNX
SD_TX_CLK_H
SD_TX_CLK_L
SD_PLL_TPD
SD_PLL_TPA
SD_IMP_CAL_TX
SD_IMP_CAL_RX
TX
RX
"0" (Root complex) - An <-> xB1
"1" (End Point) - An <-> xB2
AGND_SRDS
8569
SD_REF_CLK_H
SD_REF_CLK_L
LYNXa
LYNXb
LYNXe
LYNXf
QTH-030-01-L-D-A-K-TR
SRIO, PEX
SGMII PHY ADDR:04h
SGMII PHY ADDR:06h
SGMII, SRIO, PEX
PEX END POINT INTERFACE
I2C_ADDR:24h
I2C_ADDR:25h
PWR_GOOD
MDC_R
MDIO
I2C2_SCL_R
XI2C2_SDA
MH1
MH2
MH3
LCBG-1.5T-01
GE_CNF3
GE_CNF5
GE_CNF4
GE_CNF0
GE_010
GE_001
GE_100
nMVRST
PRESENCE_E
2V5UEM1
GF_CNF3
GF_CNF5
GF_CNF4
GF_CNF0
GF_010
GF_001
GF_100
PRESENCE_F
2V5UEM2
PEXEP_TX_H0
PEXEP_TX_L0
PEXEP_TX_H1
PEXEP_TX_L1
PEXEP_TX_H2
PEXEP_TX_L2
PEXEP_TX_H3
PEXEP_TX_L3
PEXEP_RX_H0
PEXEP_RX_L0
PEXEP_RX_H1
PEXEP_RX_L1
PEXEP_RX_H2
PEXEP_RX_L2
PEXEP_RX_H3
PEXEP_RX_L3
REFCLK_P_0
REFCLK_N_0
PEX_REFCLK_OUT_L
PEX_REFCLK_OUT_H
SGMII2_CLK/N
SGMII1_CLK/N
ICS841202BK-245LF
ICS83021AMILF
ICS557G-06LFT
NL17SZ126XV5T2G
OSC.
25MHZ
CS_CLK
SSC1
SSC0
FSEL1
FSEL0
IREF
PCIE_CLKDIS_N
CLKSRS_DIS_N
3V3_PEX_EDGE
DEFAULT POSITION:100MHz, No Spread
SSC1 SSC0 SPREAD%
0 (ON) 0 (ON) CENTER+-0.25
0 (ON) 1 (OFF) DOWN -0.5
1 (OFF) 0 (ON) DOWN-0.75
1 (OFF) 1 (OFF) NO SPREAD
FSEL1 FSEL0 Q0:Q1
0 (ON) 0 (ON) 25MHz
0 (ON) 1 (OFF) 100MHz
1 (OFF) 0 (ON) 125MHz
1 (OFF) 1 (OFF) 250MHz
Preliminary – subject to change
MPC8569E-MDS-PB (LYNX)
freescale
Size C
Document Number 084-00369-2
Rev Pilot
Date: Sunday, March 01, 2009
Sheet 12 of 21


Measure VDD here!!!
0.7-3.6V/30A
U5
PTH05T210W
SENSE_VDD
SENSE_VSS
VDD_OUT
VDD
TP1
TP4
Icore(A)=
[Vout(mV)-2500]/100
Tolerance <=10%
U72
ACS704
"I_CORE"
TP3
R261
100K
C187
1000PF
Vdef=1.1V(Rpot+Rdig=46.4K)
POT
Rpot-=21.4K
U73
AD5245BRJZ50-RL7
I2C1_SCL_R
I2C1_SDA
I2C Address 2Ch
Q6
2N7007
PWR_ON_N
R282
10.0K
R5
100K
R262
CORE POWER
Overvoltage protection:
For Vin>6V
ACM12V-701-2PL-TL00
KLDX-0202-B
MCR12DCMT4G
LED_YELLOW
T1
Chassis
GROUND TP
CS
PS
MP1
MP2
MP3
MP4
MP5
MP6
MP7
HK-3-G-T-SO5
Mounting Holes
BH1
BH2
BH3
BH4
U13
PTH05T210W
"3.3V"
TP6
3V3 POWER
Q7
2N7007
PWR_ON1_N
R299
10.0K
R301
1.62K
R300
R280
R279
SNS_3V3
SNS_DGND
CPU FAN
"5V FAN"
J4
HDR_1X2
Q5
2N7002
PWR_ON2_ACTIVE
R302
100K
LYNX MUX's POWER
U56
MIC37139-1.8BS
"1V8"
TP67
L10
100 OHM
LVDD1-VSEL
LVDD2-VSEL
UCC1-4 POWER
U109
U98
TPS2115
LVDD1
LVDD_VSEL0
LVDD2
LVDD_VSEL1
LVDD_VSEL/D1 | LVDD
1 | 2.5V/IN1
0 | 3.3V/IN2
QE GETH's POWER
U76
LT1764AEQ-2.5
"2V5GETH"
TP2
2V5GETH
2V5GETH1A
2V5GETH2A
U124
MIC49300WR
"1V0"
TP110
1V0GETH
1VGETH1
1VGETH2
LYNX UEM's POWER
U34
"2V5UEM"
TP36
2V5UEM
2V5UEM1
2V5UEM2
Uniformly stuff on the board edges
Preliminary – subject to change
MPC8569E-MDS-PB (PS)
Size C
Document Number 084-00369-2
Rev Pilot
Date: Wednesday, March 04, 2009
Sheet 13 of 21

DDR POWER
U75
TPS51116
"DDR_VTT"
"DDR_VREF"
TP84
TP85
VTT
VTT_SENSE
VREF
VDDQSET='5V' -> DDR2
VDDQSET='PU/PD'-> DDR3
U78
MAX4599
nDDR2_SEL
In = '1', COM = NO (DDR3)
In = '0', COM = NC (DDR2)
Q3
IRF7821PBF
Q4
IRF7832
D13
MBRD835L
"DDR_VDD"
TP88
GVDD
U74
MAX931CSA+
Voltage Comparator
"DDR3"
"DDR2"
D2
LED_GREEN
D3
LED_YELLOW
1V8
5V0_RISER
5V0
DGND
CHASSIS





Preliminary – subject to change

MPC8569E-MDS-PB (PS_Control)		
Size C	Document Number 084-00369-2	Rev Pilot
Date: Wednesday, March 04, 2009	Sheet 14 of 21	

GETH3

GETH4

QE: A,B,C

8569

Preliminary – subject to change

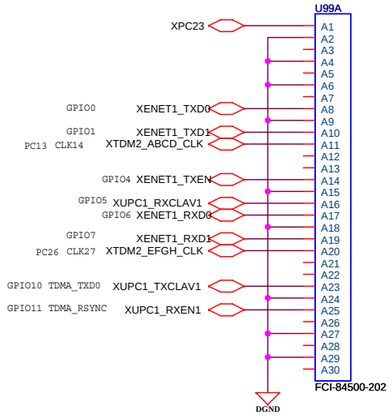
QE:
D,E,F

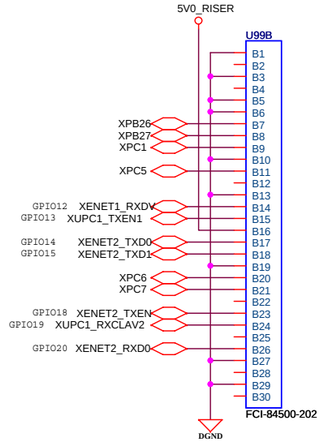
UPC1 Connected to PMC0
TDM1X connected to PMC0
TDM2X connected to PMC1

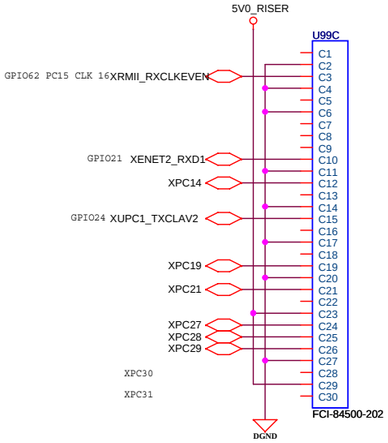
Preliminary – subject to change

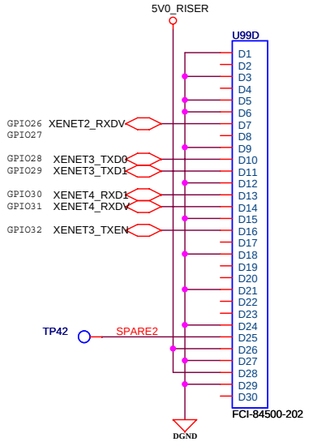
MPC8569E-MDS-PB (QE_PORT D,E,F)		
Size C	Document Number 084-00369-2	Rev Pilot
Date: Wednesday, March 04, 2009	Sheet 16 of 21	

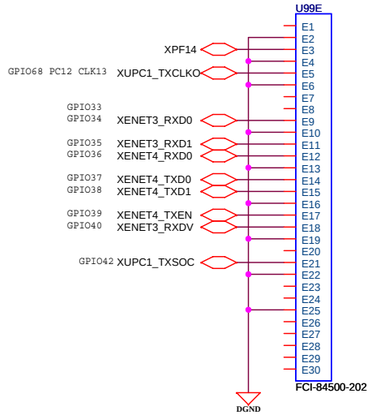
GPIO

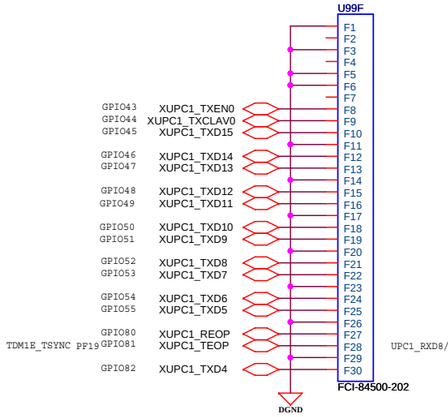


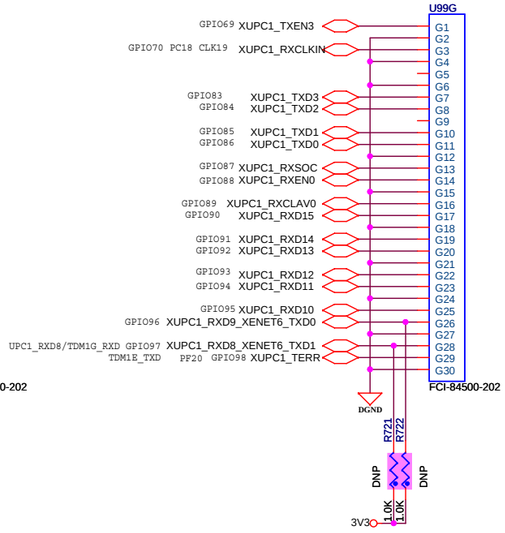


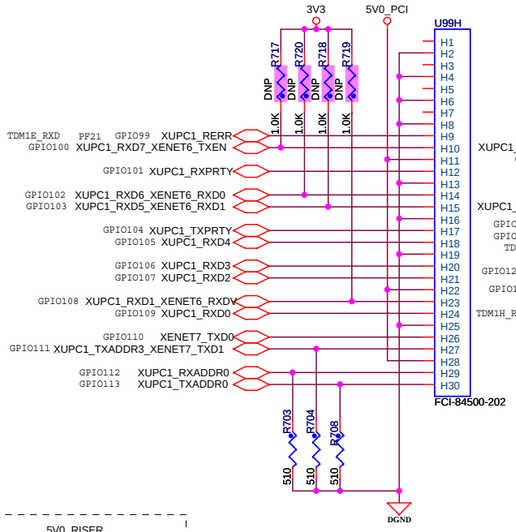


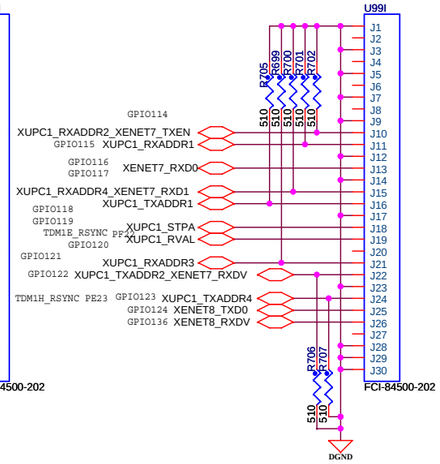


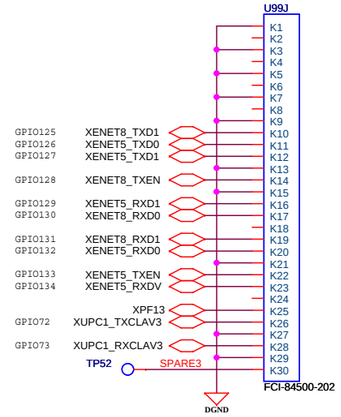


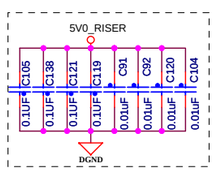








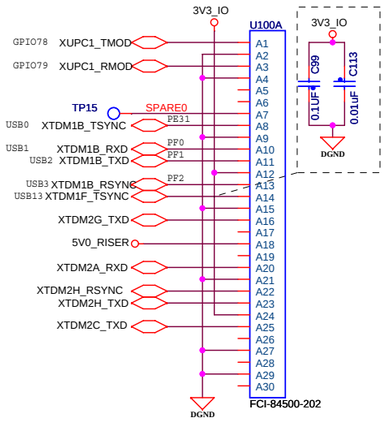


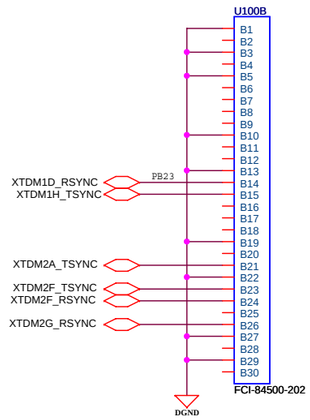


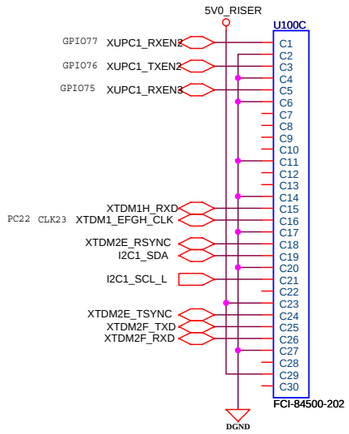
UPC1 Connected to PMC0
TDM1X connected to PMC0
TDM2X connected to PMC1

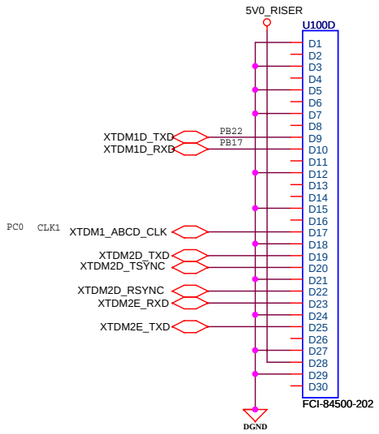
Preliminary – subject to change

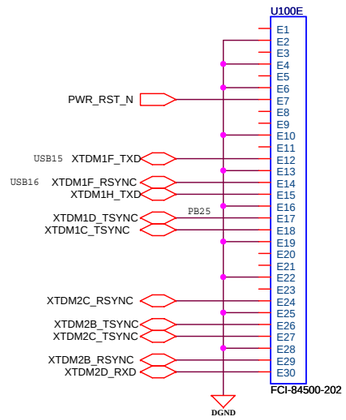
MPC8569E-MDS-PB (Riser Connector L)		
Size C	Document Number 084-00369-2	Rev Pilot
Date: Wednesday, March 04, 2009	Sheet 17 of 21	

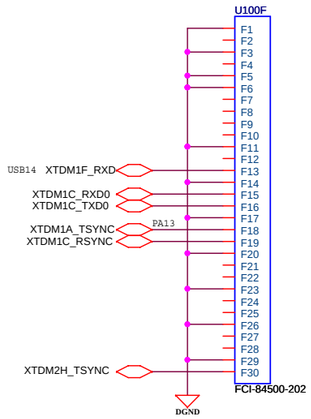


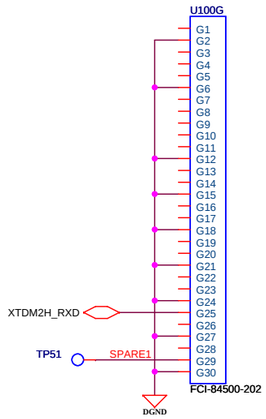


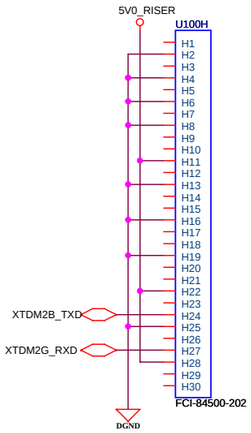


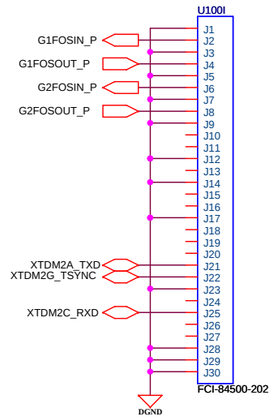


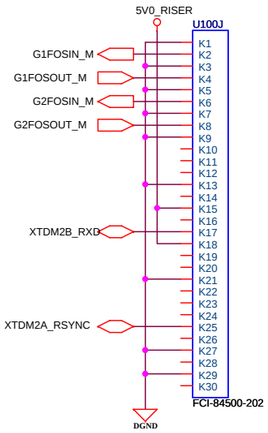


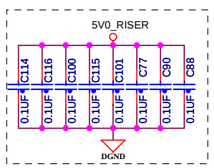










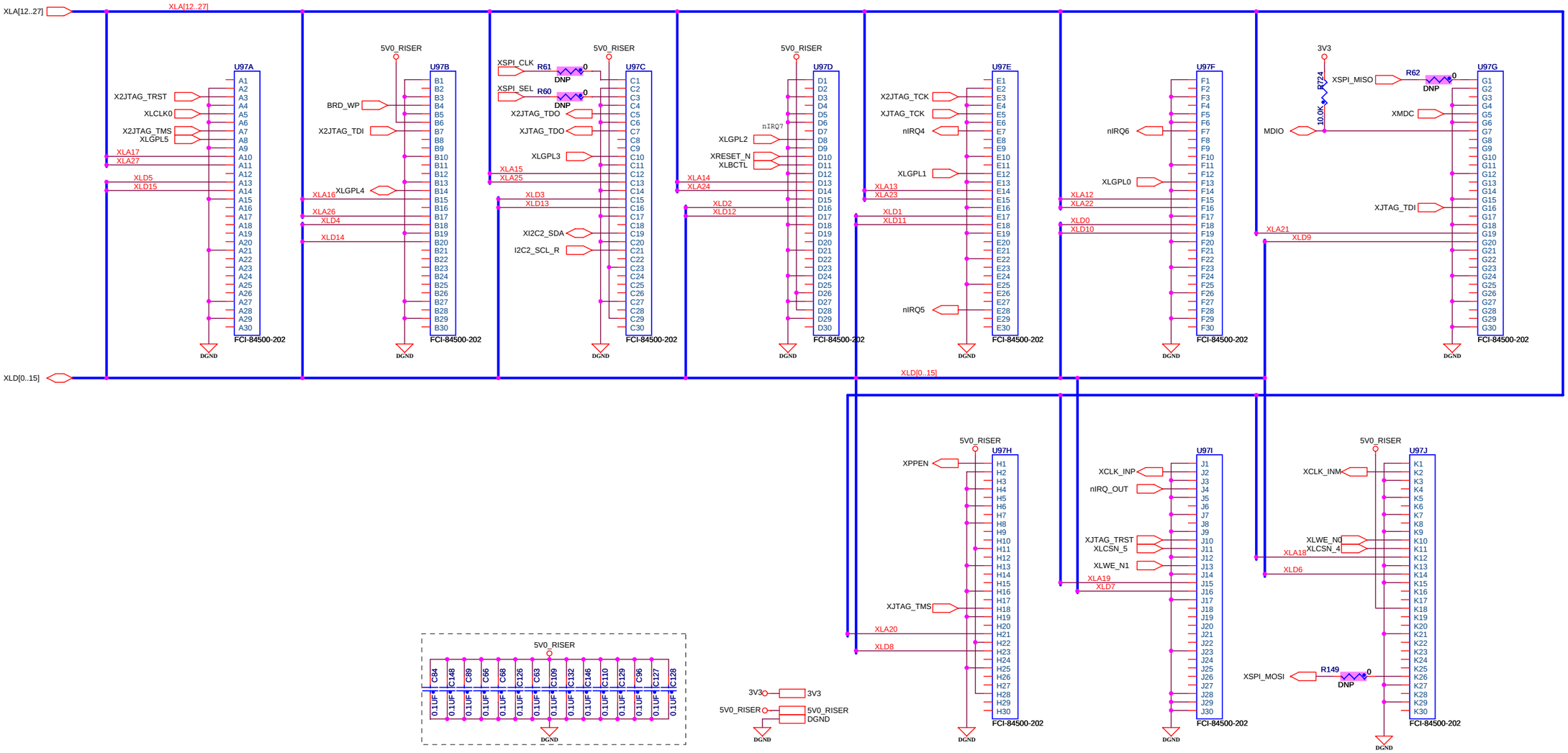


UPC1 Connected to PMC0
TDM1X connected to PMC0
TDM2X connected to PMC1

Preliminary – subject to change

MPC8568E-MDS-PB (Riser Connectors LL)		
Size C	Document Number 084-00369-2	Rev Pilot
Date: Sunday, March 01, 2009	Sheet 18 of 21	

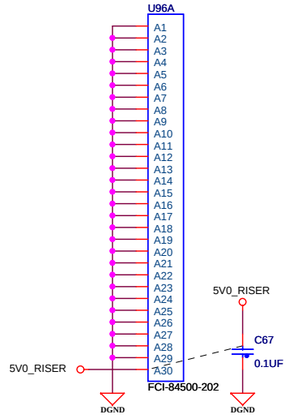
Local Bus

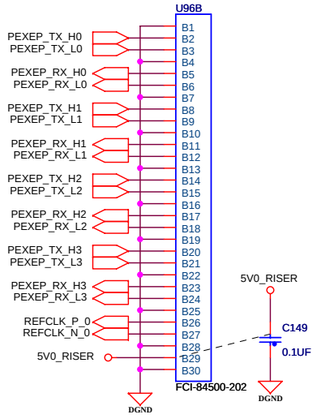


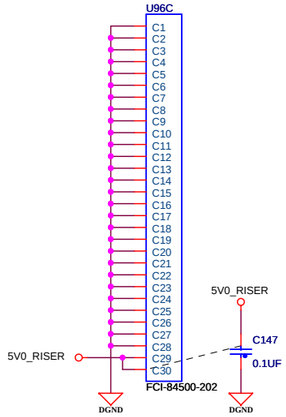
Preliminary – subject to change

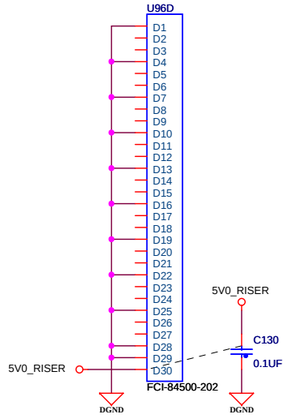
MPC8569E-MDS-PB (Riser Connector R)		
Size C	Document Number 084-00369-2	Rev Pilot
Date: Sunday, March 01, 2009	Sheet 19 of 21	

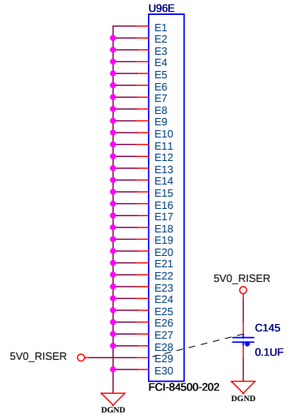
LYNX lines

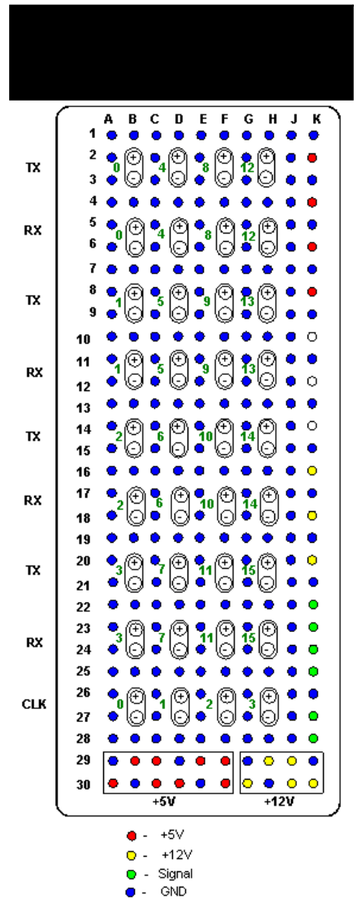


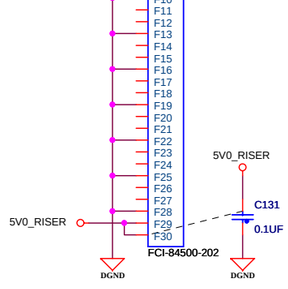


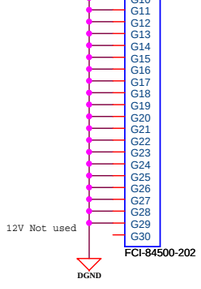


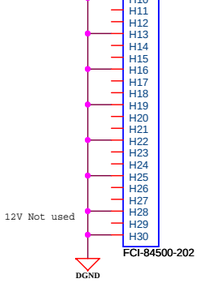


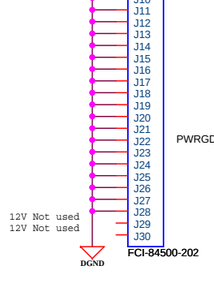


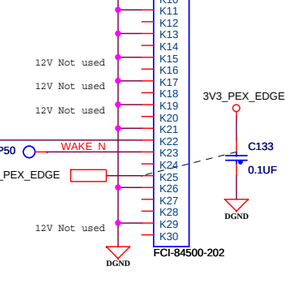


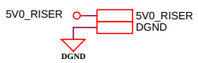








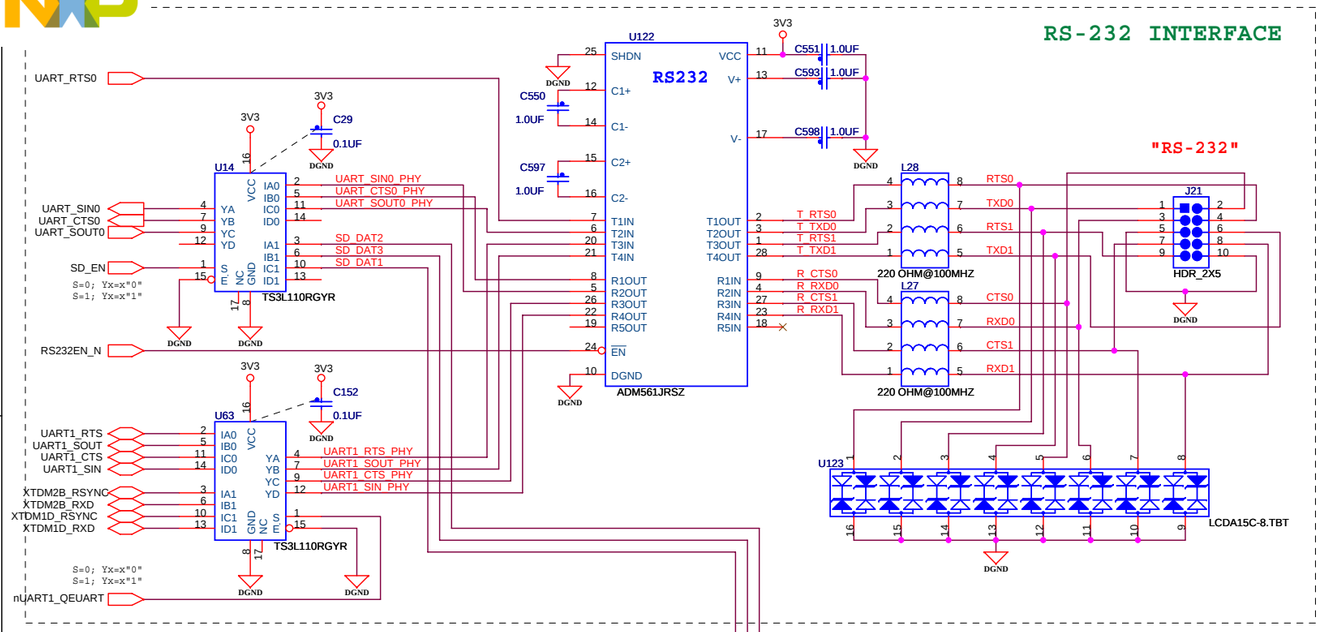


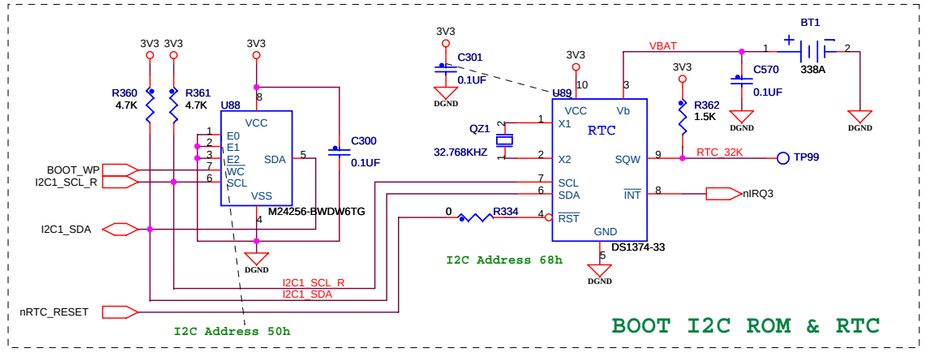


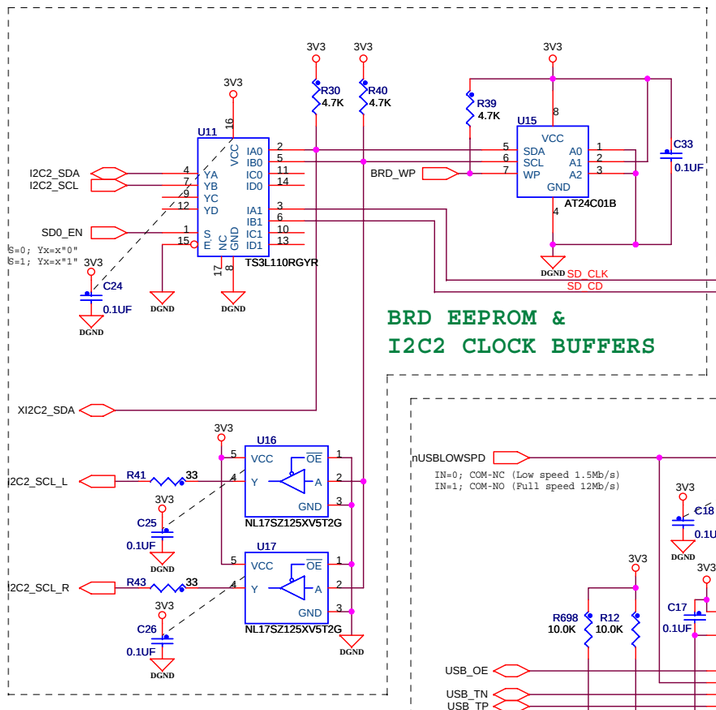
Preliminary – subject to change

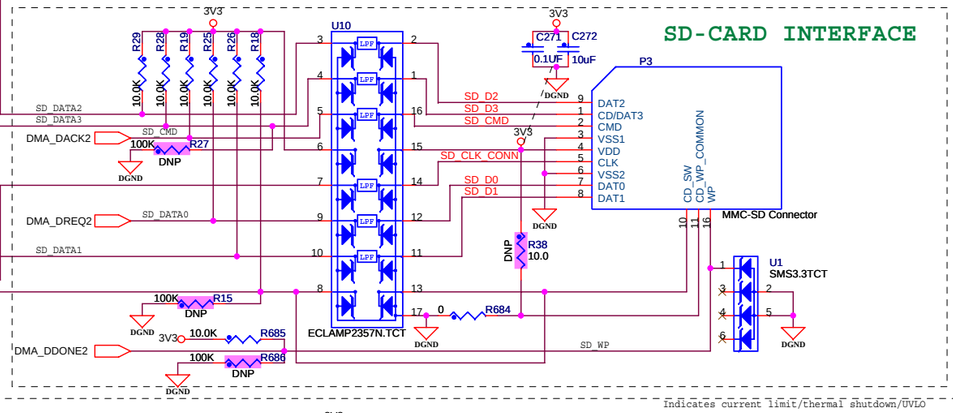
MPC8569E-MDS-PB (Riser Connector RR)		
Size C	Document Number 084-00369-2	Rev Pilot
Date: Sunday, March 01, 2009	Sheet 20 of 21	

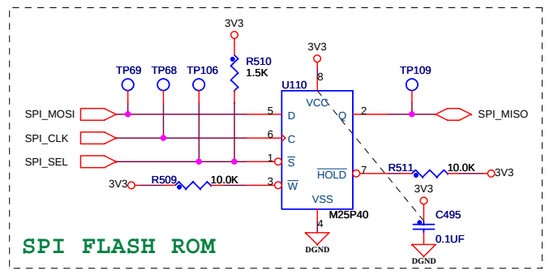
RS-232 INTERFACE

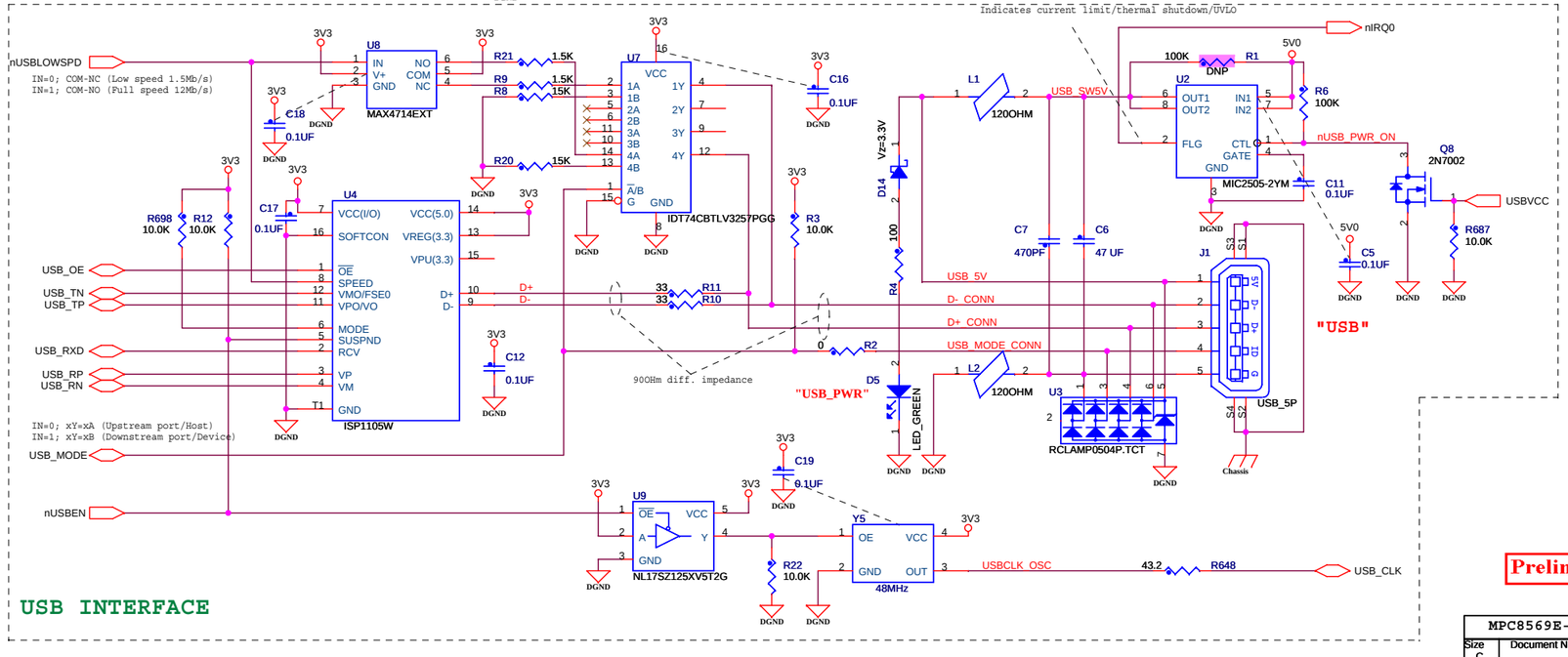












Preliminary – subject to change

MPC8569E-MDS-PB (Serial Interfaces)		
Size C	Document Number 084-00369-2	Rev Pilot
Date: Wednesday, March 04, 2009	Sheet 21 of 21	