

ANI0013-01

Interrupt Control in ISPI181x

Semiconductors

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Application Note Rev. 1.0

Note: ISPI181x denotes the ISPI181, the ISPI181A and the ISPI181B.

Revision History:

| Version | Date | Descriptions | Author |
|---------|----------|--------------|-----------|
| 1.0 | Aug 2002 | First draft. | Alvin Lim |

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1. Introduction

This application note explains the behavior of the interrupt logic in ISPI181x. Therefore, the Interrupt Enable Register, the Interrupt Register and the INTENA bit (present in the Mode Register) that affect the interrupt logic will be discussed.

2. Interrupt Enable Register

The Interrupt Enable Register is used to individually enable or disable interrupts from all endpoints, as well as interrupts caused by events on the USB bus. That is, if an interrupt event occurs while the interrupt is not enabled, nothing will be seen on the interrupt pin. Even if you then enable the interrupt during the interrupt event, there will still be no interrupt seen on the interrupt pin, see Figure 2-1.

The Interrupt Register will not register any interrupt, if it is not already enabled using the Interrupt Enable Register. The Interrupt Enable Register is not an Interrupt Mask Register.

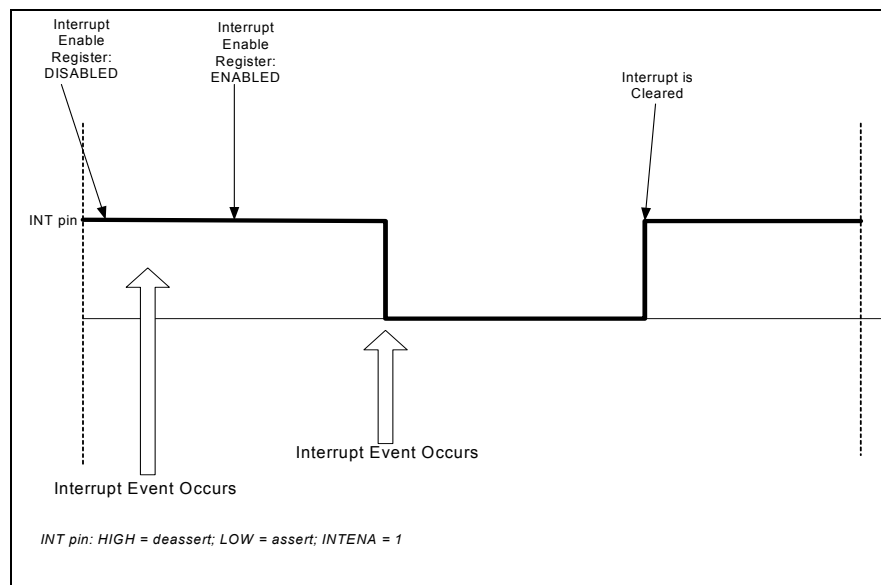


Figure 2-1: Interrupt Pin Waveform

3. Interrupt Register

The Interrupt Register informs the microcontroller or microprocessor about the interrupt events that occur on the various endpoints of ISPI 181x, as well as different bus conditions (for example, BUS RESET, SUSPEND and SOF). When an Interrupt Register bit is 1, it indicates an interrupt has occurred because of the corresponding event.

Table 3-1: Interrupt Register

| | | | | | | | | |
|---------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
| Bit | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 |
| Symbol | reserved | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R | R | R | R | R | R |
| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
| Symbol | EP14 | EP13 | EP12 | EP11 | EP10 | EP9 | EP8 | EP7 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R | R | R | R | R | R |
| Bit | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| Symbol | EP6 | EP5 | EP4 | EP3 | EP2 | EP1 | EP0IN | EP0OUT |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R | R | R | R | R | R |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Symbol | BUSTATUS | SP_EOT | PSOF | SOF | EOT | SUSPND | RESUME | RESET |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Access | R | R | R | R | R | R | R | R |

4. INTENA Bit

The INTENA bit in the Mode Register is a global interrupt enable or disable bit. The behavior of this bit is given in Figure 4-1.

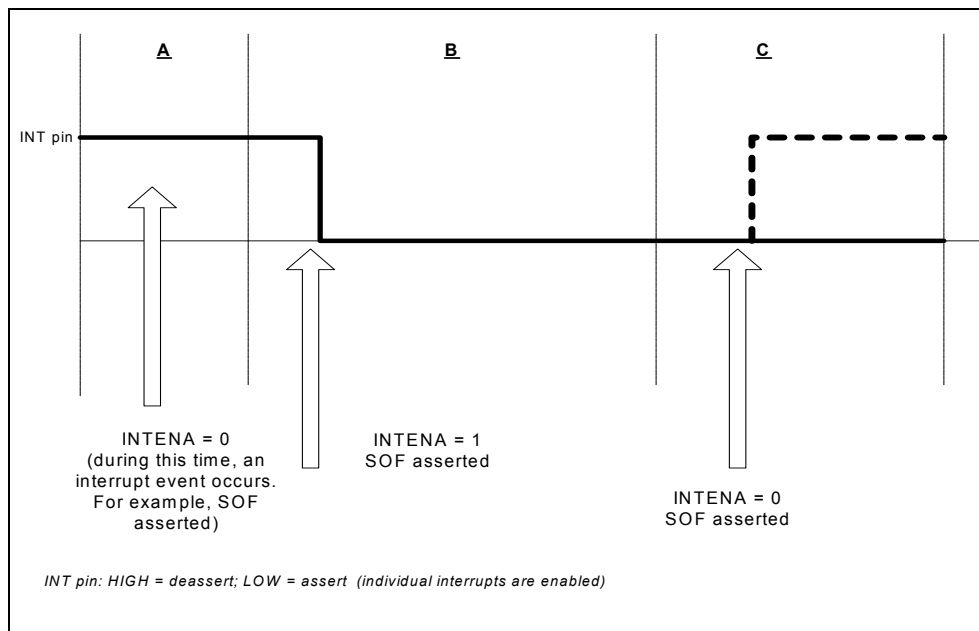


Figure 4-1: Behavior of the INTENA Bit

Event A (see Figure 4-1): When an interrupt event occurs (for example, SOF interrupt) with the INTENA bit set to logic 0, an interrupt will not be generated at the INT pin. However, it will be registered in the corresponding interrupt register bit.

Event B (see Figure 4-1): When the INTENA bit is set to logic 1, the INT pin is asserted because the SOF bit in the Interrupt Register is already asserted.

Event C (see Figure 4-1): If the firmware sets the INTENA bit to logic 0, the INT pin will still be asserted. The bold dashed line shows the desired behavior of the INT pin.

Deassertion of the INT pin can be achieved in the following manner. Interrupt Register bits[23:8] are endpoint interrupts. These interrupts are cleared on reading their respective Endpoint Status Register. Interrupt Register bits[7:0] are bus status and EOT interrupts that are cleared on reading the interrupt register. Make sure that the INTENA bit is set to logic 1 when you perform the clear interrupt commands.

5. References

- *Universal Serial Bus Specification Rev. 2.0* (full-speed and low-speed)
- *ISPI181x full-speed Universal Serial Bus interface device datasheet*.

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