AN10057

Interfacing the ISP1582/3 to the MCF5249 ColdFire processor

Rev. 04 — 18 October 2007 **Application note**

Document information

Info	Content
Keywords	isp1582, isp1583, usb, universal serial bus
Abstract	This application note explains interfacing the ISP1582/3 in generic processor mode to the MCF5249 ColdFire processor.

Revision history

Rev	Date	Description
04	20071018	Fourth release. Corrected processor name to MCF5249 in page headers. Updated Fig 1, Fig 2 and Section 4. Removed previous Fig 4 "Glue logic between the ISP1582/3 and the MCF5249 ColdFire processor". Added Section 5 and Section 6.
03	20060906	Third release. Updated Section 3.
02	20060320	Second release. Table 1 changed ISP1563 to ISP1583.
01	20051205	First release.

Contact information

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1. Introduction

This document explains the interfacing of the ISP1582 and the ISP1583 in generic processor mode to the MCF5249 ColdFire processor.

2. Generic processor mode vs. split bus mode

Unlike the ISP1582, the ISP1583 has two types of bus configurations, generic processor mode and split bus mode, which are selected using pin BUS_CONF at power up.

Table 1 shows the differences between the two types of bus configurations.

Table 1. Generic processor mode vs. split bus mode (only for the ISP1583)

Generic processor mode	Split bus mode
AD[7:0]: 8-bit address bus (selects target register)	**AD[7:0]**: 8-bit local microprocessor bus (multiplexed address and data)
DATA[15:0]: 16-bit data bus (shared by the processor and Direct Memory Access (DMA))	**DATA[15:0]**: 16-bit DMA data bus
Control signals: RW_N and DS_N or RD_N and WR_N (selected using pin MODE0), CS_N	**Control signals**: CS_N, ALE or A0 (selected using pin MODE1), RW_N and DS_N or RD_N and WR_N (selected using pin MODE0)
DMA interface (generic slave mode only): Uses lines DATA[15:0] as data bus, DIOR and DIOW as dedicated read and write strobes	**DMA interface** (master or slave mode): Uses DIOR and DIOW as dedicated read and write strobes

Table 2 shows how the main pin signals, such as BUS_CONF, MODE1 and ALE/A0, are handled in the two types of bus configurations. These pins are applicable only to the ISP1583.

Table 2. Pin configuration for generic processor and split bus modes (only for the ISP1583)

Pin name	Generic processor mode	Split bus mode
BUS_CONF	BUS_CONF = HIGH	BUS_CONF = LOW
MODE1 (used in split bus mode only)	MODE1 = HIGH	**MODE1 = LOW**: ALE function (address latch enable) **MODE1 = HIGH**: A0 function (address or data indicator)
ALE/A0	Pin ALE/A0 must be pulled down using a 10 kΩ resistor	**Address latch enable input**: When pin MODE1 = LOW during power-up, a falling edge latches the address on the multiplexed address and data bus AD[7:0]. **Address and data selection input**: When pin MODE1 = HIGH during power up, the function is determined by the level on this pin (detected on the rising edge of the WR_N pulse). • **HIGH**: Bus AD[7:0] is a register address. • **LOW**: Bus AD[7:0] is register data; used in split-bus mode only.

3. Interfacing block diagram

The main interfacing signals that must be handled on the ISP1582/3 are DATA[15:0], A[7:0] (ISP1582 address bus) or AD[7:0] (ISP1583 address bus), CS_N, RD_N and WR_N. Additionally, for the ISP1583, signals, such as ALE/A0, MODE0, MODE1 and BUS_CONF, must also be properly handled.

Fig 1 shows the block diagram to interface the ISP1582 to the MCF5249 ColdFire processor.

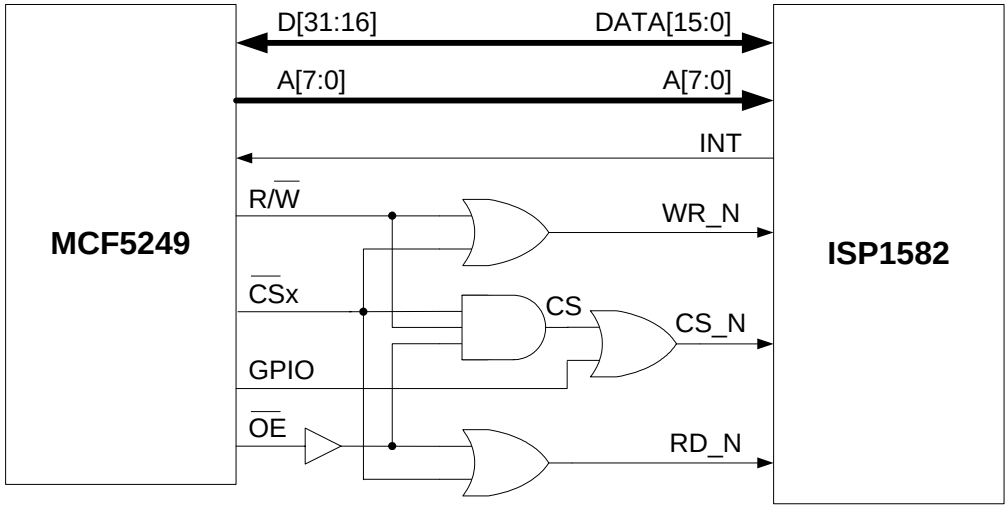


Fig 1. Interfacing the ISP1582 to the MCF5249 ColdFire processor

Fig 2 shows the block diagram to interface the ISP1583 to the MCF5249 ColdFire processor.

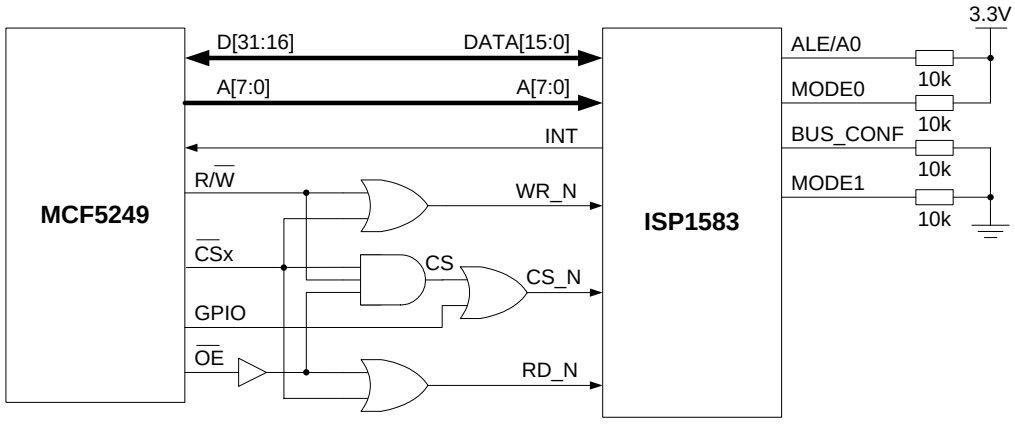


Fig 2. Interfacing the ISP1583 to the MCF5249 ColdFire processor

4. Handling signals CSx_N and R/W_N

The MCF5249 ColdFire processor write access is performed so that the chip select signal (CSx_N) is asserted after the write signal (R/W_N), which is the opposite of the way it works in the ISP1582/3. That is, in the ISP1582/3, the chip select signal (CS_N) must be asserted before the write signal (WR_N). Therefore, additional logic gates are required to correctly assert these signals at the ISP1582/3.

Fig 3 shows write access signals CSx_N and R/W_N of the MCF5249 ColdFire processor.

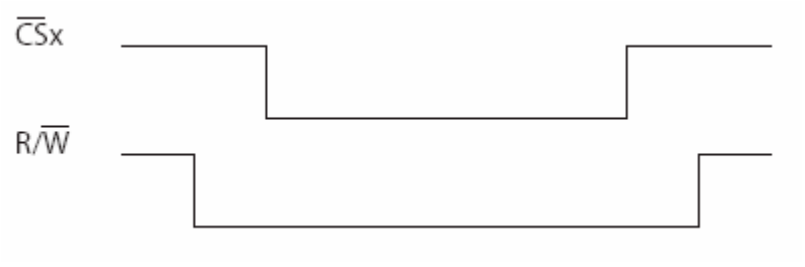
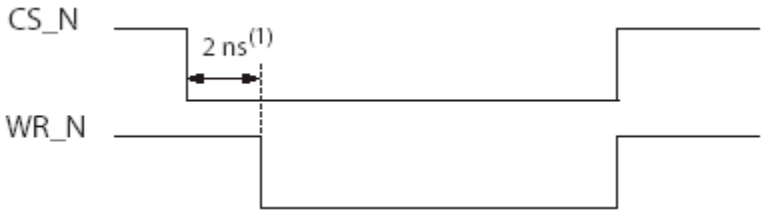


Fig 3. Write access signals of the MCF5249 ColdFire processor

An AND operation is performed on signals CSx_N and R/W_N to ensure that CS_N is asserted before WR_N. Similarly, an OR operation is performed on signals CSx_N and R/W_N to ensure that WR_N is not asserted later than CS_N.

Fig 4 shows the resultant CS_N and WR_N signals after passing through the logic gates.



Propagation delay depends on the gate selected.

(1) It is mandatory to have the WR_N assert 2 ns after the CS_N assert.

Fig 4. Resultant signals CS_N and WR_N after passing through the glue logic

5. Handling signals CSx_N and OE_N

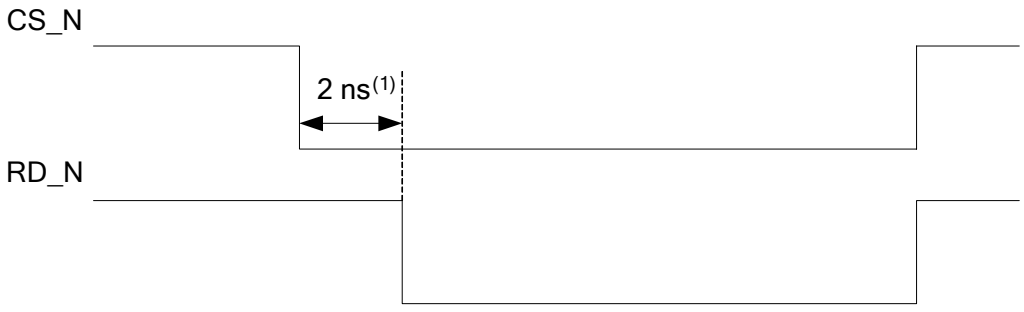
When an MCF5249 ColdFire processor read access is performed, the Chip Select signal (CSx_N) is asserted together with the Read signal (OE_N). In the ISP1582/3, the Chip Select signal (CS_N) must be asserted before the Read signal (RD_N). Therefore, additional logic gates are required to correctly assert these signals in the ISP1582/3.

Fig 5 shows the read access signals CSx_N and OE_N of the MCF5249 ColdFire processor.

Fig 5. Read access signals of the MCF5249 ColdFire processor

A buffer is added on the OE_N signal to delay it. After that, an AND operation is performed on signals CSx_N and OE_N to make sure that CS_N is asserted before RD_N. Similarly, an OR operation is performed on signals CSx_N and OE_N to make sure that RD_N is not asserted later than CS_N.

Fig 6 shows the resultant CS_N and RD_N signals after passing through the logic gates.



Propagation delay depends on the gate selected.

(1) It is mandatory to have the RD_N assert 2 ns after the CS_N assert.

Fig 6. Resultant signals CS_N and RD_N after passing through the glue logic

6. Handling ISP1582/3 CS_N

In most systems, the control bus of read and write signals is shared. Therefore, we perform an OR operation on the GPIO and CS signals to make sure that CS_N is asserted only when the read or write access is meant for ISP1582/3.

- When GPIO = '0', the read or write access is meant for ISP1582/3. Therefore, assert CS_N.
- When GPIO = '1', the read or write access is not meant for ISP1582/3. Therefore, do not assert CS_N.

Fig 7 shows the resultant CS_N passing through logic gates.

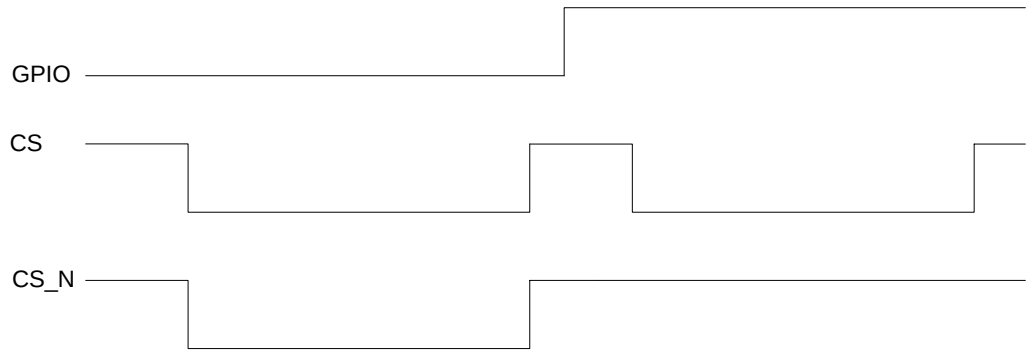


Fig 7. ISP1582/3 Chip Select (CS_N) signal

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