

# AN10066

## Interfacing to the ISP1508

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Application note

### Document information

Info	Content
<b>Keywords</b>	isp1508; isp1508a; isp1508b; usb; ulpi; universal serial bus; transceiver; utmi+ low-pin interface; host; peripheral; otg; phy
<b>Abstract</b>	This application note describes how a link can interface to the ISP1508 for host, peripheral or OTG applications.

**Revision history**

Rev	Date	Description
01	20080122	First release.

**Contact information**

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## 1. Introduction

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The ISP1508 is a High-Speed (HS) UTMI+ Low Pin Interface (ULPI) transceiver that provides great flexibility to interface to a link for USB applications. The ISP1508 also supports transparent UART mode.

This document describes how a link can interface to the ISP1508 for host, peripheral or OTG applications. This document includes PCB design guidelines as well.

## 2. Interfacing to the ISP1508

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### 2.1 ULPI interface clock

The ULPI interface is a synchronous interface. All the data transactions on the ULPI bus are synchronized to the rising edge of 60 MHz clock signal for SDR, and both the rising and falling edges of the clock for DDR. The 60 MHz is supplied by the ISP1508 (called output clock mode).

When a crystal is attached between the XTAL1 and XTAL2 pins, or a square wave clock of the same frequency is driven into XTAL1, the ISP1508 will output 60 MHz clock on the CLOCK pin.

The crystal or clock frequencies supported by the ISP1508 are 13 MHz, 19.2 MHz, 24 MHz and 26 MHz. The frequency selection is done using the CFG1 and CFG2 input pins. When a clock is driven into XTAL1, XTAL2 must be left unconnected.

In low-power mode, the clock driven into XTAL1 can be stopped to save power. When the clock is stopped, the clock driver may either drive a LOW or 3-state the clock output buffer. Otherwise, leakage current will be drawn by XTAL1, if a HIGH is driven on the XTAL1 pin. The clock must be started before asserting STP to wake up from low-power mode.

In power-down mode, the clock driven into XTAL1 can also be stopped to save power. When the clock is stopped, the clock driver may either drive a LOW or 3-state the clock output buffer. Otherwise, leakage current will be drawn by XTAL1, if a HIGH is driven on the XTAL1 pin.

### 2.2 UART mode

Before entering UART mode, 1.5 k $\Omega$  pull-up resistor on DP and 15 k $\Omega$  pull-down resistors on both DP and DM must be disabled, that is, the DP\_PULLDOWN, DM\_PULLDOWN and TERMSELECT register bits must be cleared.

Low-speed driver must be utilized whenever possible. The rise time and fall time for low-speed driver is around 200 ns, which will cause less reflection and overshoot, improving EMI performance.

It is recommended that you de-assert and assert CHIP\_SEL to exit UART mode. The ISP1508 must be de-selected for a minimum of 100 ms so that the chip completely enters power-down mode.

Alternatively, the link can assert STP to wake up the ISP1508 from UART mode. RXCMDs must not be interpreted, before re-configuring the ISP1508 as host or peripheral and setting the RESET register bit.

### 3. PCB design guidelines

This section describes the PCB design guidelines that **must** be followed to achieve high-speed signal quality.

- The PCB routing for the DP and DM lines must follow *High Speed USB Platform Design Guidelines Rev.1.0*, to achieve high-speed signal quality.
- The crystal must be connected as close as possible to the XTAL1 and XTAL2 pins of the transceiver, if used. Loops must be made as small as possible to keep noise coupled in through the PCB low.
- The 12 k $\Omega$   $\pm$  1 % reference resistor must be placed closed to the RREF pin and the other terminal is preferably via to the ground layer directly.
- Filtering capacitors connected to internal regulator outputs must have low ESR.
- Generally, ULPI interface pins can directly be routed to the link. A series termination resistor may be added to the clock line to attenuate reflection and ringing that cause EMI problems.
- Bypass capacitors for power supplies must be placed close to the transceiver. Ferrite beads can be used to filter supplies to the transceiver, if the system supply is too noisy. Ferrite beads used in the application can be between 50  $\Omega$  and 120  $\Omega$  at 100 MHz, with current rating of about 200 mA.
- It is recommended that you add ferrite beads on  $V_{BUS}$  and ground pins of the USB connector to suppress conducted emission.
- It is strongly recommended that you add ESD protection to the DP, DM,  $V_{BUS}$  and ID pins. Note that only ESD diodes specifically designed for high-speed data lines or USB applications must be used. NXP recommends the IP4359 part for ESD protection. PCB designers must ensure that high-speed signal quality is not degraded by the ESD diode.

### 4. Abbreviations

**Table 1. Abbreviations**

Acronym	Description
DDR	Double Data Rate
EMI	ElectroMagnetic Interference
ESD	ElectroStatic Discharge
ESR	Equivalent Series Resistance
HS	High-Speed
PCB	Printed-Circuit Board
RXCMD	Receive Command
SDR	Single Data Rate
TXCMD	Transmit Command
UART	Universal Asynchronous Receiver-Transmitter

Acronym	Description
ULPI	UTMI+ Low Pin Interface
USB	Universal Serial Bus

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