

# ERRATA SHEET

**Date:** February 27, 2006  
**Document Release:** Version 1.1  
**Device Affected:** LPC2102

This errata sheet describes both the functional deviations and any deviations from the electrical specifications known at the release date of this document.

Each deviation is assigned a number and its history is tracked in a table at the end of the document.

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**Identification:**

The LPC2102 devices typically have the following top-side marking:

LPC2102xxx

xxxxxxx

xxYYWW R

The last letter in the third line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the LPC2102:

Revision Identifier (R)	Comment
-	Initial device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

## Functional Deviations of LPC2102

### Core.1 Incorrect update of the Abort Link register in Thumb state

**Introduction:** If the processor is in Thumb state and executing the code sequence STR, STMIA or PUSH followed by a PC relative load, and the STR, STMIA or PUSH is aborted, the PC is saved to the abort link register.

**Problem:** In this situation the PC is saved to the abort link register in word resolution, instead of half-word resolution.

**Conditions:**

The processor must be in Thumb state, and the following sequence must occur:

<any instruction>

<STR, STMIA, PUSH> <---- data abort on this instruction

LDR rn, [pc,#offset]

In this case the PC is saved to the link register R14\_abt in only word resolution, not half-word resolution. The effect is that the link register holds an address that could be #2 less than it should be, so any abort handler could return to one instruction earlier than intended.

**Work around:** In a system that does not use Thumb state, there will be no problem.

In a system that uses Thumb state but does not use data aborts, or does not try to use data aborts in a recoverable manner, there will be no problem.

Otherwise the workaround is to ensure that a STR, STMIA or PUSH cannot precede a PC-relative load. One method for this is to add a NOP before any PC-relative load instruction. However this is would have to be done manually.

### MAM.1 Incorrect read of data from SRAM after Reset and MAM is not enabled or partially enabled

**Introduction:** The Memory Accelerator Module (MAM) provides accelerated execution from the on-chip flash at higher frequencies.

**Problem:** If code is running from on-chip Flash, a write to an SRAM location followed by an immediate read from the same SRAM location corrupts the data been read. For instance, a stack push operation immediately followed by a stack pop operation

**Work-around:** User code should enable the MAM after Reset and before any RAM accesses; this means MAMTIM and MAMCR should be set as follows:

**MAMTIM:** For CPU clock frequencies slower than 20MHz, set MAMTIM to 0x01. For CPU clock frequencies between 20MHz and 40MHz, set MAMTIM to 0x02, and for values above 40MHz set MAMTIM to 0x03.

**MAMCR:** Set MAMCR to 0x02 (MAM functions fully enabled)

MAMTIM should be written before MAMCR.

### SPI.1 Incorrect shifting of data in slave mode at lower frequencies

**Introduction:** In slave mode, the SPI can set the clock phase (CPHA) to 0 or 1.

**Problem:** Consider the following conditions:

- a. SPI is configured as a slave (with CPHA=0).
- b. SPI is running at a low frequency.

In slave mode, the SPIF (SPI Transfer Complete Flag) bit is set on the last sampling edge of SCK. If CPHA is set to 0 then the last sampling edge of SCK would be the rising edge.

Under the above conditions, if the SPI Data Register (SPDR) is written to less than a half SCLK cycle after the SPIF bit is set (this would happen if the SPI frequency is low) then the SPDR will shift data one clock early for the upcoming transfers.

Lowering the SPI frequency would increase the likelihood of the SPDR write happening in the first half SCK cycle of the last sampling clock.

Work-around: There are two possible workarounds:

- 1) Use CPHA=1.
- 2) If the data is shifted incorrectly when CPHA is set to 0 then delaying the write to SPDR after the half SCK cycle of the last sampling clock would resolve this issue.

### **SSP.1 Initial data bits/clocks of the SSP transmission are shorter than subsequent pulses at higher frequencies**

Introduction: The SSP is a Synchronous Serial Port (SSP) controller capable of operation on a SPI, 4-wire SSI or a Microwire bus. The SSP can operate at a maximum speed of 30MHz and it referred to as SPI1 in the device documentation.

Problem: At high SSP frequencies, it is found that the first four pulses are shorter than the subsequent pulses.

At 30MHz, the first pulse can be expected to be approximately 10ns shorter and the second pulse around 5ns shorter. The remaining two pulses are around 2ns shorter than subsequent pulses.

At 25MHz, the length of the first pulse would be around 7ns shorter. The subsequent three pulses are around 2ns shorter.

At 20MHz only the first pulse is affected and it is around 2ns shorter. All subsequent pulses are fine.

The deviation of the initial data bits/clocks will decrease as the SSP frequency decreases.

Work-around: None.

### **Timer.1 In counter mode, the Timer Counter reset does not occur on the correct incoming edge**

Introduction: Timer0 and Timer1 can be used in a counter mode. In this mode, the Timer Counter register can be incremented on rising, falling or both edges which occur on a selected CAP input pin.

This counter mode can be combined with the match functionality to provide additional features. One of the features would be to reset the Timer Counter register on a match. The same would also apply for Timer1.

Problem The Timer Counter reset does not trigger on the same incoming edge when the match takes place between the corresponding Match register and the Timer Counter register. The Timer Counter register will be reset only on the next incoming edge.

Work-around: There are two possible workarounds:

1. Combine the Timer Counter reset feature with the "interrupt on match" feature. The interrupt on match occurs on the correct incoming edge. In the ISR, the Timer Counter register can also be reset. This solution can only work if no edges are expected during the duration of the ISR.

2. In this solution, the "interrupt on match" feature is not used. Instead, the following specific initialization can achieve the counting operation:

- a. Initialize the Timer Counter register to 0xFFFFFFFF.

- b. If "n" edges have to be counted then initialize the corresponding Match register with value n-1. For instance, if 2 edges need to be counted then load the Match register with value 1

More details on the above example:

- a. Edge 1- Timer overflows and Timer Counter (TC) is set to 0.
- b. Edge 2- TC=1. Match takes place.
- c. Edge 3- TC=0.
- d. Edge 4- TC=1. Match takes place.
- e. Edge 5- TC=0.

**Vdd.1      Device may not work properly under increased power consumption conditions**

**Introduction:** From the Vdd<sub>1V8</sub> pin to the ARM7 core, there is a voltage drop. This voltage drop increases with higher currents (or higher power consumption). Higher system frequency and/or faster peripherals increase power consumption thereby increasing the voltage drop from the Vdd<sub>1V8</sub> pin to the core.

**Problem:** Under increased power consumption conditions, the device may not work properly. The likelihood of the problem showing up increases if the device is run at higher speeds (approaching 70MHz) and/or if the peripherals are running at close to system frequency speed (i.e If the APBDIV register is set to a value lower than 4 which would imply that the peripherals are run faster than 1/4 of the system frequency).

Also, having a lower voltage on Vdd<sub>1V8</sub> pin (e.g. below 1.8V) can cause this issue to surface.

**Work-around:** Increase the voltage on Vdd<sub>1V8</sub> to 1.95V. It is not harmful to the device if this voltage reaches 2V.

**Electrical and Timing Specification Deviations of the LPC2102**

- ESD.1:** Philips Quality Spec specifies ESD-HBM should be above 2.0 kV. The LPC2102 passed ESD-HBM Stress up to 2.5kV but without VDD-to-VDD zapping (e.g. Vref to VBat, or Vref to V3A). Units zapped according to JEDEC Standard (JESDA22-A114-B) did not pass the ESD Post Stress Test.

**Errata History - Functional Problems**

Functional Problem	Short Description	Errata occurs in device revision
Core.1	Incorrect update of the Abort link register	-
MAM.1	Incorrect read of data from SRAM	-
SPI.1	Incorrect shifting of data in slave mode at lower frequencies	-
SSP.1	Initial data bits/clocks corrupted in SSP transmission	-
Timer.1	Timer Counter reset occurs on incorrect edge in counter mode	-
Vdd.1	Device may not work properly under increased power consumption	-

**Errata History - Electrical and Timing Specification Deviations**

AC/DC Deviations	Short Description	Errata occurs in device revision
ESD.1	ESD-HBM Stress issue	-