

ERRATA SHEET

Date: April 17, 2002
Document Release: Version 1.0
Devices Affected: P87LPC768

This errata sheet describes both the functional deviations and any deviations from the electrical specifications known at the release date of this document.

Each deviation is assigned a number and its history is tracked in a table at the end of the document.

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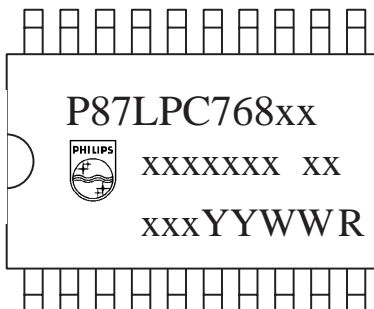
Low pincount 8-bit microcontroller

Errata Sheet

P87LPC768

IDENTIFICATION:

The typical P87LPC768 devices have the following top-side marking (SO 20 package shown):



The last letter in the third line (field 'R') will identify the device revision. This Errata Sheet covers the following revisions of the P87LPC768:

Revision Identifier (R)	Comment
no revision letter or dash ('-')	Initial device revision

Field 'YY' states the year the device was manufactured. Field 'WW' states the week the device was manufactured during that year.

FUNCTIONAL DEVIATIONS OF P87LPC768

PWM.1: PWM Brake release functionality

Introduction: When a Brake condition is asserted, the PWM channels go to their fixed Brake state set in register PWMCON1.

Problem: If the brake signal is released, the PWM channels do not stay in the Brake state but rather return to the state the PWM channels had before the Brake was asserted. Although this is how the functionality is described in the data sheet, this behavior is not desirable because it can cause problems in the application.

Workaround: None.

PWM.2: Ineffective PWM shadow register transfer during PWM counter underflow

Introduction: The PWM module contains a counter reload register and four compare registers, each of which are equipped with a shadow register. To update the current PWM signals, the user software writes the new values to the shadow registers and sets the XFER bit in register PWMCON1 to 1. With the next underflow of the PWM counter, the values in the shadow registers get transferred into the corresponding active registers, resulting in the desired change in the PWM signals. The XFER bit automatically gets cleared by hardware and remains 0 until the next update request.

Problem: If the software attempts to set the XFER bit to 1 at the same time an underflow of the PWM counter occurs, the XFER bit remains 0 and the values in the shadow registers do not get transferred to the corresponding active registers.

Workaround: Set the XFER bit to 1 twice in a row to ensure the values in the shadow registers get transferred into the corresponding active registers.

PWM.3: PWM pins stuck to low level if ports are configured to be low after reset in UCFG1

Introduction: Bit 5 of User Configuration Byte 1 (UCFG1.5; bit PRHI) is used to select whether the port pins of the P87LPC768 will be in a low state or a high state after reset.

Problem: If the port pins are configured to be low during and after reset (bit PRHI = 0), the port pins which have the PWM channels as an alternate function will stay low even when they are configured to output high level by software after the device reset sequence. The port pins affected are:

- P0.0 / PWM3
- P0.1 / PWM0
- P1.6 / PWM1
- P1.7 / PWM2

Workaround: To avoid these pins to be stuck to 0 after reset, configure bit PRHI in register UCFG1 to 1. Please note that all port pins will then be in a high state after reset. After the reset sequence, 0's can be written to the port pins that need to be low.

PWM.4: PWM still running after breakpoint was hit during emulation

Problem: While emulating the P87LPC768, the PWM module does not stop when a breakpoint is asserted. In addition, because the PWM block is switched to the internal ~6 MHz clock when a breakpoint is hit, all PWM signals will be generated based on the internal ~6 MHz clock.

Workaround: None.

PWM.5: PWM does not run in Idle mode

Problem: When the P87LPC768 is put in Idle mode the PWM module stops running.

Workaround: None. To keep the PWM block running don't use Idle or Powerdown mode.

ELECTRICAL AND TIMING SPECIFICATION DEVIATIONS OF P87LPC768

No known deviations at the release of this document.

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ERRATA HISTORY - FUNCTIONAL PROBLEMS

Functional Problem	Short Description	fixed?	problem fixed in device revision
PWM.1	PWM Brake release functionality	no	
PWM.2	Ineffective PWM shadow register transfer during PWM counter underflow	no	
PWM.3	PWM pins stuck to low level if ports are configured to be low after reset in UCFG1	no	
PWM.4	PWM still running after breakpoint was hit during emulation	no	
PWM.5	PWM does not run in Idle mode	no	

ERRATA HISTORY - AC/DC DEVIATIONS

AC/DC Deviation	Short Description	problem occurs in device revision
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