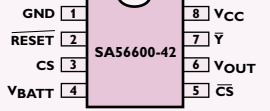
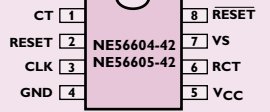
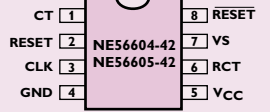
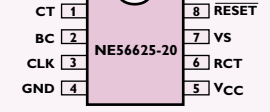
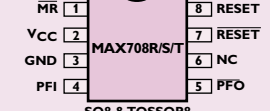
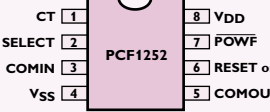
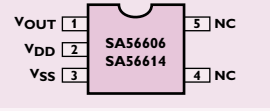
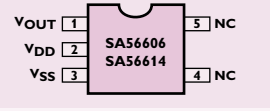
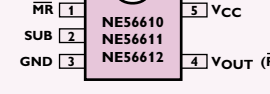


Microprocessor Supervisory and System Reset Selector Guide

Devices	Package Pinout	RESET (Note 1)	$\overline{\text{RESET}}$ (Note 2)	Output Configuration	VS Thresholds	POR Delay Time	Hysteresis	Special Features/ Direct Replacement
SA56600-42	System Reset for Lithium Battery Backup 		x	NPN Open Collector	4.2 V	8 ns	200 mV	Lithium Battery Backup (BATT) SRAM Controller (CS, CS)
NE56604-42	Resets with Built-in Watchdog Timer 	x	x	NPN Open Collector	4.2 V Adjustable 3 to 5 V	Adjustable 1 ms to 10 s	100 mV	Watchdog Timer Adjustable 1 ms to 10 s
NE56605-42	Resets with Built-in Watchdog Timer 							Watchdog Timer Adjustable 1 ms to 100 ms
NE56625-20	Reset with Built-in Watchdog Timer 		x	NPN Open Collector	2.0 V Adjustable 1.65 V to 3.0 V	Adjustable 10 ms to 10 s	100 mV	Watchdog Timer Adjustable 10 ms to 10 s Battery Check Active-LOW Output (BC), 2.2 V threshold
MAX708	3 V μ P Reset with PF Comparator & Manual Reset 	x	x	N-Ch/P-ch Push-pull	2.63, 2.93, 3.08 V	200 ms	20 mV	Power Fail indicator (PFI, $\overline{\text{PFO}}$) Manual Reset (MR)/MAX708
PCF1252	Threshold Detector & Reset 	x (Note 3)	x (Note 3)	N-Ch/P-ch Push-pull	2.55, 2.75, 3.05, 3.25, 3.55, 3.75, 4.05, 4.25, 4.55, 4.75 V	Adjustable 100 μ s to 1 s	30 mV	Comparator (COMIN, COMOUT) Power Fail ($\overline{\text{POWF}}$)
SA56606	CMOS System Resets 		x	N-ch Open Drain	2, 2.7, 2.8, 2.9, 3, 3.1, 4.2, 4.3, 4.4, 4.5, 4.7 V	400 μ s	100 mV	NCP301
SA56614	CMOS System Resets 		x	N-Ch/P-ch Push-pull				NCP300
NE56610	System Resets 		x	NPN Open Collector	2.5, 2.7, 2.9, 3.9, 4.2, 4.5 V	50 ms	60 mV	Manual Reset ($\overline{\text{MR}}$)
NE56611						100 ms		
NE56612						200 ms		

Microprocessor Supervisory and System Reset Selector Guide

Devices	Package Pinout	RESET (Note 1)	RESET (Note 2)	Output Configuration	VS Thresholds	POR Delay Time	Hysteresis	Special Features/ Direct Replacement
SA56615	CMOS Resets with Adjustable Delay Time		x	N-ch Open Drain	0.9, 1.8, 1.9, 2, 2.7, 2.9, 3, 3.1, 4.2, 4.3, 4.4, 4.5, 4.6, 4.7 V	Adjustable 200 ns to 800 µs	VS x 0.05	NCP303, MC33465, MAX6425, S809xxANMP, RN5VDxxAx
SA56616			x	N-Ch/ P-ch Push-pull				NCP302, MC33464, MAX6424, S809xxALMP, RN5VDxxCx
NE56631	Active-LOW System Reset		x	NPN Open Collector	1.9, 2, 2.7, 2.8, 2.9, 3, 3.1, 4.2, 4.3, 4.4, 4.5, 4.6 V	20 µs	50 mV	V-6300
NE56632	System Reset with Adjustable Delay Time		x	NPN Open Collector	1.9, 2, 2.7, 2.8, 2.9, 3, 3.1, 4.2, 4.3, 4.4, 4.5, 4.6 V	Adjustable 200 µs to 200 ms	50 mV	MAX6426UK
MAX809	3-pin µP Reset		x	N-Ch/ P-ch Push-pull	2.32, 2.63, 2.93, 3.08, 4.00, 4.38, 4.63 V	240 ms		MAX809, LM809, FM809
MAX810		x	x	Push-pull	2.2, 2.32, 2.63, 2.93, 3.08 V/	240 ms		MAX810, LM810, FM810
MAX6326/46			x	Push-pull	4.38, 4.63 V	280 ms	6.3 mV/	1 µA I _{DD} /
MAX6328/48			x	N-Ch Open Drain	2.2, 2.32, 2.63, 2.93, 3.08 V/	280 ms	9.5 mV	MAX6326/46, MAX6328/48
MAX6327/47			x	Push-pull	4.38, 4.63 V	280 ms	6.3 mV/	1 µA I _{DD} /
MAX6400/3	Ultra-low-power µP Reset in 4-bump CSP		x	Push-pull	2.2, 2.32, 2.63, 2.93, 3.08 V/	280 ms	6.3 mV/	1 µA I _{DD}
MAX6402/5			x	Open Drain	4.38, 4.63 V		9.5 mV	Manual Reset ($\overline{\text{MR}}$)
MAX6401/4			x	Push-pull				Wafer Level, Chip Scale Package, 4-Bump/MAX6400-MAX6405
MAX6352 (Note 2)	Dual Voltage µP Reset		x	N-Ch Open Drain	V _{DD1} : 4.63, 3.08, 2.93, 2.63 V V _{DD2} : 2.93, 2.32, 2.19, 1.58 V	280 ms	V _{th} /500	Dual voltage microprocessor reset/ MAX6352

- Note 1. Microprocessors with high-active resets: 8xC5x, 8xC3x, 8xC5xX2, 8xC3xX2, 8xC51Fx, 8xC51Rx+, 89C51Rx2, 89C66x, 8xC554, 8xC552, etc.
- Note 2. Microprocessors with low-active resets: All 16-bit devices from XA-family (XA-Cxx, XA-Gxx, XA-Sxx, XA-Hxx), all LPC7xx devices (P87LP760/761/762/767/768/769), P80C591/ P87C591 (with on-chip CAN controller).
- Note 3. Reset output polarity set by Select pin: Select pin high for low-active reset; Select to ground for high-active reset.

