

PCK351 & PCK3807A High-performance LVTTTL Clock Distribution ICs

Philips Semiconductors offers a choice of high-performance LVTTTL clock distribution ICs designed for low-skew distribution of clock signals in medium to high speed platforms such as telecom equipment, base stations, switches and routers. These devices allow the system designer to buffer the main clock source from the variable load conditions of multi-card rack systems, and to drive signals over longer traces—all while maintaining accurate alignment of clock edges as well as preserving duty cycle when fanning out LVTTTL/CMOS clock signals throughout the system.

Features—PCK351

- Supports high clock frequencies of up to 100 MHz
- Low output-to-output skew (<500 ps)
- Low duty cycle distortion (<800 ps)
- Output enable pin disables (high-Z) all outputs simultaneously
- LVTTTL compatible inputs and outputs
- Balanced, high-drive outputs (-32 mA I_{OH} , +32 mA I_{OL})
- Distributed V_{CC} and ground pins minimize switching noise
- Input overvoltage tolerance of 5.5 V
- Operates from 3.3V power supply
- Available in 24-pin SSOP and SO packages

Features—PCK3807A

- Supports high clock frequencies of up to 150 MHz
- Very low output-to-output skew (< 120 ps at 22 pF load)
- Very low duty cycle distortion (< 300 ps)
- LVTTTL compatible inputs and outputs
- Low power consumption (290 mW typ at 100 MHz/22 pF)
- Low input capacitance, 3.0 pF typical
- Distributed V_{CC} and ground pins minimize switching noise
- Input overvoltage tolerance of 5.5 V at 3.3 V supply
- Input overvoltage tolerance of 3.6 V at 2.5 V supply
- Operates from 2.5 V or 3.3 V power supply
- Available in 20-pin SO, SSOP, QSOP and TSSOP packages

Applications

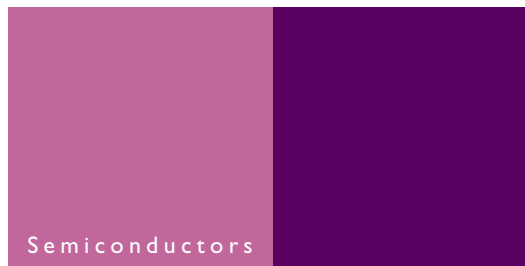
- Low-skew clock distribution
- Data signal distribution
- Telecom, networking and base station infrastructure platforms

Operating Characteristics

- Operation from a single 3.3 V power supply
- PCK3807A also operates from a single 2.5 V power supply
- -40°C to +85°C operating temperature range

Family Overview

Part Number	Function
PCK351	1:10 low-skew LVTTTL clock distribution IC with 3-state output
PCK3807A	1:10 low-skew LVTTTL clock distribution IC



Description

In digital systems involving physically distributed functionality such as multi-card rack systems, clock distribution is a key function and a significant focus of attention in the design. Available timing budgets are directly impacted by uncertainties in the timing of clock edges, such as skew, duty cycle distortion (also referred to as pulse skew) and jitter. Clock fanout buffers offer a simple way of managing skew by a combination of properties: it buffers the input clock source circuitry (making it independent from the variability of multiple clock traces to the receiving devices), produces multiple copies of the input clock signal, and does so while maintaining accurate edge alignment between all of its outputs. In LVTTTL or LVCMOS systems, PCK351 or PCK3807A provide a simple, cost-effective solution to realize fanout buffering at moderate to high clock speeds, with minimal skew.

The PCK3807A offers 1:10 fanout buffering of LVTTTL/CMOS clock signals with guaranteed low skew of less than 120 ps. It operates in 2.5 V as well as 3.3 V applications, extending the applicability of this popular function to new generation low supply voltage platforms. The PCK3807A offers low capacitance inputs, with hysteresis for improved noise margins, and employs multiple power and grounds to reduce noise.

The PCK351 offers 1:10 fanout buffering of LVTTTL/CMOS clock signals, with the additional capability to disable all outputs. In enabled mode, the output drivers produce a balanced drive for both the low and high logic states, which minimizes duty cycle distortion as a function of variable or asymmetrical loading conditions. In disabled (3-state) mode, the outputs are put in a high-impedance state.

The PCK351 is pin-, form-, and function-compatible with CDC351 to allow interchangeability and multiple sourcing of critical functions. The PCK3807A is compatible with the 74FCT3807 series of fanout buffers.

Philips Semiconductors offers a wide range of clock distribution products supporting various frequency ranges and signaling standards. For high-performance LVDS clock distribution, PCK2111 provides 1:10 fanout ratio at up to 800 MHz. For high-performance PECL clock distribution, PCK111, PCK210, PCKEL14 or PCKEP14 may be used.

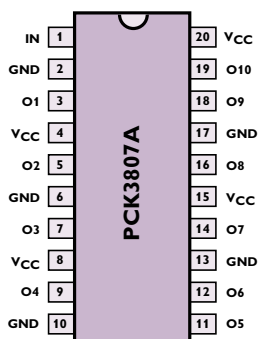
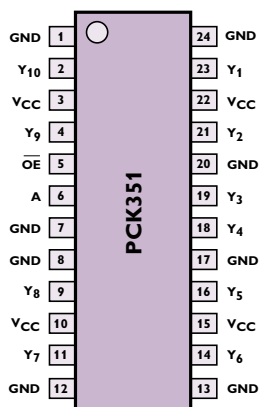
The Philips logo, consisting of the word "PHILIPS" in a bold, blue, sans-serif font.

PCK351 & PCK3807A

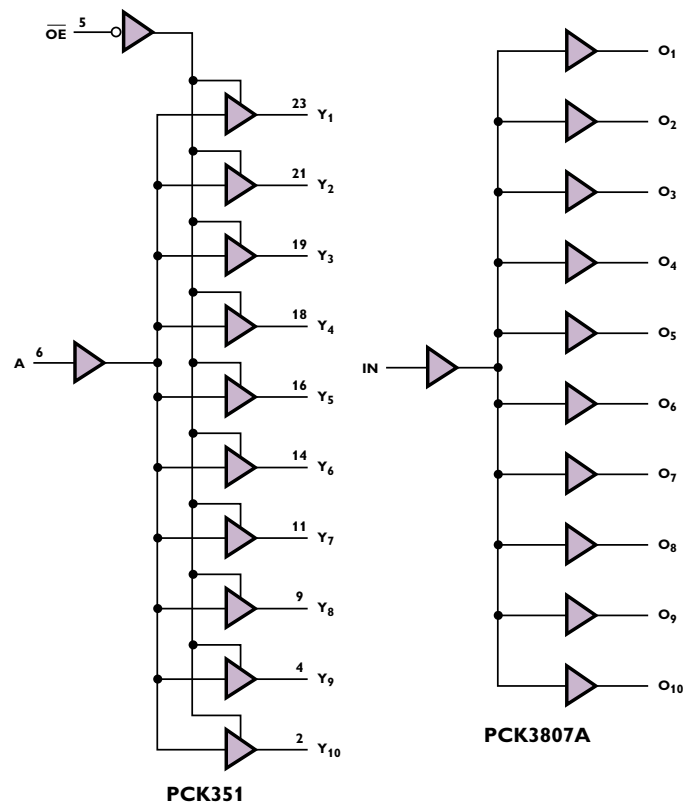
High-performance LVTTTL Clock Distribution ICs



Pin Configurations and Device Selection Table



Functional Block Diagrams



PCK351	PCK3807A
1:10 LVTTTL fan-out	1:10 LVTTTL fan-out
Output enable, 3-state	—
Up to 100 MHz typical clock frequency	Up to 150 MHz typical clock frequency
3.6 ns typical propagation delay	2.5 ns typical propagation delay
< 500 ps skew	< 120 ps skew
<800 ps pulse skew	<300 ps pulse skew
Input overvoltage tolerance	Input overvoltage tolerance
3.3 V supply	2.5 V or 3.3 V supply
Compatible with CDC351	Compatible with 74FCT3807 series

Ordering Information

Package	Container	PCK351	PCK3807A
SO	Tube	PCK351D	PCK3807AD
	Tape & Reel	PCK351D-T	PCK3807AD-T
SSOP	Tube	PCK351DB	PCK3807ADB
	Tape & Reel	PCK351DB-T	PCK3807ADB-T
QSOP	Tube	-	PCK3807ADS
	Tape & Reel	-	PCK3807ADS-T
TSSOP	Tube	-	PCK3807APW
	Tape & Reel	-	PCK3807APW-T

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