

PTN3331/PTN3332/ PTN3341/PTN3342

High-performance LVDS-LVTTL Quad Logic Translator Family

Philips offers a family of high-speed logic translator ICs, providing a solution for logic level translation between LVTTL and LVDS (low-voltage differential signaling). These LVDS drivers and receivers each provide four channels capable of up to 400 Mbit/s signaling rates. These translators allow designs to take advantage of the benefits of LVDS such as low-power, low-EMI and long signaling reach at high signaling speeds, with high common-mode noise immunity over commonly used media.

Family Overview

Part Number	Function
PTN3331	Quad high-speed LVDS line driver for point-to-point LVDS (100 Ω) signaling environments
PTN3341	Quad high-speed LVDS line driver for multi-drop LVDS (50 Ω) signaling environments
PTN3332	Quad high-speed LVDS line receiver
PTN3342	Quad high-speed LVDS line receiver with integrated 100 Ω receiver termination resistor

Features—PTN3331 and PTN3341 LVDS Line Drivers

- Support high data rates of up to 400 Mbit/s
- Four independent channels per IC with common disable
- Low channel skew (<300 ps)
- Low part-to-part skew (<800 ps)
- Propagation delay of 1.4 ns typical
- Low 100 mW power dissipation at maximum speed
- Output driver produces high-impedance when disabled or when power supply is off
- Pin compatible with SN65LVDS31
- PTN3331 drives 100 Ω point-to-point load environment
- PTN3341 drives 50 Ω multi-drop load environment
- Offered in 16-pin TSSOP and SO packages

Features—PTN3332 and PTN3342 LVDS Line Receivers

- Support high data rates of up to 400 Mbit/s
- Four independent channels per IC with common disable
- Low channel skew (<300 ps)
- Low part-to-part skew (<1 ns)
- Propagation delay of 2.1 ns typical
- Low 60 mW power dissipation at maximum speed
- Input open-circuit failsafe
- Pin compatible with SN65LVDS32
- PTN3342 includes integrated 100 Ω receiver termination resistor
- Offered in 16-pin TSSOP and SO packages

Description

In systems requiring high-speed signals to be transported over greater distances—such as from board to board within an enclosure, or from one system to another over cable—oftentimes LVDS is the signaling standard of choice. LVDS uses differential signaling to overcome common-mode noise typically picked up by cabling, while keeping power low by using only a 400 mV



voltage swing. LVDS receivers are capable of correctly receiving a differential input signal as small as 100 mV over a wide input common-mode range, so that some voltage drop over cable length can be tolerated. Edge rates are kept within moderate speeds to both maintain low EMI as well as low switching power. This combination of favorable characteristics has made LVDS a preferred signaling method in telecommunications, networking and industrial applications in medium to high speed backplane, point-to-point and multi-point configurations.

The PTN333x/PTN334x family of devices allows high-speed LVTTL-based designs to easily take advantage of LVDS interfacing by providing translation (in either direction) in a single device. The drivers (PTN3331 or PTN3341) accept a single-ended LVTTL input signal on each of their four channels, and translate it to differential LVDS. The receivers (PTN3332 or PTN3342) accept LVDS input signals and convert to single-ended LVTTL. This family can be used for data rates of up to 400 Mbit/s per channel or to translate clock signals of up to 200 MHz.

Two driver types are provided: PTN3331 for typical point-to-point LVDS applications, which employ 100 Ω receiver-end resistive termination; and PTN3341 designed for higher drive capability in multi-drop LVDS applications, in which case the transmission medium is terminated at both ends of the bus in 100 Ω , resulting in a 50 Ω load to the driver.

The receiver is also available in two variants: with (PTN3342) or without (PTN3332) internal receiver termination resistor across its differential inputs. This eliminates the need for external termination resistors in point-to-point applications. However, in multi-drop applications the bus is terminated and not the receivers, which requires that the receivers loading the bus not have built-in termination. Both PTN3332 and PTN3342 are equipped with input open-circuit failsafe circuitry, which detects an open-circuit condition at the receiver input, and forces the output driver in a HIGH state, thus preventing the output driver from going into an indeterminate state.

All four devices are pin-, form-, and function-compatible with the corresponding functions from the SN65LVDS31 and SN65LVDS32 series of devices to allow interchangeability and multiple sourcing of critical functions.

For high-performance logic translation between LVDS and differential PECL, the PTN3310 and PTN3311 may be used.

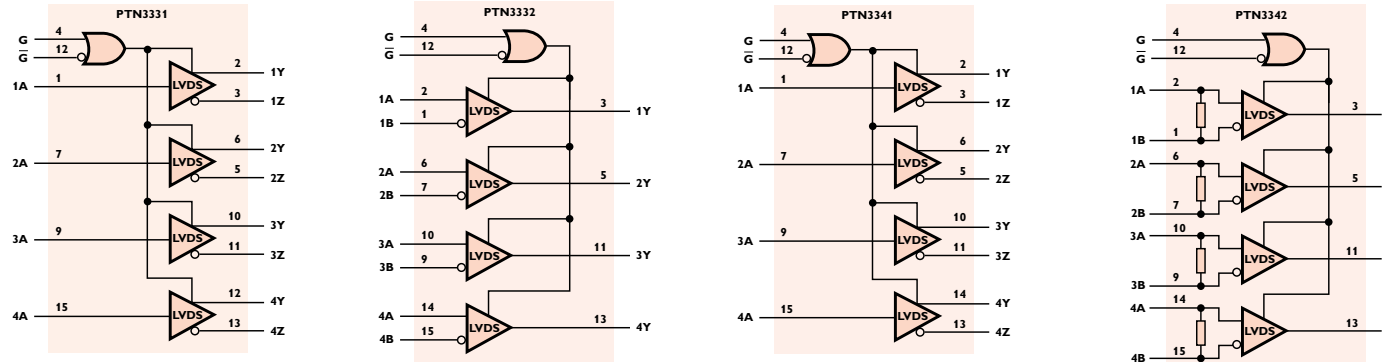
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Block Diagrams



Order Information

Package	Container	PTN3331	PTN3332	PTN3341	PTN3342
SO	Tube	PTN3331D	PTN3332D	PTN3341D	PTN3342D
	Tape & Reel	PTN3331D-T	PTN3332D-T	PTN3341D-T	PTN3342D-T
TSSOP	Tube	PTN3331DH	PTN3332DH	PTN3341DH	PTN3342DH
	Tape & Reel	PTN3331DH-T	PTN3332DH-T	PTN3341DH-T	PTN3342DH-T

Device Selection Table

PTN3331	PTN3341	PTN3332	PTN3342
Quad LVDS driver	Quad LVDS driver	Quad LVDS receiver	Quad LVDS receiver
Point-to-point	Multi-drop	No built-in receiver termination resistor	100 Ω built-in receiver termination resistor
Compatible with SN65LVDS31	Compatible with SN65LVDM31	Compatible with SN65LVDS32	Compatible with SN65LVDS32

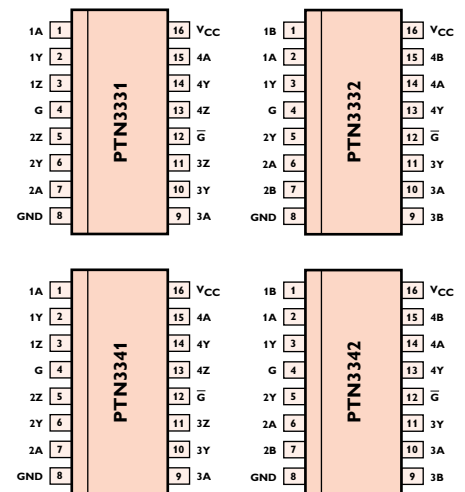
Applications

- Point-to-point or multi-point high speed differential data transmission
- Low-voltage swing, low-EMI signaling environments with high common-mode noise rejection requirements
- High-performance telecommunications and networking systems

Operating Characteristics

- Operates from 3.3 V power supply
- Meets or exceeds the requirements of ANSI TIA/EIA-644 standard for low-voltage differential signaling
- -40°C to +85°C operating temperature range
- Input frequency range of 0 to 200 MHz
- Input data rates of up to 400 Mbit/s per channel

Pin Configurations



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