

# LFPAK thermal design guide

LFPAK thermal performance junction to ambient

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## 1. Introduction

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For surface mount power devices, the total thermal path from junction to ambient ( $R_{th(j-a)}$ ) is critical in determining the safe operation and maximum usable current. In most practical applications, however, determination of  $R_{th(j-a)}$  is often very difficult as there may be two or more thermal paths from junction to ambient in parallel and characterisation of the individual paths may not be straightforward. For a power semiconductor mounted on a PCB, the primary thermal pathway from junction to ambient is vertically downwards, through the copper leadframe of the device and into the PCB (this method of cooling is essentially using the PCB as a heatsink). Although the thermal resistance through the device leadframe is easily determined by reference to the device datasheet (see  $R_{th(j-mb)}$ ), the thermal resistance from the PCB to ambient is not easily quantifiable, and hence the total thermal resistance from junction to ambient cannot be easily calculated.

## 2. Thermal performance junction to ambient

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In order to assist the circuit designer in utilizing Philips LFPAK in high power designs, a series of measurements has been performed to determine the  $R_{th(j-a)}$  for LFPAK device when mounted on PCBs of various types and sizes. As there is a large number of possible PCB shapes and sizes, it was found necessary to rationalise the board shape to squares with the LFPAK device mounted centrally within the squares. The graphs of [Figure 1](#) show  $R_{th(j-a)}$  for LFPAK mounted on 2-layer and 4-layer PCBs, with side lengths of 10 mm, 20 mm and 30 mm.



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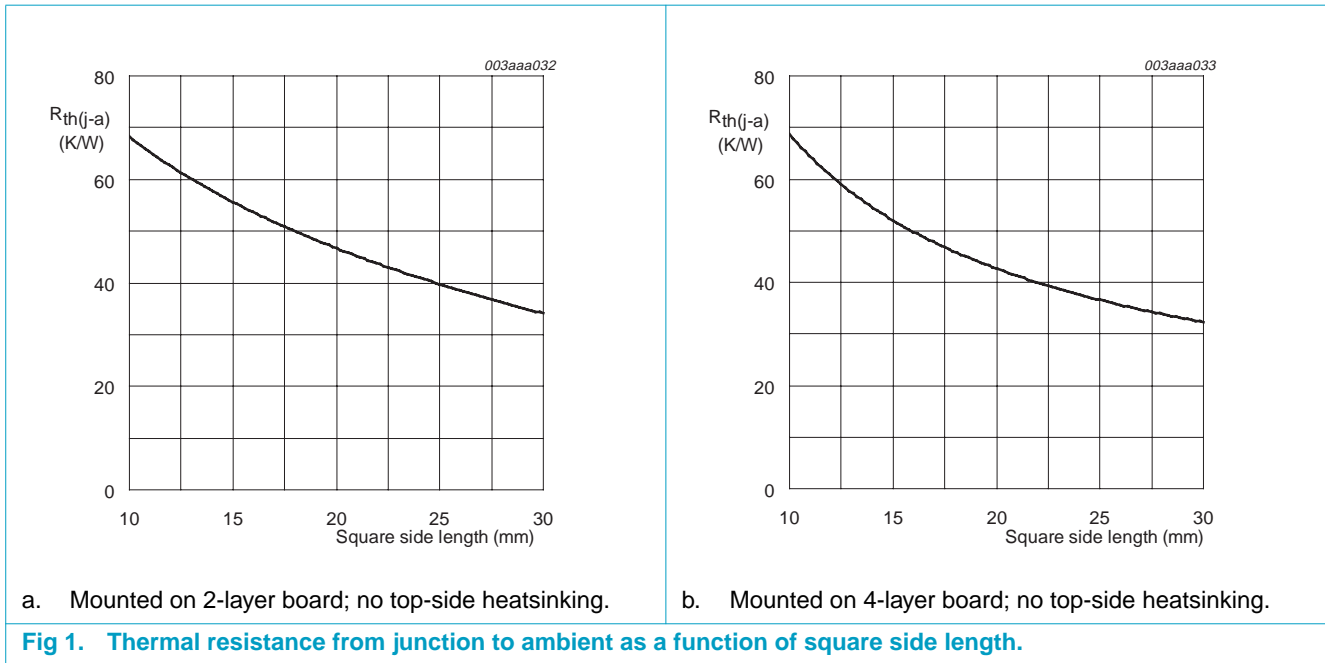
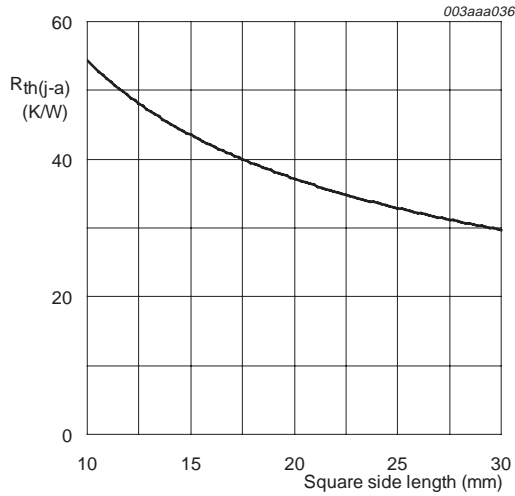


Fig 1. Thermal resistance from junction to ambient as a function of square side length.

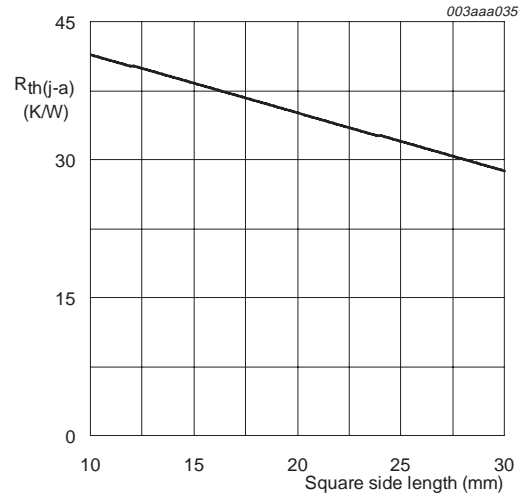
### 3. Thermal performance junction to ambient with top-side cooling

The graphs of Figure 1 demonstrate cases where the primary thermal pathway from junction to ambient is through the device leadframe and PCB. However, a second thermal pathway also exists through the top of the device package. For a D-PAK or a D<sup>2</sup>-PAK device, the thermal resistance of this “top-side” pathway is very high compared to the path through the device leadframe and PCB and hence most of the device dissipation is channelled to ambient through the leadframe and PCB. However, the internal construction of the LFPAK package drastically reduces the thermal resistance of the top-side thermal pathway, and hence very effective top-side cooling may be realized when a heatsink is mounted directly on top of the LFPAK device. The application of both top-side cooling and cooling through the PCB results in an extremely low total thermal resistance from junction to ambient for the LFPAK.

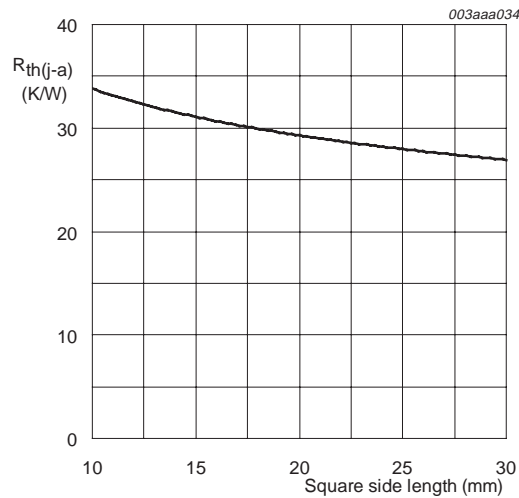
As mentioned previously, values of  $R_{th(j-a)}$  are difficult to calculate for this method of cooling, so a series of measurements has been performed to determine the  $R_{th(j-a)}$  for LFPAK devices when mounted on the three sizes of 4-layer PCB and with square top-side heatsinks of dimensions 10 mm x 10 mm, 20 mm x 20 mm and 30 mm x 30 mm. The heatsink material is 3 mm aluminium plate. The results are shown in the graphs of Figure 2. Note that electrical insulation between the top-side of LFPAK and the heatsink is **not** required, even when a heatsink is in contact with multiple LFPAK devices, as the top of the device is electrically isolated from the active parts of the device. It is good practice, however, to apply a thin film of thermally conductive grease to the top of the LFPAK package before fitting the heatsink in order to enhance the thermal conduction between the package and the heatsink.



a. Mounted on 4-layer board;  
10 mm x 10 mm top-side heatsink.



b. Mounted on 4-layer board;  
20 mm x 20 mm top-side heatsink.



c. Mounted on 4-layer board; 30 mm x 30 mm top-side heatsink.

**Fig 2. Thermal resistance from junction to ambient as a function of square side length.**

## 4. Design example

Determination of the maximum current capability of a PH3230S mounted on a 20 mm x 20 mm PCB, with a 20 mm x 20 mm top-side heatsink and an ambient temperature of 25 °C.

$$R_{th(j-a)} = 35 \text{ K/W (from graphic b in Figure 2)}$$

$$T_{amb} = 25 \text{ °C}$$

$$T_{j(max)} = 150 \text{ °C (so } \Delta T_j = 125 \text{ °C)}$$

$$R_{DSon} @ 150 \text{ °C} = 5.8 \text{ m}\Omega \text{ (from datasheet)}$$

$$P_D = \frac{\Delta T_j}{R_{th(j-a)}} \quad (1)$$

$$P_D = \frac{125}{35} = 3.6 \text{ W} \quad (2)$$

$$P_D = I_D^2 \times R_{DSon} \quad (3)$$

$$I_D = \sqrt{\frac{P_D}{R_{DSon}}} \quad (4)$$

$$I_D = \sqrt{\frac{3.6}{0.0058}} = 24.9 \text{ A} \quad (5)$$



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