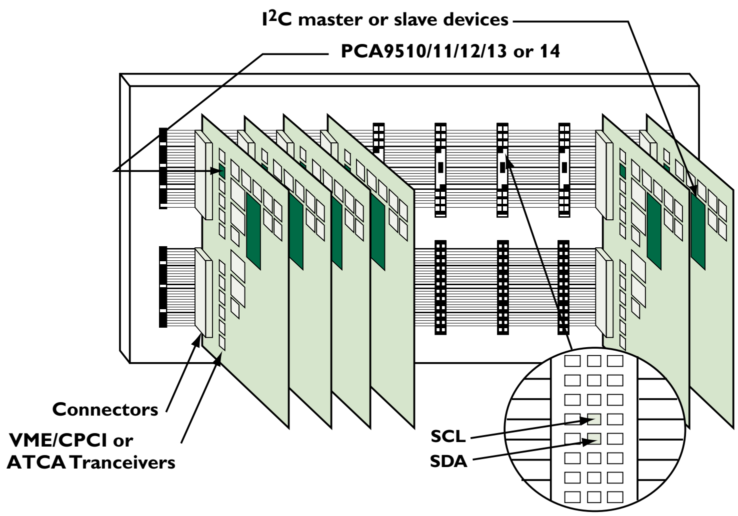
PCA9510/11/12/13/14

Level shifting and hot swappable I²C and SMBus bus buffers

Semiconductors



Description

Specifically designed for backplane multi-point and hot swap applications; the PCA9510/11/12/13/14/15 Hot Swappable Bus Buffers isolate the backplane and card capacitance to permit the design of larger systems. The devices support live insertion with idle detect and precharge features, since PICMG 2.9 CompactPCI/VME and PICMG 3.x AdvancedTCA cards must be hot-swappable without corrupting the I²C bus data. All devices are bi-directional, requiring no directional control and are suitable for multi-master I²C bus or SMBus environments by supporting bus arbitration and contention with master devices located on any I²C segments. They operate up to 400 kHz with a supply voltage from 2.7 V to 5.5 V and have 5.5 V tolerant I/Os.

Features

- Bi-directional buffers for the I²C bus clock (SCL) and data (SDA) lines increase fanout and prevent corruption of the active I²C bus data during board insertion or removal from the backplane
- Compatible with I²C standard mode (0 – 100 kHz), I²C fast mode (0 – 400 kHz), and SMBus (10 – 100 kHz)
- Support clock stretching, multiple master arbitration and synchronization
- Operating power supply voltage range from 2.7 V to 5.5 V with 5.5 V tolerant I/Os
- Operational temperature range from -40 °C to 85 °C
- Offered in 8 pin SO and TSSOP (MSOP) packages

Benefits

- Allow insertion of cards into active I²C or SMBus for 24/7 operation without powering down the system and without corrupting the I²C bus data
- Allow use of I²C or SMBus in multi-point architectures
- Allow building of expandable systems without modifying current architecture
- Easy implementation; no programming required
- Small footprint 8 pin package

Applications

- Insertion/removal of unpowered cards into an active I²C or SMBus
- More I²C devices or larger wiring capacitance than the 400 pF maximum allowed in the I²C specification
- Different operating supply voltages or logic voltage levels within one system
- Isolation of sections within the I²C or SMBus
- Long bus wiring or multi-point backplane traces

Feature selection chart

Features	PCA9510	PCA9511	PCA9512	PCA9513	PCA9514
Idle detect	Yes	Yes	Yes	Yes	Yes
High impedance SDA, SCL, pins for V_{CC} = 0 V	Yes	Yes	Yes	Yes	Yes
Rise time accelerator circuitry on all SDA and SCL lines	—	Yes	Yes	Yes	Yes
Rise time accelerator circuitry hardware disable pin for lightly loaded systems	—	—	Yes	—	—
Rise time accelerator threshold 0.8 V vs. 0.6 V improves noise margin	—	—	Yes	Yes	Yes
Ready open drain output	Yes	Yes	—	Yes	Yes
Two V_{CC} pins to support 5 V to 3.3 V level translation with improved noise margins	—	—	Yes	—	—
1 V precharge on all SDA and SCL lines	In only	Yes	Yes	—	—
100 µA current source on SCLIN and SDAIN for PICMG applications	—	—	—	Yes	—

PHILIPS

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The I²C bus is used for system management functions in larger systems and the PCA9510/11/12/13/14 devices may be needed to help buffer the capacitance and provide hot swap capability. One primary system management architecture is Intelligent Platform Management Interface (IPMI), which is an Intel initiative in conjunction with Hewlett-Packard, NEC and Dell for server applications and consists of three specifications:

- **Intelligent Platform Management Interface (IPMI)** – software extensions provide a self monitoring capability that increases the reliability of the system and monitors the platform physical health characteristics such as: temperatures, voltages, fans and chassis intrusion, and provides general system management such as: automatic alerting, automatic system shutdown and re-start, remote re-start and power control.
- **Intelligent Platform Management Bus (IPMB)** – intra-chassis (dark green line inside the box) connections using I²C/SMBus as the physical means to transfer information.
- **Inter Chassis Management Bus (ICMB)** – inter-chassis (lime green line outside the box) connection using various means like RS-485, CAN or I²C to transfer information.

This new standard is needed as the complexity of systems increase and MTBF decreases, so there needs to be a way to monitor and control platform components outside of the normal system operation loop. This means that failures can be detected and corrected to keep the system operating. IPMI uses the proven capabilities of the I²C bus to provide a self monitoring capability that increases system reliability.
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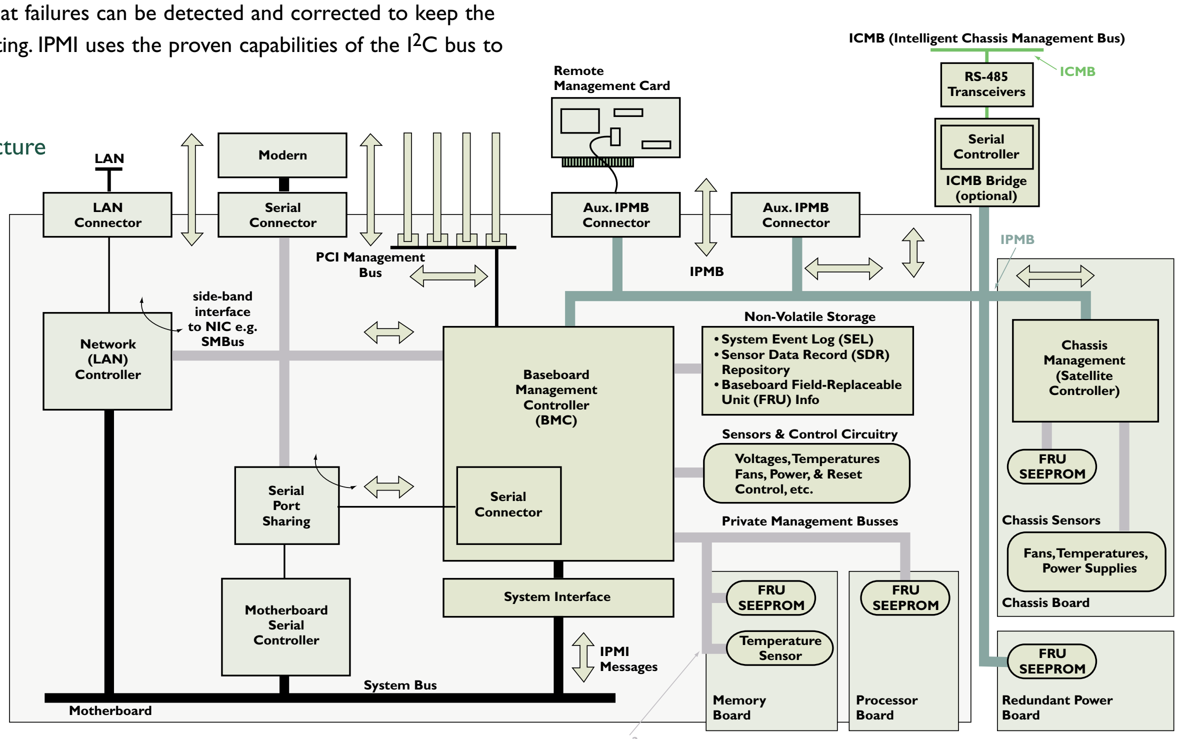
Features include:

- I²C based
- Multi-master capable
- Simple Request/Response Protocol
- IPMI Command set based
- Supports non-IPMI devices
- Physical I²C but write only (master capable devices)
- Enables the Baseboard Management Controller (BMC) to accept IPMI request messages from other management controllers in the system
- Allows non-intelligent devices as well as management controllers on the bus

The BMC serves as a controller to give system software access to the IPMB (hot swap is not required since servers can be powered down to insert or remove cards).

The PCA9510/11/12/13/14 Hot Swappable Bus Buffers can be used on the various boards that plug into the motherboard to isolate the bus capacitance to each board. The Private Management Busses (gray line on boards) are local I²C busses for communications with various slave devices (e.g., temperature sensor and EEPROMs) using normal I²C protocols.

IPMI architecture



Use of IPMI in PICMG Architectures – The PICMG (PCI Industrial Computer Manufacturers Group) is a consortium of over 600 companies, who collaboratively develop open interconnection specifications for high performance telecommunications and industrial computing platforms. PICMG specifications that use IPMI include PICMG 2.9 for CompactPCI® applications and the recently announced PICMG 3.x for AdvancedTCA™, new larger form factor rack mount boards for next-generation telecommunications equipment that is based on switched fabric architectures and has mandatory dual redundant IPMBs. PICMG requires the hot swappable features of the PCA9510/11/12/13/14 Hot Swappable Bus Buffers since telecom/computing equipment can't be powered down to insert or remove cards.

Use of IPMI in VME Architecture – The VME draft standard VITA38 suggests IPMI as the system management protocol by using the PICMG 2.9 system management specification with pin configuration changes (VME backplane connectors are different from CompactPCI) and maximum capacitance changes (CompactPCI can have a maximum of 8 slots while VME can have a maximum of 21 slots).

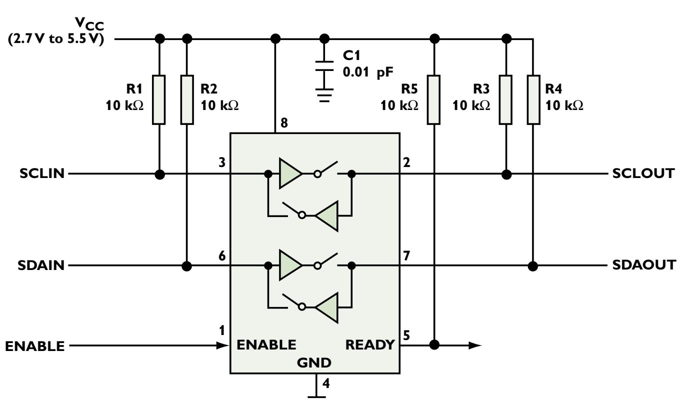
PCA9510, PCA9511, PCA9513 and PCA9514 description

The PCA9510, PCA9511, PCA9513, and PCA9514 are hot swappable I^2C and SMBus buffers that allow I/O card insertion into a live backplane without corrupting the clock or data buses. Control circuitry prevents the backplane I^2C bus from being connected to the card I^2C bus until a Stop command or bus idle occurs on the backplane. When the connection is made, the bus buffers provide bi-directional buffering, keeping the backplane and card capacitances isolated.

The PCA9510/11/12/13/14 incorporate:

- A digital ENABLE input pin, which enables the device when asserted HIGH and forces the device into a low current mode when asserted LOW
- An open-drain READY output pin, which indicates that the backplane and card sides are connected together (HIGH) or not (LOW).

Typical application drawing



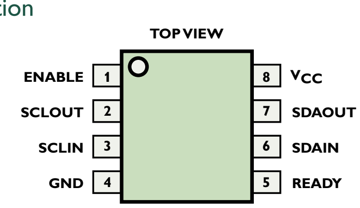
R1 and R2 are not required for PCA9513 applications since the internal 100 µA current source maintains the SCLIN and SDAIN lines high.

Rise time accelerator circuitry allows the use of weaker DC pull-up resistors while still meeting rise time requirements. The PCA9513 and PCA9514 rise time accelerator threshold has been moved from 0.6 V to 0.8 V to provide better noise margin and is deactivated on the PCA9510.

During insertion, the PCA9510/11 SDA and SCL lines are precharged to 1 V to minimize the current required to charge the parasitic capacitance of the chip and prevent glitching the I^2C bus. The PCA9513 and PCA9514 do not have this feature since the precharge is detrimental in some applications and new resistive tip pins are more effective than precharge in some live insertion applications.

The PCA9513 supplies a 100 µA current source to the SCLIN and SDAIN pins in lieu of using pull-up resistors for PICMG backplane applications. Including the current source into the device reduces parts count and provides for a consistent RC time constant as cards are removed and inserted into the backplane. As more cards are added (increasing the bus capacitance) the effective pull-up resistance decreases (more current sources in parallel) which maintains the RC time constant value level.

Pin configuration



PCA9510/11/13/14

Pin description

Pin	Symbol	Description
1	ENABLE	Chip enable pin. Grounding this pin puts the part in a low current (<1 µA) mode. It also disables the rise time accelerators. Isolates SDAIN from SDAOUT and isolates SCLIN from SCLOUT.
2	SCLOUT	Serial clock output to and from the SCL bus on the card.
3	SCLIN	Serial clock input to and from the SCL bus on the backplane.
4	GND	Ground. Connect this pin to a ground plane for best results.
5	READY	This is an open-drain output which pulls LOW when SDAIN and SCLIN are disconnected from SDAOUT and SCLOUT, and turns off when the two sides are connected.
6	SDAIN	Serial data input to and from the SDA bus on the backplane.
7	SDAOUT	Serial data output to and from the SDA bus on the card.
8	V_{CC}	Power supply.

Ordering information

Package	Container	PCA9510	PCA9511	PCA9512	PCA9513	PCA9514
SO	Tube	PCA9510D	PCA9511D	PCA9512D	PCA9513D	PCA9514D
	T & R	PCA9510D-T	PCA9511D-T	PCA9512D-T	PCA9513D-T	PCA9514D-T
TSSOP	T & R	PCA9510DP-T	PCA9511DP-T	PCA9512DP-T	PCA9513DP-T	PCA9514DP-T

In Europe and Asia, add ",112" for tube orders and substitute ",118" for "-T" for tape and reel orders (e.g., PCA9511D,112 and PCA9511D,118). Additional technical information can be found in Application Note AN10160 (www.semiconductors.philips.com/logic/support/appnotes/i2c) and additional information on packages including outline dimensions, MSL ratings, Theta JA can be obtained at www.semiconductors.philips.com/logic/packaging.

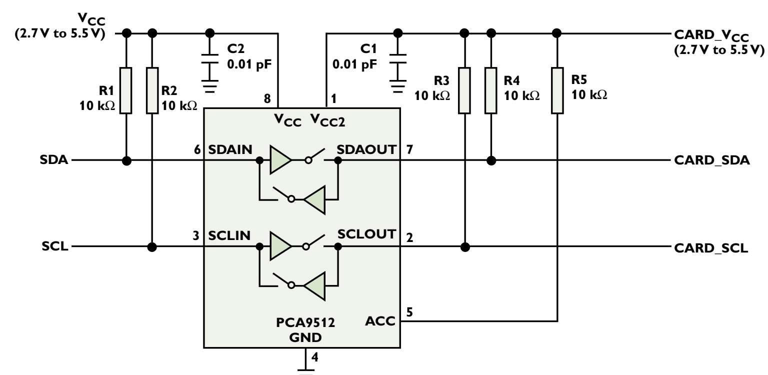
PCA9510/11/12/13/14

Level shifting and hot swappable I^2C and SMBus bus buffers

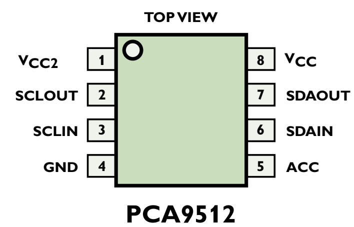
PCA9512 description

The PCA9512 is a hot-swappable I^2C and SMBus buffer that allows I/O card insertion into a live backplane without corrupting the data and clock buses. It is similar to the PCA9511, excluding the digital ENABLED input pin (pin #1) and the open-drain READY output pin (pin #5). The PCA9512 replaces the ENABLE pin with a dedicated supply voltage pin, $V_{CC}2$, for the card side. This provides level shifting between 3.3 V and 5 V systems with optimal noise margin. Both the backplane and card may be powered with supply voltages ranging from 2.7 V to 5.5 V, with no constraints on which supply voltage is higher. The READY pin is replaced with a digital COS input pin (ACC), which enables when connected to $V_{CC}2$, or disables when connected to ground the rise-time accelerator currents for lightly loaded circuits.

PCA9512 block diagram



Pin configuration



Pin description

Pin	Symbol	Description
1	V_{CC2}	Supply voltage for devices on the card I^2C busses. Connect pull-up resistors from SDAOUT and SCLOUT to this pin.
2	SCLOUT	Serial clock output to and from the SCL bus on the card.
3	SCLIN	Serial clock input to and from the SCL bus on the backplane.
4	GND	Ground. Connect this pin to a ground plane for best results.
5	ACC	CMOS threshold digital input pin that enables and disables the rise-time accelerators on all four SDA and SCL pins. ACC enables all accelerators when set to V_{CC2}, and turns them off when set to GND.
6	SDAIN	Serial data input to and from the SDA bus on the backplane/ long distance bus.
7	SDAOUT	Serial data output to and from the SDA bus on the card.
8	V_{CC}	Power supply from the backplane, connect pull-up resistors from SDAIN and SCLIN to this pin.

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